HD49319F

CMOS 9-Bit A/D Converter

HITACHI

ADE-207-122 (Z)
Rev. 0
November 1993

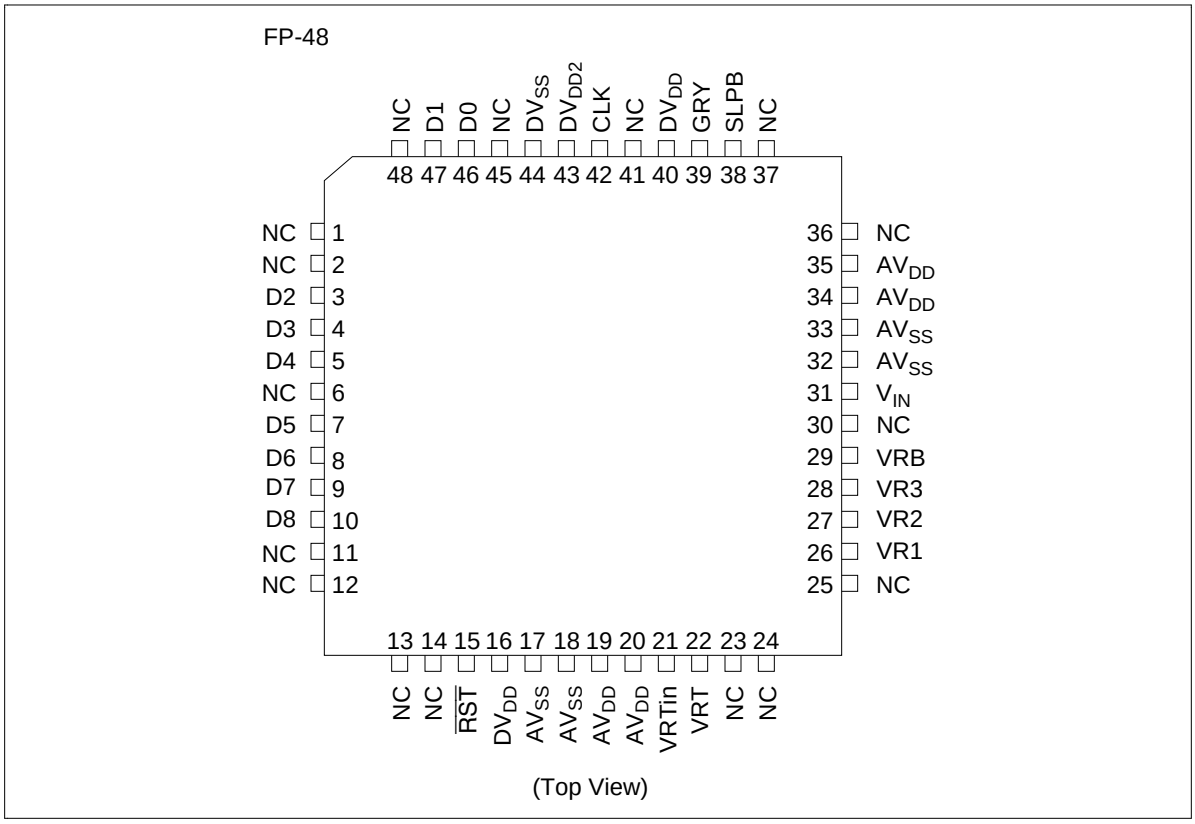
Description

The HD49319F is a high-speed, low-power monolithic CMOS 9-bit A/D converter LSI.

Features

- Resolution: 9 bits
- Double +5.0 V/+3.3 V power supply (Digital output only: +3.3 V)
- Output codes: binary/gray, selectable
- Low voltage interface possible (+3.3 V)
- Sleep mode provided (low-power waiting mode)
- Reset function provided

Pin Arrangement



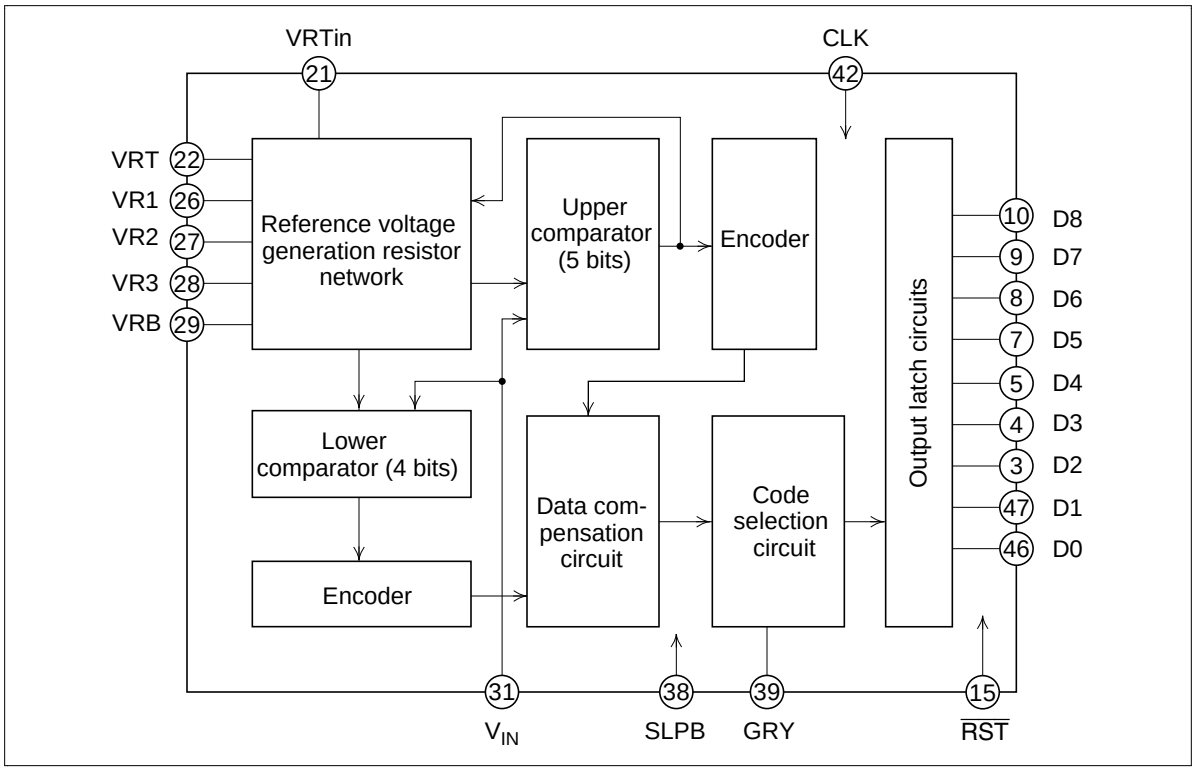
Pin Description

Pin No.	Symbol	Function
1, 2	NC	Unused
3 to 5	D2 to D4	Digital output
6	NC	Unused
7 to 9	D5 to D7	Digital output
10	D8	Digital output (MSB)
11 to 14	NC	Unused
15	$\overline{RST}$	Reset signal input
16	DV_{DD}	Digital power supply (+5 V), Connect this pin in common with AV_{DD} external to the IC.
17, 18	AV_{SS}	Analog ground (0 V)
19, 20	AV_{DD}	Analog power supply (5 V)
21	VRTin	Reference voltage op-amp input (high side: +3 V or 0 V). When the internal op-amp is used, input +3 V to this pin. When unused, connect to AV_{SS}.
22	VRT	Reference voltage input (high side: +3 V). When the internal op-amp is used, insert both a 0.1 µF ceramic capacitor and an over 10 µF chemical capacitor between this pin and AV_{SS}. When unused, apply +3.0 V to this pin.
23 to 25	NC	Unused
26 to 28	VR1 to VR3	Reference voltage intermediate taps. Insert 0.1 µF capacitors between these pins and AV_{SS}.
29	VRB	Reference voltage input (low side: 0 V). Apply a 0 V reference voltage, or connect to AV_{SS}.
30	NC	Unused
31	V_{IN}	Analog signal input (0 to +3 V)
32, 33	AV_{SS}	Analog ground (0 V)
34, 35	AV_{DD}	Analog power supply (+5 V)
36 to 37	NC	Unused
38	SLPB	Sleep mode control input H: Normal operating mode L: Sleep mode
39	GRY	Output code selection input H: Gray code L: Binary code

Pin Description (cont)

Pin No.	Symbol	Function
40	DV_{DD}	Digital power supply (+5 V). Connect this pin in common with AVDD external to the IC.
41	NC	Unused
42	CLK	Conversion clock input (TTL or CMOS)
43	DV_{DD2}	Digital power supply (+3.3 V)
44	DV_{SS}	Digital ground (0 V). Connect this pin in common with AV_{SS} external to the IC.
45	NC	Unused
46	D0	Digital output (LSB)
47	D1	Digital output
48	NC	Unused

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rated Value	Units
Power supply voltage 1	$V_{DD(max)}$	6.0	V
Power supply voltage 2	$DV_{DD2(max)}$	6.0	V
Input signal	$V_{IN(max)}$	–0.3 to V_{DD} + 0.3	V
Reference pin voltage	$V_{REF(max)}$	–0.3 to V_{DD} + 0.3	V
Digital input voltage	$V_{I(max)}$	–0.3 to V_{DD} + 0.3	V
Reference pin voltage difference	$V_{RT} – V_{RB}$	3.1	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

Notes: 1. V_{DD} refers to both AV_{DD} and DV_{DD}.
2. Connect AV_{DD} and DV_{DD} to a common point outside the IC. If AV_{DD} and DV_{DD} are separated by a noise filter, make sure that their voltages differ by less than 0.3 V or power up, and by less than 0.1 V during operation.
3. Connect AV_{SS} and DV_{SS} to a common point outside the IC.

Electrical Characteristics (Unless otherwise specified, V_{DD} = 5.0 V, DV_{DD2} = 3.3 V, V_{RT} = 3.0 V, V_{RB} = 0.0 V, Ta = 25°C, and the internal op-amp is unused.)

Item	Symbol	Min	Typ	Max	Units	Measurement Conditions	Note
Resolution	RES	9	9	9	bit		
Power supply voltage	V_{DD}	4.75	5.00	5.25	V		
range	DV_{DD2}	3.0	3.3	V_{DD}	V		
Power supply current	I_{DD1} *1	—	18	23	mA	f_{CLK} = 15 MHz , f_{IN} = 1 kHz	
	I_{DD2} *2	—	1	3	mA	sine wave	
Reference resistance	R_{REF}	300	480	—	Ω	Resistance between, V_{RT} and V_{RB}	
Analog input current	I_{IN} *3	–400	—	400	µA	V_{IN} : 0 to 3 V, f_{CLK} = 15 MHz	
Digital output voltage	V_{OH}	V_X–0.5*4	—	DV_{DD2}	V	I_{OH} = –2 mA	
	V_{OL}	—	—	0.5	V	I_{OL} = 2 mA	
Op-amp offset	VRTin-VRT	–30	—	30	mV	VRTin = 3.0 V, (When the op-amp is used)	
Digital input voltage	$V_{IH(SLPB)}$	2	—	V_{DD}	V		
(SLPB)	$V_{IL(SLP)}$	0	—	0.3	V		
Digital input voltage	V_{IH}	2	—	V_{DD}	V		
(other than SLPB)	V_{IL}	0	—	0.8	V		

Electrical Characteristics (Unless otherwise specified, V_{DD} = 5.0 V, DV_{DD2} = 3.3 V, V_{RT} = 3.0 V, V_{RB} = 0.0 V, Ta = 25°C, and the internal op-amp is unused.) (cont)

Item	Symbol	Min	Typ	Max	Units	Measurement Conditions	Note
Digital input current	I_{IH}	–50	—	50	µA	$V_{IH} = V_{DD}$	
	I_{IL}	–50	—	50	µA	V_{IL} = 0 V	
	$I_{IL(\overline{RST})}$	–200	—	50	µA	V_{IL} = 0 V	
Op-amp input current	I_{OP}	–50	—	50	µA	VRTin = 3 V	
Maximum conversion speed	$f_{CLK(max)}$	15	—	—	MHz		1
Minimum conversion speed	$f_{CLK(min)}$	—	—	0.5	MHz		
Minimum clock pulse	$t_{WH(min)}$	—	—	30	ns		
width	$t_{WL(min)}$	—	—	30	ns		
Maximum clock pulse	$t_{WH(max)}$	1	—	—	µs		
width	$t_{WL(max)}$	1	—	—	µs		
Digital output delay time	t_{PD}	—	—	38	ns	Load capacitance = 10 pF	
Digital output hold time	t_{HOLD}	8	—	—	ns		
Analog signal read-in time	t_{AP}	–5	6	10	ns		
Integration linearity	I_{NL}	—	2	5.5	LSBpp	f_{CLK} = 15 MHz	
Differentiation linearity	DNL	–0.7	—	+0.7	LSB		
Reset pulse width	T_{RH}	$3\times1/f_{CLK}$	—	—			
	T_{RL}	$3\times1/f_{CLK}$	—	—			

Notes: *1. I_{DD1} is Quiescent current of V_{DD}.

*2. I_{DD2} is Quiescent current of DV_{DD2}.

*3. I_{IN} is not transition current, but static current.

*4. In case of

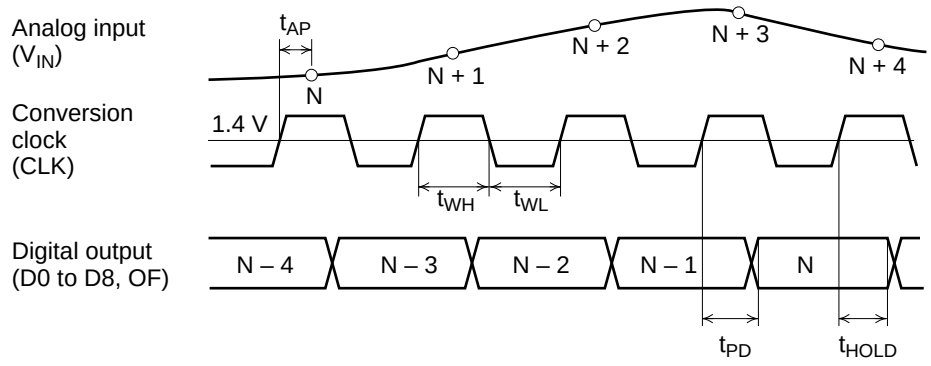
$V_{DD} – 1V > DV_{DD2} \rightarrow V_X = DV_{DD2}$

$V_{DD} – 1V < DV_{DD2} \rightarrow V_X = V_{DD} – 1V$

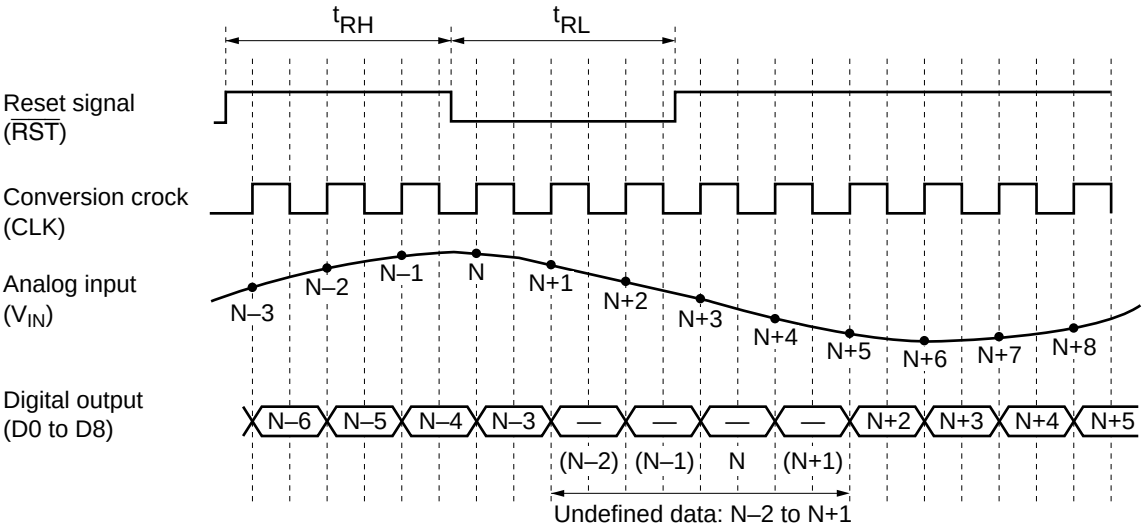
1. With the change in input voltage between conversions on each clock 2.2 V or less.

Timing Chart

• **Conversion timing**



• **Reset signal specification**



Cautionary Items

Power Supply Current

When the internal op-amp is used, the current which drives the reference resistors is added to the power supply current.

Sleep Mode

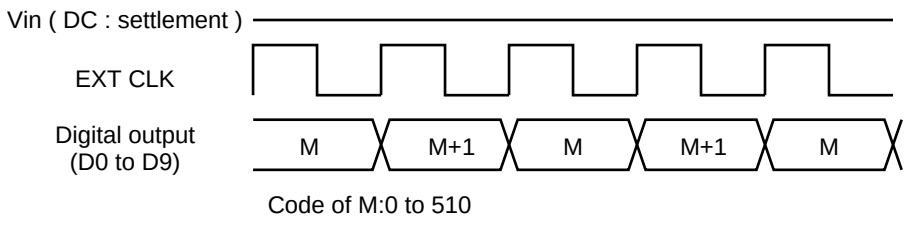
When the SLPB pin input signal is low, the chip enters sleep mode. This allows the IC's power supply current to be held to almost zero.

During sleep mode, the internal circuits are stopped and the digital outputs are undefined (either high or low).

During sleep mode using the internal op-amp, the internal op-amp is also stopped and the reference voltage is not applied to the reference resistors for saving the power supply current.

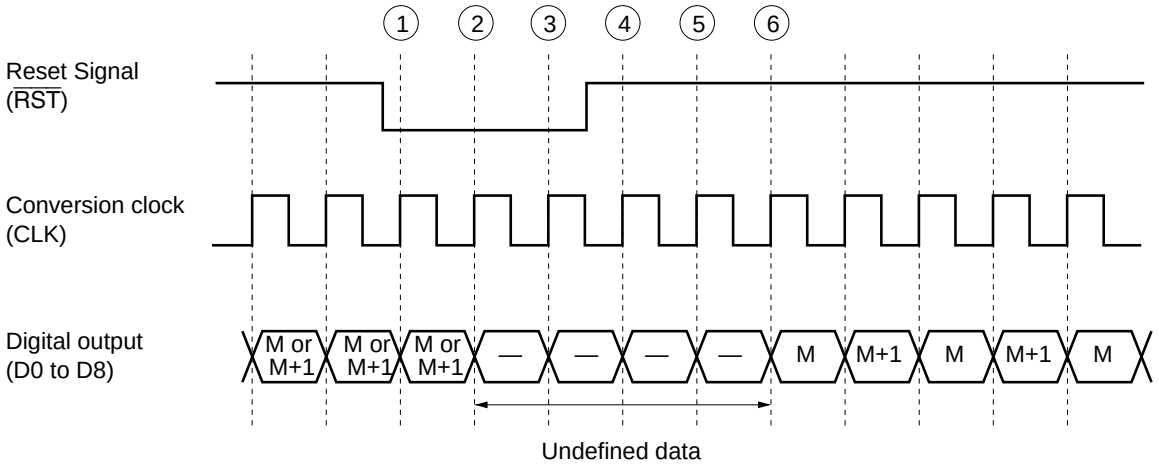
After clearing sleep mode by setting the SLPB input high, input at least 5 clock cycles to restore the chip to normal operation. When the internal op-amp is used, input at least 5 clock cycles after the reference voltage was restored.

This IC has the characteristics such that digital data charge 1 LSB (2 LSB max.) at everyclock pulse for each level of DC input data. Be careful this could be a problem in some cases.

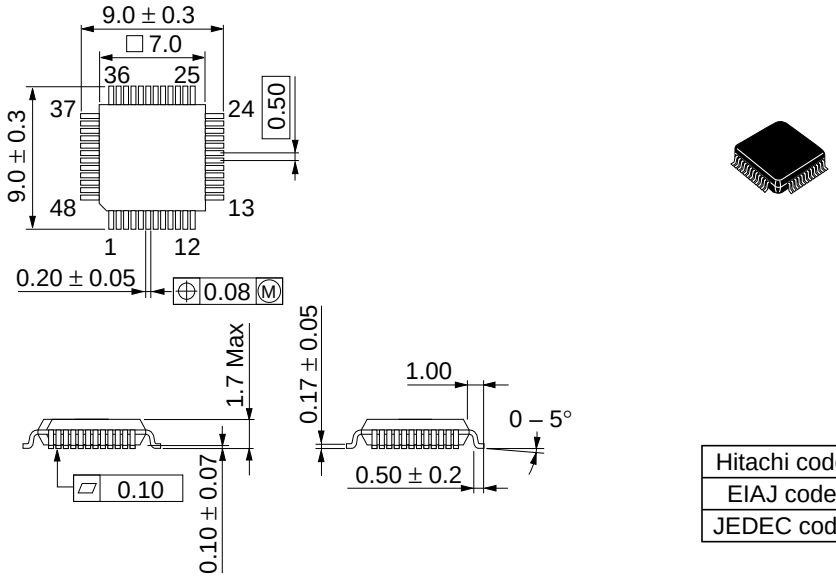


• Using the Reset Function

This IC has the characteristics shown in the over figure. When the reset function is not used, whether operation starts from M or M+1 is determined when power is applied, but were operation starts is indeterminate prior to power application. When the reset function is used, operation starts from data M from the sixth clock cycle counted from the falling edge of the reset signal($\overline{RST}$) as shown in the figure below. Note that V_{IN} is DC.



Package Dimension (Unit: mm)



Hitachi code	FP-48
EIAJ code	—
JEDEC code	SC-592-A

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