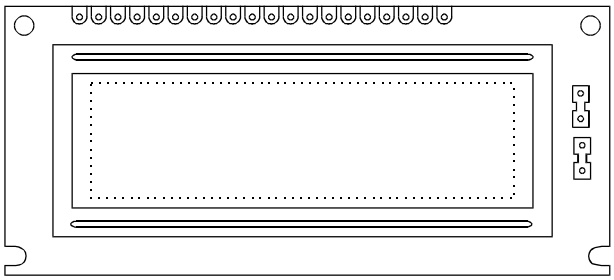
HANTRONIX

PRODUCT SPECIFICATION

HDM32GS12-1

122 x 32 GRAPHICS
LCD DISPLAY MODULE



HANTRONIX, INC. 10080 BUBB RD. CUPERTINO, CA 95014	**Q.A.:** JB	**REV.:** 1.0	HDM32GS12-1	SHEET 1 OF 7 **DATE:** 2/4/98

■ Absolute Maximum Ratings

Parameter	Symbol	Rated Values	Unit
Supply voltage(1)	VSS	-8.0～-0.3	V
Supply voltage(2)	V5	-16.5～0.3	V
Supply voltage(3)	V1,V4,V2,V3	V5～0.3	V
Input voltage	V1	VSS-0.3～0.3	V
Output voltage	VO	VSS-0.3t0.03	V
Permissible loss	PD	250	mv
Operating temperature	Tapr	0～+50	℃
Storage temperature	Tsth	-20～+60	℃
Solder temperature	Tol	260 ℃ for～3s	—

■ Pin Description

Pin Name	Function
DB0～DB7	Data input
A0	Selects display data or instructions. HIGH:Display data. LOW:instructions.
$\overline{RES}$	Resets the system and selects the interface type for a 68-port/80-port MPU. HIGH:68-port MPU interface. LOW:80-port MPU interface.
$\overline{CS}$	Chip Select input. LOW:Active level sensing.
E ($\overline{RD}$)	Read/Write Enable signal when a 68-port MPU is connected. (Active-LOW Read Enable signal when an 80-port MPU is connected.)
R/$\overline{W}$ ($\overline{WR}$)	Read/Write Select signal when a 68-port MPU is connected. HIGH:Read Select LOW:Write Selext (Active-LOW Write Enable input when an 80-port MPU is connected. Rising edge sensing.)
CL	External clock input(only effective with external clock types).
VDD	5V power supply.
VSS	0V power supply (GND level).
VO	VO=-5V contrast adjustment.

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics

(V_{DD}=0V, Ta=−20to75°C)

Parameter		Symbol	Condition		Applicable Terminals	Min	Typ	Max	Unit
Operating voltage (1)*1	Recommended operation	Vss			Vss	−5.5	−5.0	−4.5	V
	Potential operation					−7.0	—	−2.4	
Operating voltage (2)	Recommended operation	V5			V5	−13.0	—	−3.5	V
	Potential operation					−13.0	—	—	
	Potential operation	V1, V2			V1, V2	0.6×V5	—	V_{DD}	
	Potential operation	V3, V4			V3, V4	V5	—	0.4×V_{DD}	
HIGH input voltage		V_{IHT}			A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$ pins	Vss+2.0	—	V_{DD}	V
		V_{IHC}			CL, FR, M/$\overline{S}$, $\overline{RES}$ pins	0.2×Vss	—	V_{DD}	
LOW input voltage		V_{ILT}			A0, D0~D7, E, R/$\overline{W}$, $\overline{CS}$ pins	Vss	—	Vss+0.8	V
		T_{ILC}			CL, FR, M/$\overline{S}$, $\overline{RES}$ pins	Vss	—	0.8×Vss	
HIGH output voltage		V_{OHT}	I_{OH}=−3.0 mA		D0~D7 pins	Vss+2.4	—	—	V
		V_{OHC1}	I_{OH}=−2.0 mA		FR pins	Vss+2.4	—	—	
		V_{OHC2}	I_{OH}=−120 μA		OSC2	0.2×Vss	—	—	
LOW output voltage		V_{OLT}	I_{OL}=3.0 mA		D0~D7, FR pins	—	—	Vss+0.4	V
		V_{OLC1}	I_{OL}=2.0 mA		FR pins	—	—	Vss+0.4	
		V_{OLC2}	I_{OL}=120 μA		OSC2	—	—	0.8×Vss	
Input leak current		I_{LI}			A0, E, R/$\overline{W}$, $\overline{CS}$, CL, $\overline{RES}$, M/$\overline{S}$ pins	−1.0	—	1.0	μA
Output leak current		I_{LO}	Applicable when FR is in a high-impedance state		D0~D7, FR pins	−3.0	—	3.0	
LCD driver ON resistance		R_{ON}	Ta=25°C	V5=−5.0V	SEG0~60	—	5.0	7.5	kΩ
				V5=−3.5V	COM0~15	—	10.0	50.0	
Static current consumption		I_{DDQ}	$\overline{CS}$=CL=V_{DD}			—	0.05	1.0	μA
Active current consumption	External CLK	$I_{DD(1)}$	During display	fCL=2kHz	V_{DD}	—	2.0	5.0	
	Oscillator			RI=1MΩ		—	9.5	15.0	
				fCL=18kHz		—	5.0	10.0	
		$I_{DD(2)}$	During access t_{CYC}=200kHz			—	300	500	
Input terminal capacity		C_{IN}	Ta=25°C, f=1MHz		All input terminals	—	5.0	8.0	pF
Oscillating frequency		fosc	RI=1.0MΩ±2%, Vss=−5.0V			15	18	21	kHz
			RI=1.0MΩ±2%, Vss=−3.0V			11	16	21	
Reset time		tR			$\overline{RES}$	1.0	—	1000	μs

* 1 A wide range of operating voltages is guaranteed, except in case of abrupt voltage fluctuations during MPU access.

● AC Characteristics

○ Read/Write timing for the 80-port MPU

(Ta=−20to75°C, Vss=−5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		10	—	—	ns
Address set-up time		t_{AW8}		20	—	—	ns
System cycle time	$\overline{WR}$, $\overline{RD}$	t_{CYC8}		1000	—	—	ns
Control pulse width		t_{CC}		200	—	—	ns
Data set-up time	D0toD7	t_{DS8}		80	—	—	ns
Data hold time		t_{DH8}		10	—	—	ns
$\overline{RD}$ access time		t_{ACC8}	CL=100pF	—	—	90	ns
Output disable time		t_{OH8}		10	—	60	ns

* 2 The ratings when Vss=−3.0V are approximately 100% higher than when Vss=−5.0V.

○ Read/Write timing for the 68-port MPU

(Ta=−20to75°C, Vss=−5.0V±10%)

Parameter	Signal	Symbol	Condition	Min	Typ	Max	Unit
System cycle time	A0, $\overline{CS}$ R/$\overline{W}$	t_{CYC6} *3		1000	—	—	ns
Address set-up time		t_{AW6}		20	—	—	ns
Address hold time		t_{AH6}		10	—	—	ns
Data set-up time	D0toD7	t_{DS6}		80	—	—	ns
Data hold time		t_{DH6}		10	—	—	ns
Output disable time		t_{OH6}	CL=100pF	10	—	60	ns
Access time		t_{ACC6}		—	—	90	ns
Enable pulse width READ	E	t_{EW}		100	—	—	ns
Enable pulse width WRITE				80	—	—	ns

* 3 t_{CYC6} indicates the cycle during which $\overline{CS}$/E are HIGH; it does not indicate the cycle of the E signal.

* 4 The ratings when Vss=−3.0V are approximately 100% higher than when Vss=−5.0V.

■ Optical Characteristics

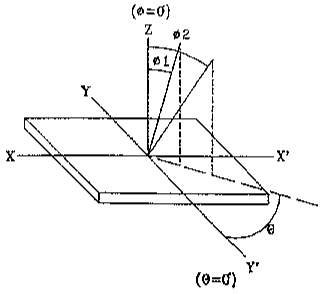
1 . STN TYPE

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	$\phi 2-\phi 1$	K=1.4	40	—	—	deg.	*1,*2
Contrast Ratio	K	ϕ =10℃ θ = 0℃	—	3	—	—	*3
Response Time(Rise)	tr	ϕ =10℃ θ = 0℃	—	150	250	ms	*4
Response Time(Fall)	tf	ϕ =10℃ θ = 0℃	—	200	300	ms	*4

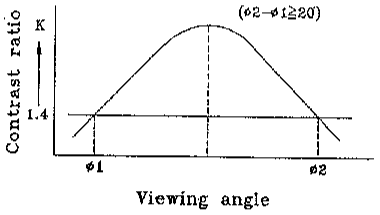
2 . TN TYPE

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	$\phi 2-\phi 1$	K=1.4	60	—	—	deg.	*1,*2
Contrast Ratio	K	ϕ =25℃ θ = 0℃	—	3	—	—	*3
Response Time(Rise)	tr	ϕ =25℃ θ = 0℃	—	80	120	ms	*4
Response Time(Fall)	tf	ϕ =25℃ θ = 0℃	—	60	90	ms	*4

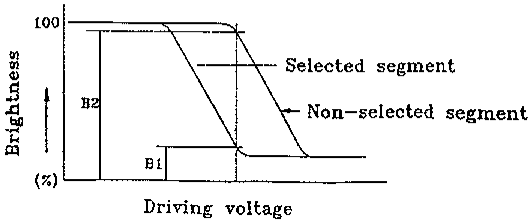
*1. Definition of Q AND φ



*2. Contrast vs viewing angle

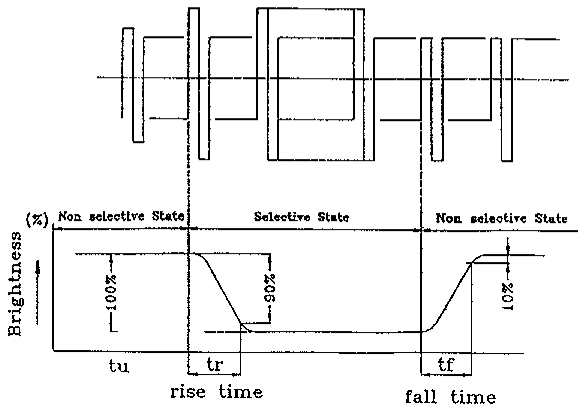


*3. definition of contrast ratio



$$K=\frac{\text{Brightness of non-selected segment(B2)}}{\text{Brightness of selected segment(B1)}}$$

*4. Definition of optical response



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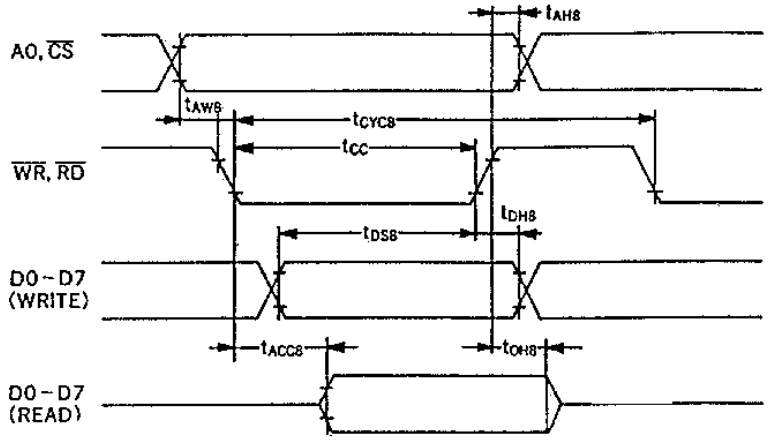
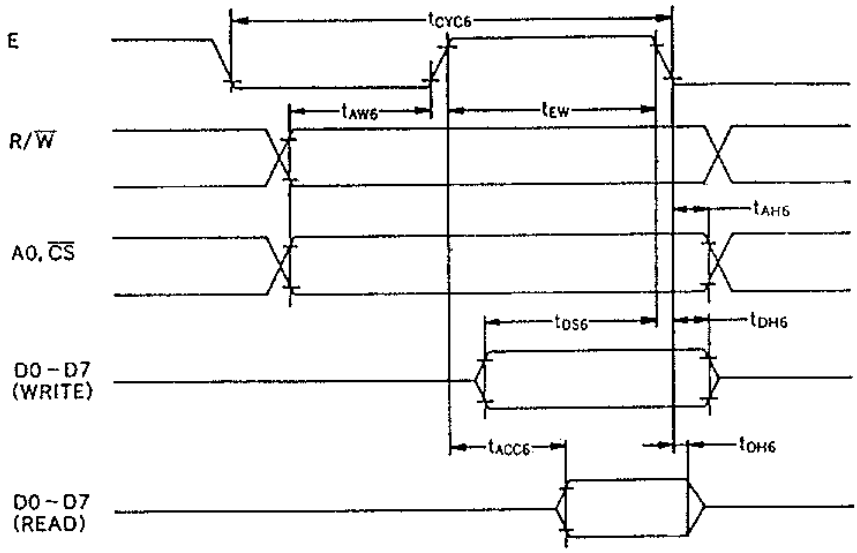
● Timing Chart

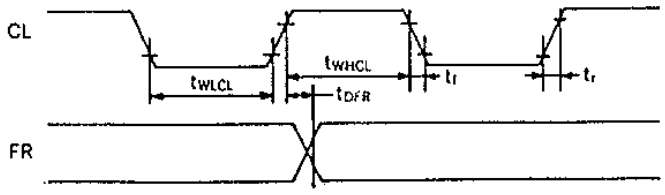
○ Read/Write timing for the 80-port MPU



○ Read/Write timing for the 68-port MPU



○ Control timing for 80-port/68-port display



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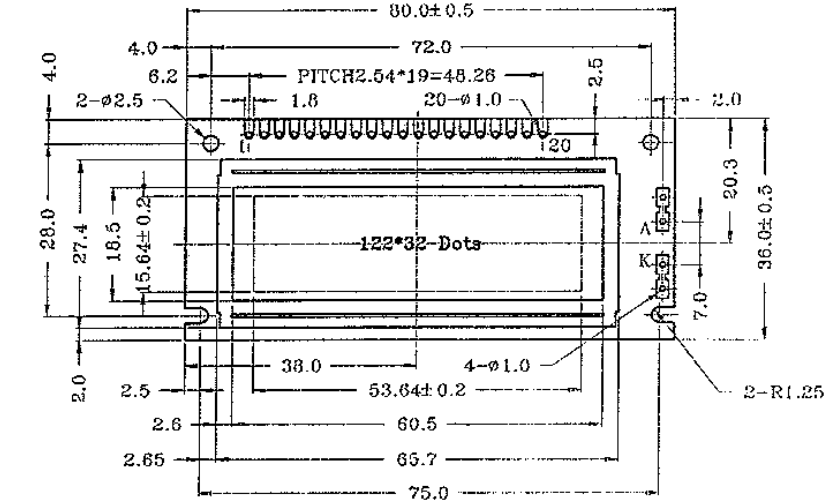
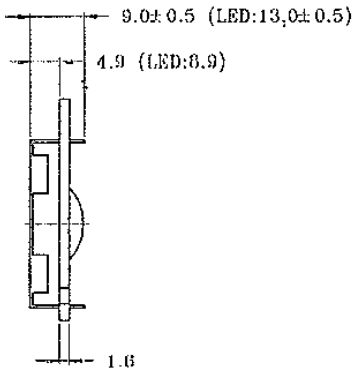
■ DISPLAY COMMANDS

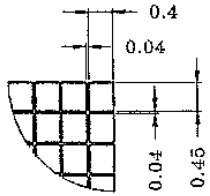
(Based on the 80-port MPU; the $\overline{RD}$ and $\overline{WR}$ commands differ for the 68-port MPU.)

	Command	$\overline{RD}$ $\overline{WR}$ A0	D7 D6 D5 D4 D3 D2 D1 D0	Function
1	Display ON/OFF	1 0 0	1 0 1 0 1 1 1 0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. *7
2	Display START Line	1 0 0	1 1 0 Display START address (0~31)	Determines the line of RAM data to be displayed at the display's top line (COM0).
3	Page Address Set	1 0 0	1 0 1 1 1 0 Page (0~3)	Sets the page of the Display RAM in the page address register.
4	Column (Segment) Address Set	1 0 0	0 Column address (0~79)	Sets the column address of the Display RAM in the column address register.
5	Status Read	0 1 0	BUSY ADC ON/OFF RESET 0 0 0 0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1 0 1	Write Data	Writes the data on the data bus to RAM. These commands access a previously-specified address of the Display RAM, after which the column address is incremented by one.
7	Read Display Data	0 1 1	Read Data	Reads data from the Display RAM onto the data bus.
8	ADC Select	1 0 0	1 0 1 0 0 0 0 0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1 0 0	1 0 1 0 0 1 0 0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) *7 0: Normal display operation
10	Duty Select	1 0 0	1 0 1 0 1 0 0 0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11	Read Modify Write	1 0 0	1 1 1 0 0 0 0 0	Increments the column address counter by one only when display data is written but not when it is read.
12	End	1 0 0	1 1 1 0 1 1 1 0	Cancels the Ready Modify Write mode.
13	Reset	1 0 0	1 1 1 0 0 0 1 0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

*7. Power Save mode is entered by selecting static drive in Display OFF status.

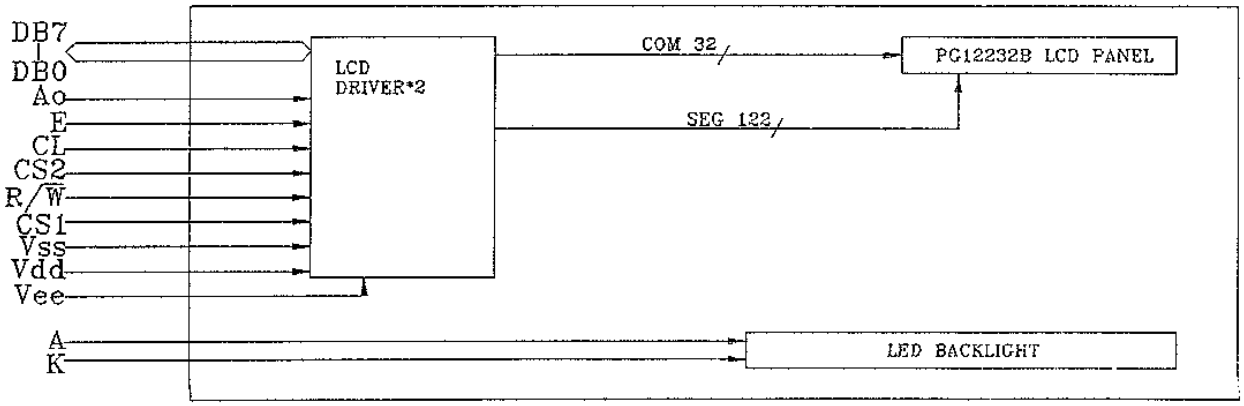






SCALE:10/1

PIN NO.	SIGNAL
1	Vss
2	Vdd
3	Vee
4	Ao
5	CS1
6	CS2
7	CL
8	/RD(E)
9	/WR(R/W)
10	DB0
11	DB1
12	DB2
13	DB3
14	DB4
15	DB5
16	DB6
17	DB7
18	RES
19	A
20	K



The tolerance unless classified ±0.3mm

UNIT:mm

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