16Mx64 bit SDRAM Unbuffered DIMM H-Series

PC/100 SDRAM Specification Supporting
based on 16Mx8 SDRAM, LVTTL, 4-Banks & 4K Refresh
HYM71V651601

PRELIMINARY

DESCRIPTION

The HYM71V651601 H-Series are high speed 3.3-Volt Synchronous DRAM Modules composed of eight 16Mx8 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E^2PROM on a 168-pin glass-epoxy printed circuit board. One 0.33μF and one 0.1μF decoupling capacitors per each SDRAM are mounted on the module.

The HYM71V651601 H-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 128M bytes memory. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- 1.375" (34.93mm) PCB Height
- One Row of SDRAMs
- 168-Pin Unbuffered DIMM
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms
- All inputs and outputs referenced to positive edge of system clock
- Internal four banks operation
- Programmable Burst Length and Burst Type
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 2,3 clocks
- Data mask function by DQM

ORDERING INFORMATION

Part No.	Clock Frequency	Power	PCB Height	Package	Based Comp. Part No
HYM71V651601TH-8	125MHz	Normal	1.375	TSOPII	HY57V1298020TC-8
HYM71V651601TH-10P	100MHz				HY57V1298020TC-10P
HYM71V651601TH-10S	100MHz				HY57V1298020TC-10S
HYM71V651601LTH-8	125MHz	Low Power			HY57V1298020LTC-8
HYM71V651601LTH-10P	100MHz				HY57V1298020LTC-10P
HYM71V651601LTH-10S	100MHz				HY57V1298020LTC-10S

PIN DESCRIPTION

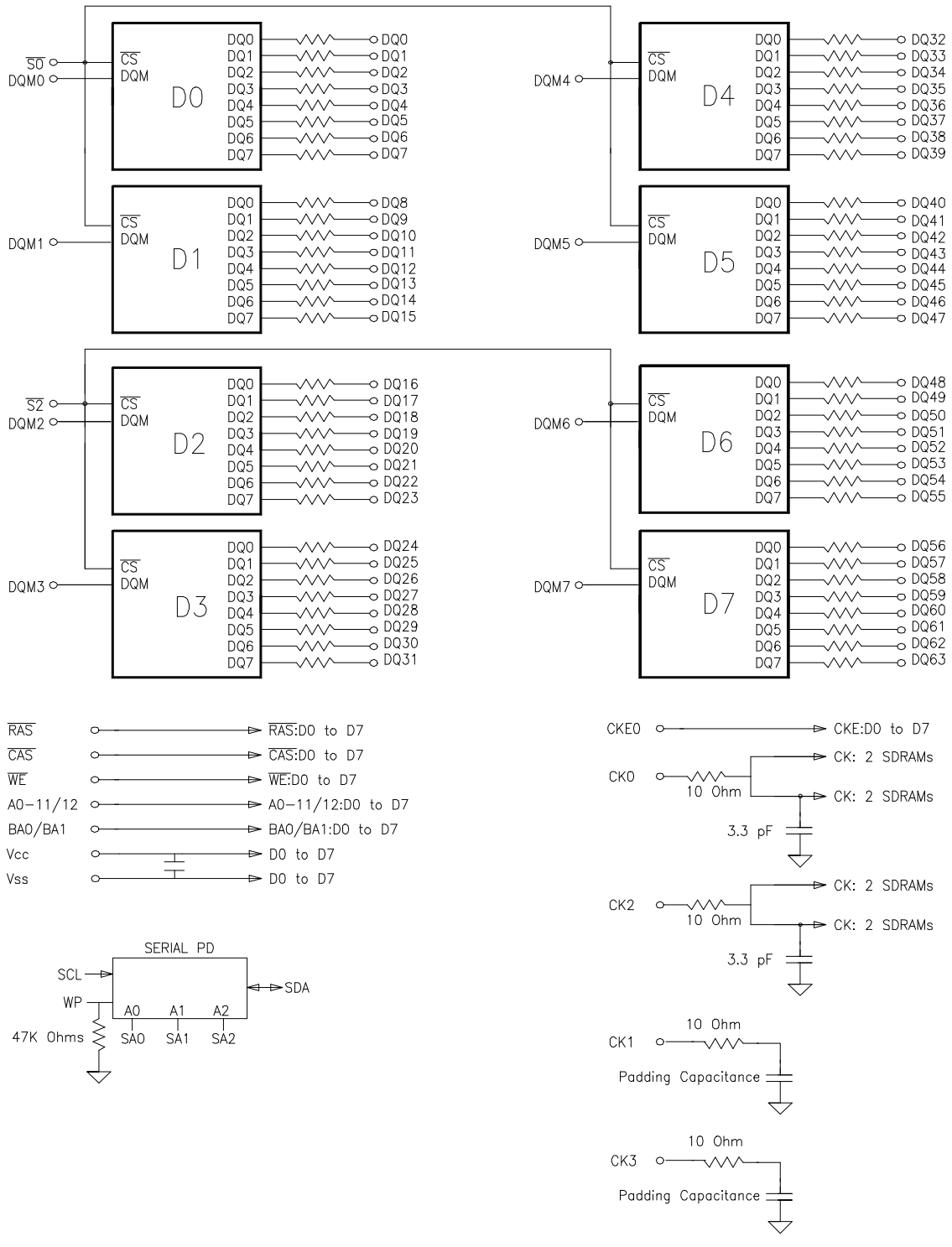
Pin	Pin Name	Description
CK0-CK3	Clock	The system clock input; All other inputs are registered to the SDRAM on the rising edge of CLK. CK1 and CK3 are not used in this module.
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0,/S2	Chip Select	Command input enable of mask except CLK, CKE and DQM
/RAS, /CAS,/WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation. Refer function truth table for details
DQM0-7	Data Input / Output Mask	DQM control output buffer in read mode and masks input data in write mode
DQ0-DQ63	Data Input / Output	Multiplexed data input / output pin
BA0, BA1	Bank Address	Select either one of banks during both /RAS and /CAS activity
A0-A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA9 Auto-precharge flag: A10
Vcc/Vss	Power Supply/Ground	Power supply and ground for internal circuit and input buffer
SDA	Serial Address and Data Input / Output.	Serial Address and Data Input / Output for EEPROM
SCL	Serial Clock	Serial Clock
SA0-SA2	INPUT	Addresses in Serial E^2PROM for Socket Presence.
WP	Write Protection	EEPROM Write Protection

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	NC
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	Vcc	48	NC	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/S0	72	DQ27	114	NC	156	DQ59
31	NC	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	*CK3
38	A10(AP)	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	*CK1	167	SA2
42	CK0	84	Vcc	126	NC	168	Vcc

Note : 1. CK1 and CK3 are connected with termination R/C (Refer to the block diagram)

BLOCK DIAGRAM



Note : 1. The serial resistor values of DQs are 10 Ohms.

2. The padding capacitance of termination R/C for CK1/3 is 10pF.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION -8	FUNCTION -10P	FUNCTION -10S	VALUE -8	VALUE -10P	VALUE -10S	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	12			0Ch			1
BYTE4	# of Column Addresses on This Assembly	10			0Ah			
BYTE5	# of Module Banks on This Assembly	1 Banks			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @ /CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	µs			80h			
BYTE13		X8			8h			
	Error Checking SDRAM Width	None			h			
BYTE15	imum Clock Delay Back to Back Random Column	tCCD=1 Latency						
BYTE16	Burst Lengths Supported				8Fh			2
	# of Banks on SDRAM Device	4			04			
BYTE18	CAS # Latency				06			
BYTE19	CS # Latency				01h			
BYTE20		/WE Latency=0			01h			
	SDRAM Module Attributes	Neither Buffered nor			00h			
	SDRAM Module Attributes,	+/-10% voltage tolerance, Burst read, Single bit write, precharge, Early /RAS			0E			
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	12ns		12ns	C0h		C0h	
BYTE2	Access Time from Clock 2	6ns		6ns	60h		60h	
BYTE2	SDRAM Cycle Time 1	-		-	00h		00h	
BYTE2	Access Time from Clock 1	-		-	00h		00h	
BYTE2	Minimum Row Precharge Time (	20ns	20ns		14h	14h		
BYTE28	tRRD)	16ns		20ns	10h		14h	
BYTE2	Minimum /RAS to /CAS Delay (tRCD)		20ns	20ns		14h	14h	
30	Minimum /RAS Pulse width (	48ns	50ns		30h	32h		
BYTE31		128MB			20h			
32	Command & Address signal input setup time (	2ns	2ns		20h	20h		
BYTE33	tAH)	1ns		1ns	10h		10h	
BYTE	Data signal input setup time (tDS)		2ns	2ns		20h	20h	
35	Data signal input hold time (	1ns	1ns		10h	10h		
BYTE36 -	Superset Information(May be used in the future)	-						
BYTE62		Intel SPD 1.2A			12h			
BYTE63		-	-		10h	16h		
BYTE64		Hyundai JEDEC ID			AD			
BYTE65 -	Manufacturer JEDEC ID Code	Unused			h			
BYTE	Manufacturing Location	HEI (Korea) HEU (Europe)			0 h 02h			

SERIAL PRESENCE

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION			VALUE			NOTE
		-8	-10P	-10S	-8	-10P	-10S	
BYTE73-90	Manufacturer's Part Number (SDRAM) except 'HYM'	-			-			6
BYTE73	Manufacturer's Part Number(SDRAM)	7			37h			6
BYTE74	Manufacturer's Part Number(128M bit based)	1			31h			6
BYTE75	Manufacturer's Part Number(3.3V)	V			56h			6
BYTE76	Manufacturer's Part Number(Data Width)	6			36h			6
BYTE77	Manufacturer's Part Number(Data Width)	5			35h			6
BYTE78	Manufacturer's Part Number(Memory Depth)	1			31h			6
BYTE79	Manufacturer's Part Number(Memory Depth)	6			36h			6
BYTE80	Manufacturer's Part Number(Refresh)	0(4K Ref.)			30h			6
BYTE81	Manufacturer's Part Number(4 Internal Bank)	1			31h			6
BYTE82	Manufacturer's Part Number(TSOPII Mounted)	T			54h			6
BYTE83	Manufacturer's Part Number(x4 Registered)	H			48h			6
BYTE84	Manufacturer's Part Number(Hyphen)	'-'			2Dh			6
BYTE85	Manufacturer's Part Number(Min. Cycle Time)	8	1	1	38h	31h	31h	6
BYTE86	Manufacturer's Part Number(Min. Cycle Time)	Blank	0	0	20h	30h	30h	6
BYTE87	Manufacturer's Part Number(Min. Cycle Time)	Blank	P	S	20h	50h	53h	6
BYTE88-90	Manufacturer's Part Number	Blanks			20h			6
BYTE91	Revision Code for Components	Process Code			-			3, 6
BYTE92	Revision Code for PCB	Process Code			-			3, 6
BYTE93	Manufacturing Date	Work Week			-			3, 5
BYTE94	Manufacturing Date	Year			-			3, 5
BYTE95 - 98	Assembly Serial Number	-			-			3
BYTE99 - 125	Manufacturer Specific Data (May be used in the Future)	None			00h			
BYTE126	System Frequency support	100MHz			64h			4
BYTE127	Intel Specification details for 100MHz Support	Note 7			A7h	A7h	A5h	
BYTE128 -256	Unused storage locations	-			00h			4

Note: 1. The bank address is excluded.
2. In interleaved type, the burst lengths supported is 1, 2, 4, 8.
3. Not fixed but dependent.
4. Refer to Intel SPD 1.2A specifications.
5. BCD adopted.
6. ASCII adopted.
7. CLK0-3 connected to the DIMM, TBD junction temp, CL=2(3) support and supporting Intel defined Concurrent Auto Precharge.
8. In case of L-part , character 'L' will be added between byte 81 and byte 82.

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	8	W
Soldering Temperature · Time	T_{SOLDER}	260·10	°C · Sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

DC OPERATING CONDITIONS (T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1
Input High Voltage	V_{IH}	2.0	3.0	V_{CC} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	1, 3

Note :
1. All voltages are referenced to Vss=0V
2. V_{IH}(max) is acceptable 5.6V AC pulse width with <= 3ns of duration.
3. V_{IL}(min) is acceptable –2.0V AC pulse width with <= 3ns of duration.

AC OPERATING CONDITIONS (T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

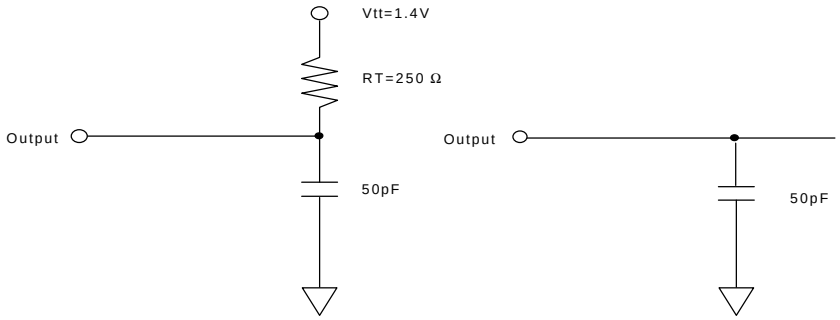
Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor(50pF).
For details, refer to AC/DC output load circuit.

CAPACITANCE

(T_A=25°C, f=1MHz)

Parameter	Pin	Symbol	Typ.	Max.	Unit
Input Capacitance	A0-A11, BA0/BA1	C_{IN1}	-	55	pF
Input Capacitance	/RAS, /CAS, /WE	C_{IN2}	-	50	pF
Input Capacitance	/S0, /S2	C_{IN3}	-	30	pF
Input Capacitance	CK0,CK2	C_{IN4}	-	40	pF
Input Capacitance	CKE0	C_{IN5}		50	pF
Input Capacitance	DQM0-DQM7	C_{IN6}	-	20	pF
Output Capacitance	DQ0-DQ63	C_{OUT}	-	15	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS I

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Input Leakage Current	I_{LI}	-8	8	μA	1
Output Leakage Current	I_{LO}	-1	1	μA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +4mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not under test = 0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6V

DC CHARACTERISTICS(II)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition		Speed			Unit	note
				-8	-10P	-10S		
Operating Current	ICC1	Burst Length=1, One bank active tRAS≥tRAS(min), tRP≥tRP(min), I_{OL}=0mA		960	960	960	mA	1
Precharge Standby Current in power down mode	ICC2P	CKE≤V_{IL}(max),tCK=min		16			mA	
	ICC2PS	CKE≤V_{IL}(max),tCK=∞		12				
Precharge Standby Current in non power down mode	ICC2N	CKE≥V_{IH}(min), /CS≥V_{IH}(min),tCK=min Input signals are changed one time during 2Clks. All other pins≥V_{DD}-0.2V or ≤0.2V		160			mA	
	ICC2NS	CKE≥V_{IH}(mim),tCK=∞ Input signals are stable		80				
Active Standby Current in power down mode	ICC3P	CKE≤V_{IL}(max),tCK=min		56			mA	
	ICC3PS	CKE≤V_{IL}(max),tCK=∞		56				
Active Standby Current in non power down mode	ICC3N	CKE≥V_{IH}(min), /CS≥V_{IH}(min),tCK=min Input signals are changed one time during 2CLKs. All other pins≥V_{DD}-0.2V or ≤0.2V		320			mA	
	ICC3NS	CKE≥V_{IH}(mim),tCK=∞ Input signals are stable		320				
Burst Mode Operating Current	ICC4	tCK≥tCK(min), Continuous burst,I_{OL}=0mA All banks active	CL=3	1120	960	960	mA	1
			CL=2	960	960	880		
Auto Refresh Current	ICC5	tRRC≥tRRC(min), all banks active		1360			mA	2
Self Refresh Current	ICC6	CKE≤0.2V		16			mA	3
				6.4			mA	4

Note :
1. ICC1 and ICC4 depend on output loading and cycle rates. Specified values are measured with the output open.
2. Minimum of tRRC (Refresh /RAS cycle time) is listed on AC characteristic II.
3. HYM71V651601TH-8/10P/10S
4. HYM71V651601LTH-8/10P/10S

AC CHARACTERISTICS I

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CL=3	tCK3	8	1000	10	1000	10	1000	ns	
	CL=2	tCK2	12		10		12		ns	
Clock High Pulse Width		tCHW	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	3	-	3	-	3	-	ns	1
Access Time From Clock	CL=3	tAC3	-	6	-	6	-	6	ns	2
	CL=2	tAC2	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	1	-	1	-	1	-	ns	1
CLK to Data Output in Low Z-Time		tOLZ	1	-	1	-	1	-	ns	
CLK to Data Output in High Z-Time	CL=3	tOHZ3	3	6	3	6	3	6	ns	
	CL=2	tOHZ2	3	6	3	6	3	6	ns	

Note : 1. Assumed tR / tF(input rise and fall time) is 1ns.
2. Access times to be measured with input signals of 1V/ ns edge rate, 0.8V to 2.0V

AC CHARACTERISTICS II

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
/RAS cycle time	Operation	tRC	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	68	-	70	-	70	-	ns	
/RAS to /CAS Delay		tRCD	20	-	20	-	20	-	ns	
/RAS Active Time		tRAS	48	100K	50	100K	50	100K	ns	
/RAS Precharge Time		tRP	20	-	20	-	20	-	ns	
/RAS to /RAS Bank Active Delay		tRRD	16	-	20	-	20	-	ns	
/CAS to /CAS Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	4	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	CL=3	tPROZ3	3	-	3	-	3	-	CLK	
	CL=2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note : 1. A new command can be given tRRC after self refresh exit.

MODULE OPERATING OPTION TABLE

HYM71V651601TH-8

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V651601TH-10P

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V651601TH-10S

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/ AP	BA	Note
Mode Register set		H	X	L	L	L	L	X	OP code			1
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All baknks		H	X	L	L	H	L	X	X	H	X	
Precharge selected bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge Power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note:
1. OP Code : Operand Code
2. V = Valid, X = Don't care, H = Logic High, L = Logic Low, RA = Row Address, CA = Column Address

PACKAGE DIMENSION