8Mx64 bit SDRAM SO DIMM X-Series

PC/100 SDRAM Specification Supporting
based on 8Mx16 SDRAM, LVTTL, 4-Banks & 4K-Refresh
HYM71V65M801

PPRELIMINARY

DESCRIPTION

The HYM71V65M801 X-Series are high speed 3.3-Volt Synchronous DRAM Modules composed of four 8Mx16 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E^2PROM on a 144-pin Zig Zag Dual pin glass-epoxy printed circuit board. Three 0.1uF decoupling capacitors per each SDRAM are mounted on the module.

The HYM71V65M801 X-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 64M bytes memory. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- 1.00"(25.40mm) PCB Height
- One Row of SDRAMs on SO DIMM
- 144-Pin Unbuffered SO DIMM
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms
- All inputs and outputs referenced to positive edge of system clock
- Internal four banks operation
- Programmable Burst Length and Burst Type
  - 1,2,4,8 and Full page for Sequential Burst
  - 1,2,4 and 8 for Interleave Burst
- Programmable /CAS latency ; 2,3 clocks
- Data mask function by DQM

ORDERING INFORMATION

Part No.	Clock Frequency	Power	PCB Height	Package	Based Comp. Part No
HYM71V65M801TX-8	125MHz	Normal	1.00"	TSOPII	HY57V1291620TC-8
HYM71V65M801TX-10P	100MHz				HY57V1291620TC-10P
HYM71V65M801TX-10S	100MHz				HY57V1291620TC-10S
HYM71V65M801LTX-8	125MHz	Low Power			HY57V1291620LTC-8
HYM71V65M801LTX-10P	100MHz				HY57V1291620LTC-10P
HYM71V65M801LTX-10S	100MHz				HY57V1291620LTC-10S

PIN DESCRIPTION

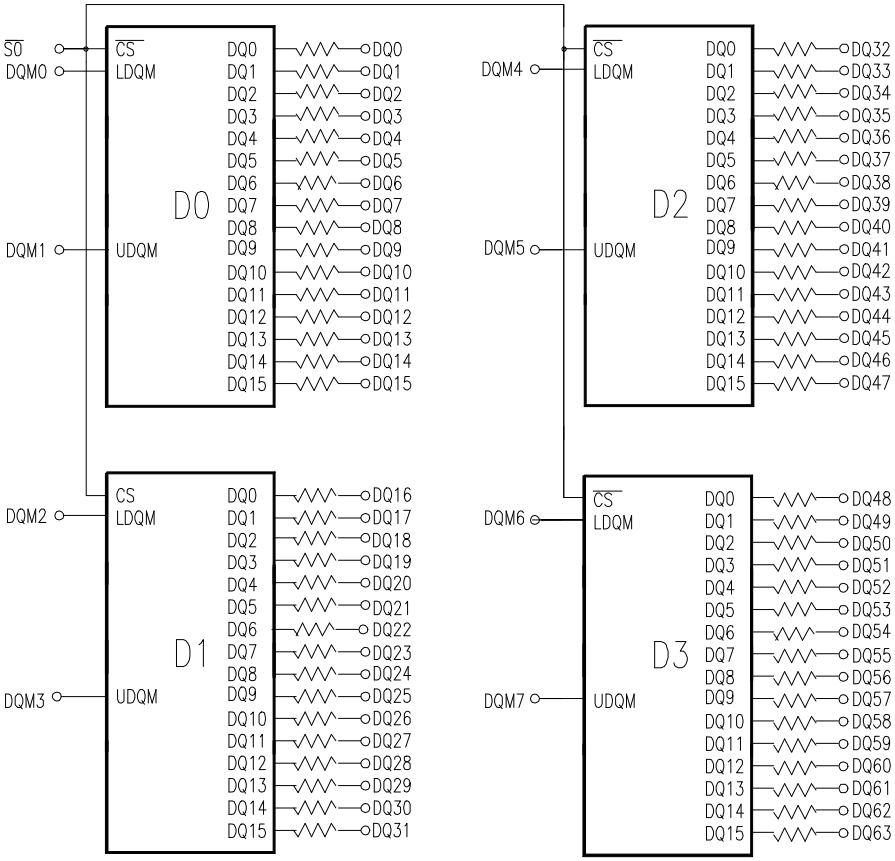
Pin	Pin Name	Description
CK0, CK1	Clock	The system clock input; All other inputs are registered to the SDRAM on the rising edge of CLK. CK1 is not used in this module.
CKE0	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0	Chip Select	Command input enable of mask except CLK, CKE and DQM
/RAS, /CAS,/WE	Row Address Strobe, Column Address Strobe, Write Enable	/RAS, /CAS and /WE define the operation. Refer function truth table for details
DQM0-7	Data Input / Output Mask	DQM control output buffer in read mode and masks input data in write mode
DQ0-DQ63	Data Input / Output	Multiplexed data input / output pin
BA0, BA1	Bank Address	Select either one of banks during both /RAS and /CAS activity
A0-A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA8 Auto-precharge flag: A10
Vcc/Vss	Power Supply/Ground	Power supply and ground for internal circuit and input buffer
SDA	Serial Address and Data Input / Output.	Serial Address and Data Input / Output for EEPROM
SCL	Serial Clock	Serial Clock
SA0-SA2	INPUT	Addresses in Serial E^2PROM for Socket Presence.
WP	Write Protection	EEPROM Write Protection

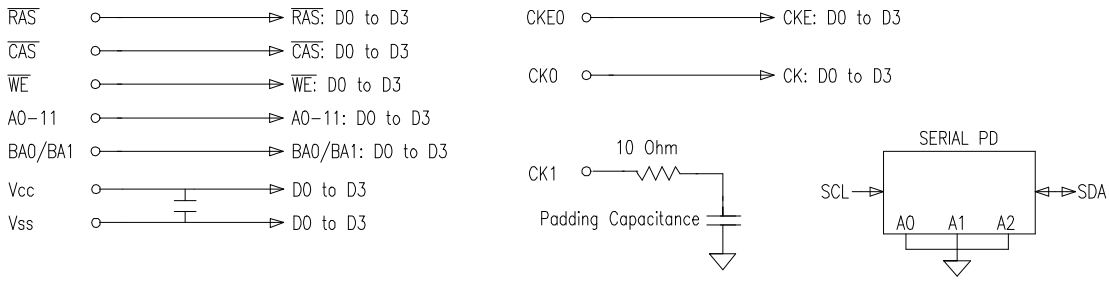
PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	2	Vss	73	NC	74	*CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10(AP)	112	A11
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	Vcc	46	Vcc	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	Vcc	130	Vcc
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	/RAS	66	/CAS	137	DQ31	138	DQ63
67	/WE	68	NC	139	Vss	140	Vss
69	/S0	70	NC	141	SDA	142	SCL
71	NC	72	NC	143	Vcc	144	Vcc

Note : * CK1 is connected with termination R/C. (Refer to the Block Diagram.)

BLOCK DIAGRAM





Note : 1. The padding capacitance of termination R/C for CK1 is 10pF.

2. Three 0.1uF decoupling capacitors per SDRAM device.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION			VALUE			NOTE
		-8	-10P	-10S	-8	-10P	-10S	
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes			80h			
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes			08h			
BYTE2	Fundamental Memory Type	SDRAM			04h			
BYTE3	# of Row Addresses on This Assembly	12			0Ch			1
BYTE4	# of Column Addresses on This Assembly	9			09h			
BYTE5	# of Module Banks on This Assembly	1 Banks			01h			
BYTE6	Data Width of This Assembly	64 Bits			40h			
BYTE7	Data Width of This Assembly (Continued)	-			00h			
BYTE8	Voltage Interface Standard of This Assembly	LVTTL			01h			
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	8ns	10ns	10ns	80h	A0h	A0h	
BYTE10	Access Time from Clock @ /CAS Latency=3	6ns	6ns	6ns	60h	60h	60h	
BYTE11	DIMM Configuration Type	None			00h			
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported			80h			
BYTE13	Primary SDRAM Width	X16			10h			
BYTE14	Error Checking SDRAM Width	None			00h			
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency			01h			
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page			8Fh			2
BYTE17	# of Banks on SDRAM Device	4 Banks			04h			
BYTE18	CAS # Latency	/CAS Latency=2,3			06h			
BYTE19	CS # Latency	/CS Latency=0			01h			
BYTE20	Write Latency	/WE Latency=0			01h			
BYTE21	SDRAM Module Attributes	Neither Buffered nor Registered			00h			
BYTE22	SDRAM Module Attributes, General	+/-10% voltage tolerance, Burst read, Single bit write, Precharge all, Auto precharge, Early /RAS precharge			0Eh			
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	12ns	10ns	12ns	C0h	A0h	C0h	
BYTE24	Access Time from Clock @ /CAS Latency=2	6ns	6ns	6ns	60h	60h	60h	
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE26	Access Time from Clock @ /CAS Latency=1	-	-	-	00h	00h	00h	
BYTE27	Minimum Row Precharge Time (tRP)	20ns	20ns	20ns	14h	14h	14h	
BYTE28	Minimum Row Active to Row Active Delay (tRRD)	16ns	20ns	20ns	10h	14h	14h	
BYTE29	Minimum /RAS to /CAS Delay (tRCD)	20ns	20ns	20ns	14h	14h	14h	
BYTE30	Minimum /RAS Pulse width (tRAS)	48ns	50ns	50ns	30h	32h	32h	
BYTE31	Module Bank Density	64MB			10h			
BYTE32	Command & Address signal input setup time (tAS)	2ns	2ns	2ns	20h	20h	20h	
BYTE33	Command & Address signal input hold time (tAH)	1ns	1ns	1ns	10h	10h	10h	
BYTE34	Data signal input setup time (tDS)	2ns	2ns	2ns	20h	20h	20h	
BYTE35	Data signal input hold time (tDH)	1ns	1ns	1ns	10h	10h	10h	
BYTE36 - 61	Superset Information(May be used in the future)	-			00h			
BYTE62	SPD Revision	Intel SPD 1.2A			12h			4, 5
BYTE63	Checksum for Byte 0-62	-	-	-	07h	0Dh	2Dh	
BYTE64	Manufacturer JEDEC ID Code	Hyundai JEDEC ID			ADh			
BYTE65 - 71	Manufacturer JEDEC ID Code	Unused			FFh			
BYTE72	Manufacturing Location	HEI (Korea) HEA (United States) HEU (Europe)			01h 02h 03h			

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION			VALUE			NOTE
		-8	-10P	-10S	-8	-10P	-10S	
BYTE73-90	Manufacturer' s Part Number (SDRAM) except ' HYM'	-			-			6
BYTE73	Manufacturer' s Part Number(SDRAM)	7			37h			6
BYTE74	Manufacturer' s Part Number(128M bit based)	1			31h			6
BYTE75	Manufacturer' s Part Number(3.3V)	V			56h			6
BYTE76	Manufacturer' s Part Number(Data Width)	6			36h			6
BYTE77	Manufacturer' s Part Number(Data Width)	5			35h			6
BYTE78	Manufacturer' s Part Number(Module Type)	M			4Dh			6
BYTE79	Manufacturer' s Part Number(Memory Depth)	8			38h			6
BYTE80	Manufacturer' s Part Number(Refresh)	0(4K Ref.)			30h			6
BYTE81	Manufacturer' s Part Number(4 Internal Bank)	1			31h			6
BYTE82	Manufacturer' s Part Number(TSOPII Mounted)	T			54h			6
BYTE83	Manufacturer' s Part Number(x4 Registered)	X			58h			6
BYTE84	Manufacturer' s Part Number(Hyphen)	'-'			2Dh			6
BYTE85	Manufacturer' s Part Number(Min. Cycle Time)	8	1	1	38h	31h	31h	6
BYTE86	Manufacturer' s Part Number(Min. Cycle Time)	Blank	0	0	20h	30h	30h	6
BYTE87	Manufacturer' s Part Number(Min. Cycle Time)	Blank	P	S	20h	50h	53h	6
BYTE88-90	Manufacturer' s Part Number	Blanks			20h			6
BYTE91	Revision Code for Components	Process Code			-			3, 6
BYTE92	Revision Code for PCB	Process Code			-			3, 6
BYTE93	Manufacturing Date	Work Week			-			3, 5
BYTE94	Manufacturing Date	Year			-			3, 5
BYTE95 - 98	Assembly Serial Number	-			-			3
BYTE99 - 125	Manufacturer Specific Data (May be used in the Future)	None			00h			
BYTE126	System Frequency support	100MHz			64h			4
BYTE127	Intel Specification details for 100MHz Support	Note 7			87h	87h	85h	
BYTE128 -256	Unused storage locations	-			00h			4

Note: 1. The bank address is excluded.
2. In interleaved type, the burst lengths supported is 1, 2, 4, 8.
3. Not fixed but dependent.
4. Refer to Intel SPD 1.2A specifications.
5. BCD adopted.
6. ASCII adopted.
7. CLK0 connected to the DIMM, TBD junction temp, CL=2(3) support and supporting .
8. In case of L-part , character ' L' will be added between byte 81 and byte 82.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	4	W
Soldering Temperature · Time	T_{SOLDER}	260·10	°C · Sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

DC OPERATING CONDITIONS (T_A=0°C to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	1
Input High Voltage	V_{IH}	2.0	3.0	V_{CC} + 0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.3	0	0.8	V	1, 3

Note :
1. All voltages are referenced to Vss=0V
2. V_{IH}(max) is acceptable 5.6V AC pulse width with <= 3ns of duration.
3. V_{IL}(min) is acceptable –2.0V AC pulse width with <= 3ns of duration.

AC OPERATING CONDITIONS (T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High/Low Level Voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise/Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

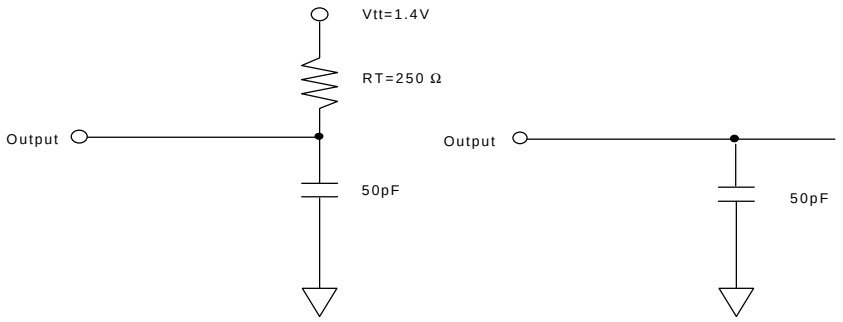
Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor(50pF).
For details, refer to AC/DC output load circuit.

CAPACITANCE

(T_A=25°C, f=1MHz)

Parameter	Pin	Symbol	Typ.	Max.	Unit
Input Capacitance	A0-A11/12, BA0/BA1	C_{IN1}	-	45	pF
Input Capacitance	/RAS, /CAS, /WE	C_{IN2}	-	45	pF
Input Capacitance	/S0	C_{IN3}	-	40	pF
Input Capacitance	CK0	C_{IN4}	-	45	pF
Input Capacitance	CKE0	C_{IN5}		40	pF
Input Capacitance	DQM0-DQM7	C_{IN6}	-	15	pF
Output Capacitance	DQ0-DQ63	C_{OUT}	-	15	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS (I)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Min.	Max.	Unit	Note
Input Leakage Current	I_{LI}	-4	4	μA	1
Output Leakage Current	I_{LO}	-1	1	μA	2
Output High Voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output Low Voltage	V_{OL}	-	0.4	V	I_{OL} = +4mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not under test = 0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6V

DC CHARACTERISTICS(II)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Parameter	Symbol	Test Condition		Speed			Unit	note
				-8	-10P	-10S		
Operating Current	ICC1	Burst Length=1, One bank active tRAS≥tRAS(min), tRP≥tRP(min), I_{OL}=0mA		480	480	480	mA	1
Precharge Standby Current in power down mode	ICC2P	CKE≤V_{IL}(max),tCK=min		8			mA	
	ICC2PS	CKE≤V_{IL}(max),tCK=∞		6				
Precharge Standby Current in non power down mode	ICC2N	CKE≥V_{IH}(min), /CS≥V_{IH}(min),tCK=min Input signals are changed one time during 2Clks. All other pins≥V_{DD}-0.2V or ≤0.2V		80			mA	
	ICC2NS	CKE≥V_{IH}(mim),tCK=∞ Input signals are stable		40				
Active Standby Current in power down mode	ICC3P	CKE≤V_{IL}(max),tCK=min		28			mA	
	ICC3PS	CKE≤V_{IL}(max),tCK=∞		28				
Active Standby Current in non power down mode	ICC3N	CKE≥V_{IH}(min), /CS≥V_{IH}(min),tCK=min Input signals are changed one time during 2CLKs. All other pins≥V_{DD}-0.2V or ≤0.2V		160			mA	
	ICC3NS	CKE≥V_{IH}(mim),tCK=∞ Input signals are stable		160				
Burst Mode Operating Current	ICC4	tCK≥tCK(min), Continuous burst,I_{OL}=0mA All banks active	CL=3	560	480	480	mA	1
			CL=2	480	480	440		
Auto Refresh Current	ICC5	tRRC≥tRRC(min), all banks active		1080			mA	2
Self Refresh Current	ICC6	CKE≤0.2V		8			mA	3
				3.2			mA	4

Note :

ICC1 and ICC4 depend on output loading and cycle rates. Specified values are measured with the output open.

Minimum of tRRC (Refresh /RAS cycle time) is listed on AC characteristic II.

HYM71V65M801TX-8/10P/10S

HYM71V65M801LTX-8/10P/10S

AC CHARACTERISTICS I

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
System Clock Cycle Time	CL=3	tCK3	8	1000	10	1000	10	1000	ns	
	CL=2	tCK2	12		10		12		ns	
Clock High Pulse Width		tCHW	3	-	3	-	3	-	ns	1
Clock Low Pulse Width		tCLW	3	-	3	-	3	-	ns	1
Access Time From Clock	CL=3	tAC3	-	6	-	6	-	6	ns	2
	CL=2	tAC2	-	6	-	6	-	6	ns	
Data-Out Hold Time		tOH	3	-	3	-	3	-	ns	
Data-Input Setup Time		tDS	2	-	2	-	2	-	ns	1
Data-Input Hold Time		tDH	1	-	1	-	1	-	ns	1
Address Setup Time		tAS	2	-	2	-	2	-	ns	1
Address Hold Time		tAH	1	-	1	-	1	-	ns	1
CKE Setup Time		tCKS	2	-	2	-	2	-	ns	1
CKE Hold Time		tCKH	1	-	1	-	1	-	ns	1
Command Setup Time		tCS	2	-	2	-	2	-	ns	1
Command Hold Time		tCH	1	-	1	-	1	-	ns	1
CLK to Data Output in Low Z-Time		tOLZ	1	-	1	-	1	-	ns	
CLK to Data Output in High Z-Time	CL=3	tOHZ3	3	6	3	6	3	6	ns	
	CL=2	tOHZ2	3	6	3	6	3	6	ns	

Note : 1. Assumed tR / tF(input rise and fall time) is 1ns.
2. Access times to be measured with input signals of 1V/ ns edge rate, 0.8V to 2.0V

AC CHARACTERISTICS II

Parameter		Symbol	-8		-10P		-10S		Unit	Note
			Min	Max	Min	Max	Min	Max		
/RAS cycle time	Operation	tRC	68	-	70	-	70	-	ns	
	Auto Refresh	tRRC	68	-	70	-	70	-	ns	
/RAS to /CAS Delay		tRCD	20	-	20	-	20	-	ns	
/RAS Active Time		tRAS	48	100K	50	100K	50	100K	ns	
/RAS Precharge Time		tRP	20	-	20	-	20	-	ns	
/RAS to /RAS Bank Active Delay		tRRD	16	-	20	-	20	-	ns	
/CAS to /CAS Delay		tCCD	1	-	1	-	1	-	CLK	
Write Command to Data-In Delay		tWTL	0	-	0	-	0	-	CLK	
Data-In to Precharge Command		tDPL	1	-	1	-	1	-	CLK	
Data-In to Active Command		tDAL	4	-	3	-	3	-	CLK	
DQM to Data-Out Hi-Z		tDQZ	2	-	2	-	2	-	CLK	
DQM to Data-In Mask		tDQM	0	-	0	-	0	-	CLK	
MRS to New Command		tMRD	2	-	2	-	2	-	CLK	
Precharge to Data Output Hi-Z	CL=3	tPROZ3	3	-	3	-	3	-	CLK	
	CL=2	tPROZ2	2	-	2	-	2	-	CLK	
Power Down Exit Time		tPDE	1	-	1	-	1	-	CLK	
Self Refresh Exit Time		tSRE	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	ms	

Note : 1. A new command can be given tRRC after self refresh exit.

MODULE OPERATING OPTION TABLE

HYM71V65M801TX -8

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
125MHz	3CLKs	3CLKs	6CLKs	9CLKs	3CLKs	6ns	3ns
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V65M801TX -10P

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

HYM71V65M801TX -10S

	/CAS Latency	tRCD	tRAS	tRC	tRP	tAC	tOH
100MHz	3CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
83MHz	2CLKs	2CLKs	5CLKs	7CLKs	2CLKs	6ns	3ns
66MHz	2CLKs	2CLKs	4CLKs	6CLKs	2CLKs	6ns	3ns

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/ AP	BA	Note
Mode Register set		H	X	L	L	L	L	X	OP code			1
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All baknks		H	X	L	L	H	L	X	X	H	X	
Precharge selected bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Self Refresh	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge Power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X	X			

Note:
1. OP Code : Operand Code
2. V = Valid, X = Don't care, H = Logic High, L = Logic Low, RA = Row Address, CA = Column Address

PACKAGE DIMENSION