HYM5V72A400A N-Series

4Mx72-bit CMOS DRAM MODULE

DESCRIPTION

The HYM5V72A400A is a 4M x 72-bit Fast page mode CMOS DRAM module consisting of eighteen HY51V16400A in 24/28 pin SOJ or TSOPII and two 16-bit BiCMOS line driver in TSSOP on a 168 pin glass-epoxy printed circuit board. 0.22§ þdecoupling are mounted for each DRAM. The HYM5V72A400ATNG/SLTNG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 32M byte memory.

FEATURES

- Low power dissipation
  Max. self-refresh 20.09mW (SL-part)
  Max. battery back-up 39.53mW (SL-part)
  Max. CMOS standby 13.61mW (SL-part)
  33.05mW
  Max. TTL standby 65.45mW
  Max. operating

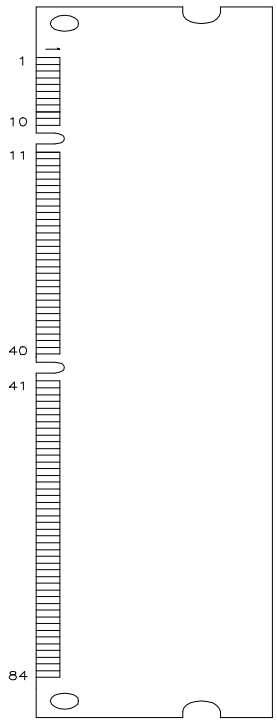
Speed	Power
60	5.87W
70	5.22W
80	4.57W

- Single power supply of 3.3V±10%
- TTL compatible inputs and outputs
- Fast access time

Speed	t_{RAC}	t_{CAC}	t_{HPC}
60	60ns	20ns	40ns
70	70ns	23ns	45ns
80	80ns	25ns	50ns

- EDO mode operation
- /CAS-before-/RAS, /RAS-only, Hidden refresh, Self-refresh
- 4096 refresh cycles / 256ms (SL-part)
  4096 refresh cycles / 64ms
- Buffered inputs (except /RAS and DQ)
- 4 Byte interleave enabled, Dual address inputs (A0,B0)

PIN CONNECTION



PIN CONNECTION

/RAS0, /RAS2	Row Address Strobe
/CAS0, /CAS4	Column Address Strobe
/WE0, /WE2	Write Enable
/OE0, /OE2	Output Enable
A0-A11, B0	Address Input
DQ0-DQ71	Data Input/Output
PD1-PD8	Presence Detect
/PDE	Presence Detect Enable
ID0,ID1	ID Bit
V_{CC}	Power (+ 3.3V)
V_{SS}	Ground

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	/OE2	86	DQ36	128	NC
3	DQ1	45	/RAS2	87	DQ37	129	NC
4	DQ2	46	/CAS4	88	DQ38	130	NC
5	DQ3	47	NC	89	DQ39	131	NC
6	Vcc	48	/WE2	90	Vcc	132	/PDE
7	DQ4	49	Vcc	91	DQ40	133	Vcc
8	DQ5	50	NC	92	DQ41	134	NC
9	DQ6	51	NC	93	DQ42	135	NC
10	DQ7	52	DQ18	94	DQ43	136	DQ54
11	SQ8	53	DQ19	95	DQ44	137	DQ55
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ20	97	DQ45	139	DQ56
14	DQ10	56	DQ21	98	DQ46	140	DQ57
15	DQ11	57	DQ22	99	DQ47	141	DQ58
16	DQ12	58	DQ23	100	DQ48	142	DQ59
17	DQ13	59	Vcc	101	DQ49	143	Vcc
18	Vcc	60	DQ24	102	Vcc	144	DQ60
19	DQ14	61	NC	103	DQ50	145	NC
20	DQ15	62	NC	104	DQ51	146	NC
21	DQ16	63	NC	105	DQ52	147	NC
22	DQ17	64	NC	106	DQ53	148	NC
23	Vss	65	DQ25	107	Vss	149	DQ61
24	NC	66	DQ26	108	NC	150	DQ62
25	NC	67	DQ27	109	NC	151	DQ63
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE0	69	DQ28	111	NC	153	DQ64
28	/CAS0	70	DQ29	112	NC	154	DQ65
29	NC	71	DQ30	113	NC	155	DQ56
30	/RAS0	72	DQ31	114	NC	156	DQ67
31	/OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ32	116	Vss	158	DQ68
33	A0	75	DQ33	117	A1	159	DQ69
32	A2	76	DQ34	118	A3	160	DQ70
34	A4	77	DQ35	119	A5	161	DQ71
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	PD1	121	A9	163	PD2
38	A10	80	PD3	122	A11	164	PD4
39	NC	81	PD5	123	NC	165	PD6
40	Vcc	82	PD7	124	Vcc	166	PD8
41	NC	83	ID0(Vss)	125	NC	167	ID1
42	NC	84	Vcc	126	B0	168	Vcc

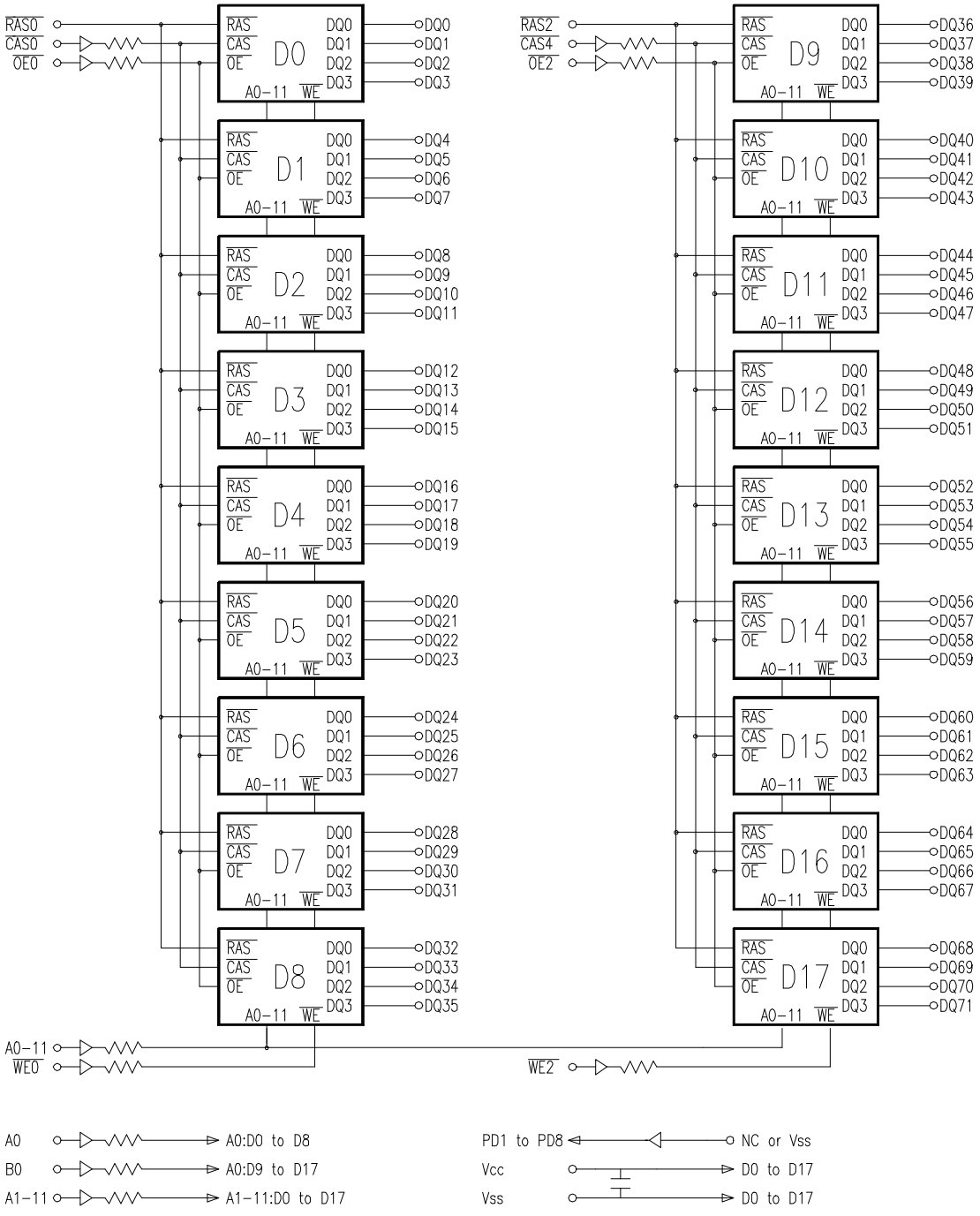
PRESENCE DETECT PINS

PIN	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	ID0	ID1
-60	NC	NC	Vss	NC	Vss	NC	NC	Vss	Vss	NC or Vss
-70	NC	NC	Vss	NC	Vss	Vss	NC	Vss	Vss	NC or Vss
-80	NC	NC	Vss	NC	Vss	NC	Vss	Vss	Vss	NC or Vss

NOTE :

1. PDs are either open NC or driven to Vss via on-board buffer circuits.
2. IDs are connected directly to NC or Vss without a buffer.
3. ID1 will be either open NC for Self-Refresh or driven to Vss for standard.

BLOCK DIAGRAM



NOTE : All resistors are 25 Ohm±5%

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	¡ É
T_{STG}	Storage Temperature	-55 to 125	¡ É
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	20	mA
P_D	Power Dissipation	9.78	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0¡ Éto 70¡ É)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0¡ Éto 70¡ ÉVCC= 3.3V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	VSS¡ ÎVIN¡ ÎVCC+1.0, other pins not under test=VSS	All but /RAS	-10	10	¥ ÌA	
			/RAS	-90	90		
ILO	Output Leakage Current (High impedance State)	VSS¡ ÎVOUT¡ Îvcc /RAS & /CAS at VIH		-10	10	¥ ÌA	
ICC1	VCC Supply Current Operating	tRC=tRC (min.)	60	-	1630	mA	1,2,3
			70	-	1450		
			80	-	1270		
ICC2	VCC Supply Current TTL Standby	/RAS & /CAS at VIH, other inputs ≥ VSS		-	18.18	mA	
				-			
ICC3	VCC Supply Current /RAS-only refresh	tRC=tRC(min.)	60	-	1630	mA	1,3
			70	-	1450		
			80	-	1270		
ICC4	VCC Supply Current, EDO mode	tHPC= tHPC (min.)	60	-	1270	mA	1,2,3
			70	-	1090		
			80	-	910		
ICC5	VCC Supply Current CMOS Standby	/RAS & /CAS ≥ VCC – 0.2V		-	9.18	mA	
			SL-part	-	3.78		5
ICC6	VCC Supply Current /CAS before /RAS refresh	tRC=tRC(min.)	60	-	1630	mA	1,3
			70	-	1450		
			80	-	1270		
ICC7	VCC Supply Current, Battery Back Up (SL-part only)	tRC= 62.5µs, /CAS = CBR cycling or 0.2V, /WE = VCC – 0.2V A0 - A11= VCC – 0.2V or 0.2V DQ0-DQ71=VCC-0.2V, 0.2V or open	tRAS ≤ 300ns	-	6.48	mA	1,4,5
			tRAS ≤ 1¥ ìs	-	10.98		
ICC8	VCC Supply Current Self Refresh (SL-part only)	/RAS & /CAS ≤ 0.2V /OE & /WE & A0-A11=VCC 0.2V or 0.2V DQ0-DQ71=VCC-0.2V, 0.2 or open		-	5.58	mA	5
VOL	Output Low Voltage	IOL= 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH= -2.0mA		2.4	-	V	

NOTE
1. ICC1, ICC3, ICC4,ICC6 and ICC7 depend on cycle rate.
2. output loading. Specified values are obtained with the ouptup open.
3. ICC is specified as average current. For ICC1,ICC3 and ICC6 address can be changed maximum two times while /RAS=VIL. For ICC4, address can be changed maximum once while /CAS=VIH.
4. Only tRAS(max.)=1µs is applied to refresh of battery backup but tRAS(max.)=10µs is applied to normal functional operation.
5. ICC5(max.)=3.78mA, ICC7 and ICC8 are applied to SL-part only (HYM5V72A400ASLTNG).

AC CHARACTERISTICS

(TA=0¡ ßto 70¡ ÉVCC= 3.3V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1,2,3

#	SYMBOL	PARAMTER	HYM5V72A400A N-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	100	-	130	-	150	-	ns	
2	tRWC	/RAS to /CAS Precharge Time	168	-	188	-	208	-	ns	14,15
3	tHPC	EDO Mode Cycle Time	40	-	45	-	50	-	ns	
4	tHPRWC	Time from /CAS Precharge	88	-	93	-	103	-	ns	13,15
5	tRAC	Access Time from /RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from /CAS	-	20	-	23	-	25	ns	4,9,15
7	tAA	Access Time from Coulmn Address	-	31	-	36	-	41	ns	4,10,15
8	tCPA	Access Time from /CAS Precharge	-	40	-	45	-	50	ns	4,15
9	tCLZ	/CAS to Output Low Impedance	2	-	2	-	2	-	ns	4,13
10	tCEZ	Output Buffer Turn-off Delay	0	18	0	20	0	20	ns	5,17
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3,12
12	tRP	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	tRSH	/RAS Hold Time	20	-	23	-	25	-	ns	15
16	tCSH	/CAS Hold Time	58	-	68	-	78	-	ns	14
17	tCAS	/RAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	/RAS to /CAS Delay	18	40	18	47	18	55	ns	9,16
19	tRAD	/RAS to Column Address Delay Time	13	24	13	29	15	34	ns	10,16
20	tCRP	/CAS to RAS Precharge Time	15	-	15	-	15	-	ns	15
21	tCP	/CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	6	-	6	-	6	-	ns	15
23	tRAH	Row Address Hold Time	8	-	8	-	8	-	ns	14
24	tASC	Column Address Set-up Time	2	-	2	-	2	-	ns	13
25	tCAH	Column Address Hold Time	12	-	12	-	17	-	ns	13
26	tAR	Column Address Hold Time from /RAS	48	-	53	-	58	-	ns	14
27	tRAL	Column Address to /RAS Lead Time	36	-	41	-	46	-	ns	15
28	tRCS	Read Command Set-up Time	2	-	2	-	2	-	ns	13
29	tRCH	Read Command Hold Time Referenced to /CAS	2	-	2	-	2	-	ns	6,13
30	tRRH	Read Command Hold Time Referenced to /RAS	-2	-	-2	-	-2	-	ns	6,14
31	tWCH	Write Command Hold Time	12	-	12	-	17	-	ns	13
32	tWCR	Write Command Hold Time from /RAS	43	-	53	-	58	-	ns	14
33	tWP	Write Command Pulse Width	10	-	10	-	15	-	ns	
34	tRWL	Write Command to /RAS Lead Time	20	-	23	-	25	-	ns	15
35	tCWL	Write Command to /CAS Lead Time	17	-	20	-	22	-	ns	13
36	tDS	Data-In Set-up Time	-2	-	-2	-	-2	-	ns	7,14
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7,15
38	tDHR	Data-In Hold Time Referenced to /RAS	48	-	48	-	53	-	ns	14
39	tREF	Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	18
		SL-part	-	256	-	256	-	256	ms	
40	tWCS	Write Command Set-up Time	2	-	2	-	2	-	ns	8,13

AC CHARACTERISTICS

#	SYMBOL	PARAMTER	HYM5V72A400A N-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	t_{CWD}	/CAS to /WE Delay Time	43	-	48	-	50	-	ns	8,15
42	t_{RWD}	/RAS to /WE Delay Time	86	-	98	-	108	-	ns	8,14,15
43	t_{AWD}	Column Address to /WE Delay Time	62	-	69	-	74	-	ns	8,14,15
44	t_{CSR}	/CAS Set-up Time (CBR Cycle)	10	-	10	-	10	-	ns	15
45	t_{CHR}	/CAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	14
46	t_{RPC}	/RAS to /CAS Precharge Time	-2	-	-2	-	-2	-	ns	14
47	t_{CPT}	/RAS Precharge Time (CBR Counter Test)	20	-	25	-	25	-	ns	
48	t_{ROH}	/RAS Hold Time Reference to /OE	5	-	5	-	5	-	ns	15
49	t_{OEA}	/OE Access Time	0	20	0	23	0	25	ns	15
50	t_{OED}	/OE to Data Delay	20	-	20	-	20	-	ns	15
51	t_{OEZ}	Output Buffer Turn Off Delay Time from /OE	2	18	2	20	2	20	ns	5,17
52	t_{OEH}	/OE Command Hold Time	10	-	10	-	10	-	ns	
53	t_{CPWD}	/WE Delay Time from /CAS Precharge	43	-	48	-	53	-	ns	8,14,15
54	t_{RHCP}	/RAS Hold Time from /CAS Precharge	37	-	42	-	47	-	ns	13
55	t_{PD}	/PDE to Valid Presence Detect Data	-	10	-	10	-	10	ns	11
56	t_{PDOFF}	/PDE Inactve to Presence Detects Inactive	2	-	2	-	2	-	ns	12
57	t_{WRP}	/WE to /RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
58	t_{WRH}	/WE to /RAS Hold Time (CBR Cycle)	8	-	8	-	8	-	ns	
59	t_{RASS}	/RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	ns	
60	t_{RPS}	/RAS Precharge Time (Self Refresh Cycle)	90	-	110	-	130	-	ns	
61	t_{CHS}	/CAS Hold Time (Self Refresh Cycle)	-50	-	-50	-	-50	-		

NOTE :

1. An initial pause of 200§ Ás required after power-up followed by 8 /RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 /CAS-before-/RAS intilization cycles instead of 8 /RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If /RAS= Vss during power-up, the HYM5V72A400A begin an active cycle. This conditionn results in higher power-up current than necessary demands from the power-up. It is recommended that /RAS and /CAS track with Vcc during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V16400A data sheet for detailed information.
4. Measured at V_{OH}=2.4V and V_{OL}=0.4V with a load equivalent to 1 TTL loads and 100pF.
5. t_{CEZ}(max.).t_{OEZ}(max.),t_{REZ}(max.) and t_{WEZ}(max.) define the time at which the output achiveds the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in late write or read-modify-write Cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) throught the entire cycle
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. t_{PDOFF}(max.) is determined by the pull-up resistor value. Care must be taken to ensure adequate recovery time prior to reading valid up-level on subsequent SIMM position.
13. A + 2ns timing skew from the DRAM tothe DIMM resulted from the addition of buffers (DRAM loading may add to skew).
14. A - 2ns timing skew from the DRAM tothe DIMM resulted from the addition of buffers (DRAM loading may add to skew).
15. A + 5ns (/CAS,/WE,/OE) or + 6ns (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
16. A - 2ns min and a - 5ns (/CAS,/WE,/OE) or - 6ns (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
17. A + 2ns min and a + 5ns (/CAS,/WE,/OE) or + 6ns (address) timing skew from the DRAM to the DIMM resulted from the addition of buffers. (DRAM loading may add skew).
18. A burst of 4096 /CAS-before-/RAS refresh cycles must bwe executed within 64ms after existing self refresh (for SL-part).

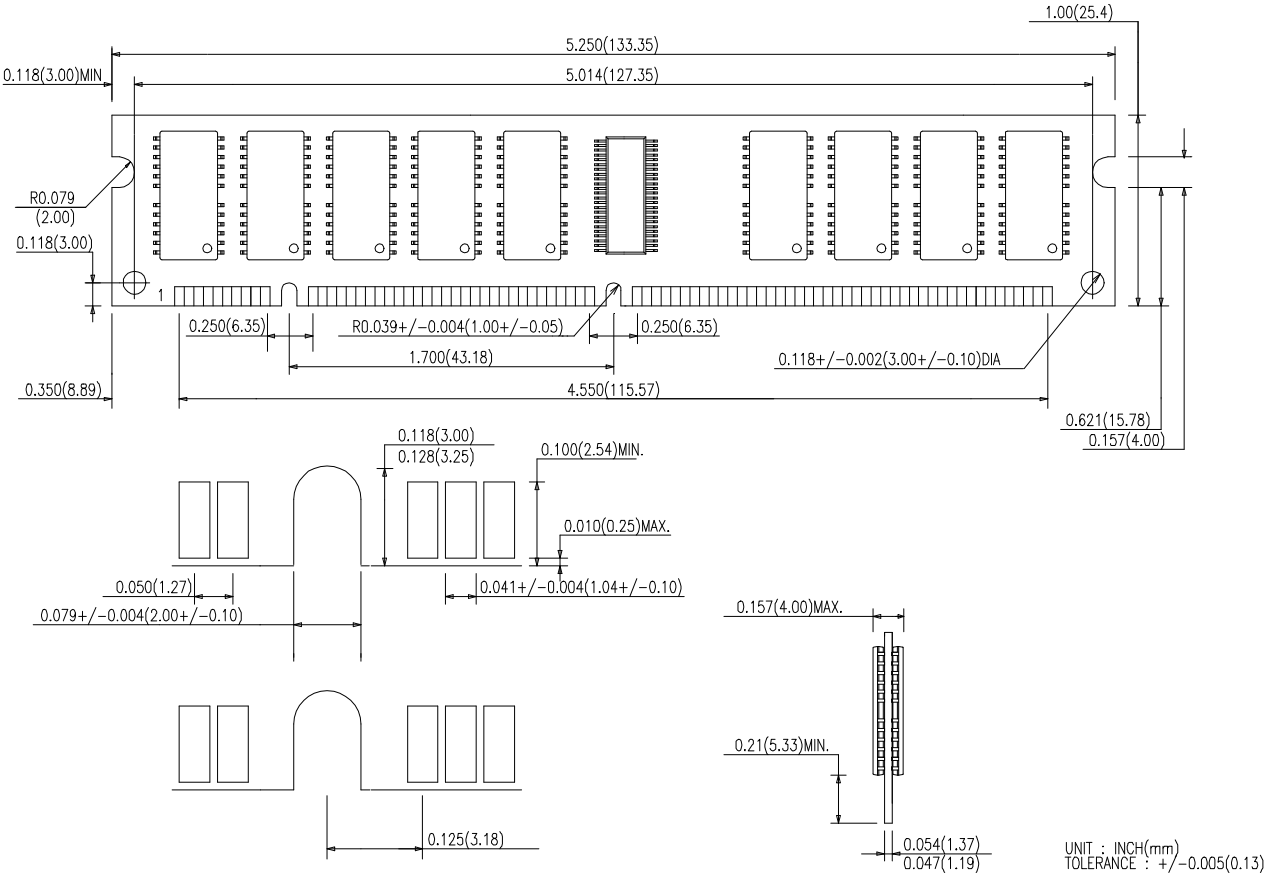
CAPACITANCE

(TA=25¡ ÉVcc= 3.3V± 10%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A11,B0)	-	13	pF
C_{IN2}	Input Capacitance (/RAS0, /RAS2)	-	70	pF
C_{IN3}	Input Capacitance (/CAS0, /CAS4, /WE0,/WE2,/OE0,/OE2)	-	13	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ71)	-	15	pF

PACKAGE DIMENSION

168pin Dual Inline Memory Module (TNG;TSOP Gold plated)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V72A400ATNG	60/70/80		DIMM	Gold
HYM5V72A400ASLTNG	60/70/80	SL-part	DIMM	Gold