

HAT1026R

Silicon P Channel Power MOS FET
High Speed Power Switching

HITACHI

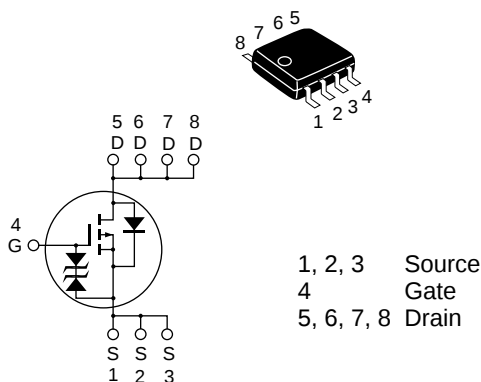
ADE-208-457 H (Z)
9th. Edition
February 1999

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	− 30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	− 7	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	− 56	A
Body–drain diode reverse drain current	I_{DR}	− 7	A
Channel dissipation	P_{ch} ^{Note2}	2.5	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	− 55 to + 150	°C

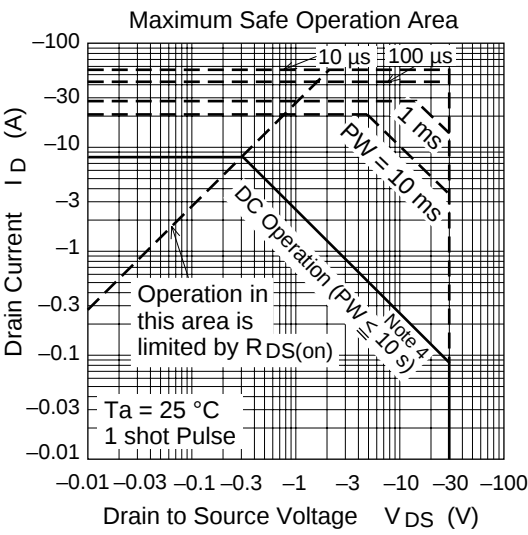
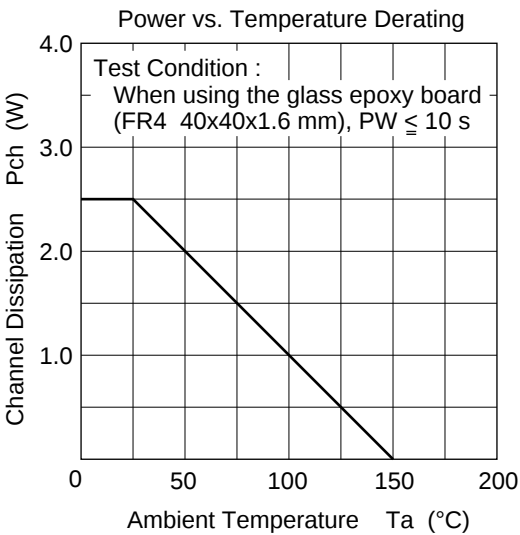
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics (Ta = 25°C)

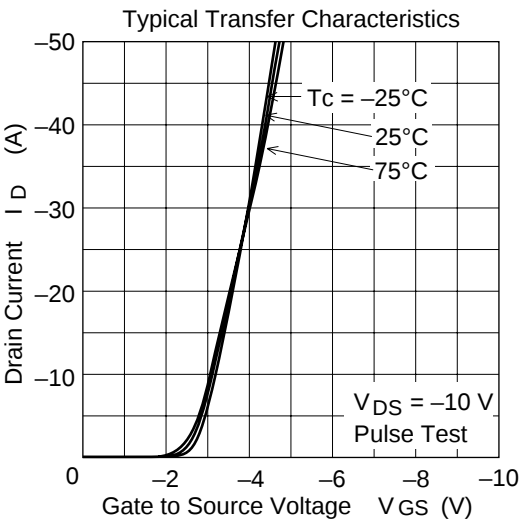
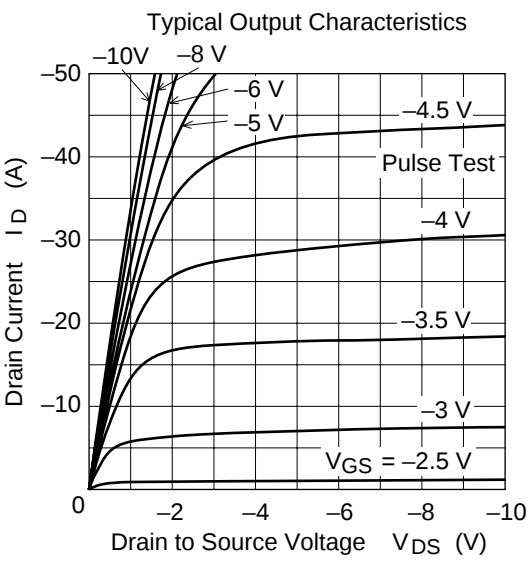
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	− 30	—	—	V	$I_D = -10\text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\text{ }\mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	− 10	μA	$V_{DS} = -30\text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	− 1.0	—	− 2.5	V	$V_{DS} = -10\text{ V}$, $I_D = -1\text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.028	0.037	Ω	$I_D = -4\text{ A}$, $V_{GS} = -10\text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	0.04	0.065	Ω	$I_D = -4\text{ A}$, $V_{GS} = -4\text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	8	12	—	S	$I_D = -4\text{ A}$, $V_{DS} = -10\text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	1700	—	pF	$V_{DS} = -10\text{ V}$
Output capacitance	C_{oss}	—	1000	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	190	—	pF	$f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	60	—	ns	$V_{GS} = -4\text{ V}$, $I_D = -4\text{ A}$
Rise time	t_r	—	330	—	ns	$V_{DD} \cong -10\text{ V}$
Turn-off delay time	$t_{d(off)}$	—	80	—	ns	
Fall time	t_f	—	120	—	ns	
Body–drain diode forward voltage	V_{DF}	—	− 0.9	− 1.4	V	$I_F = -7\text{ A}$, $V_{GS} = 0$ ^{Note3}
Body–drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -7\text{ A}$, $V_{GS} = 0$ $diF/dt = 20\text{ A}/\mu s$

Note: 3. Pulse test

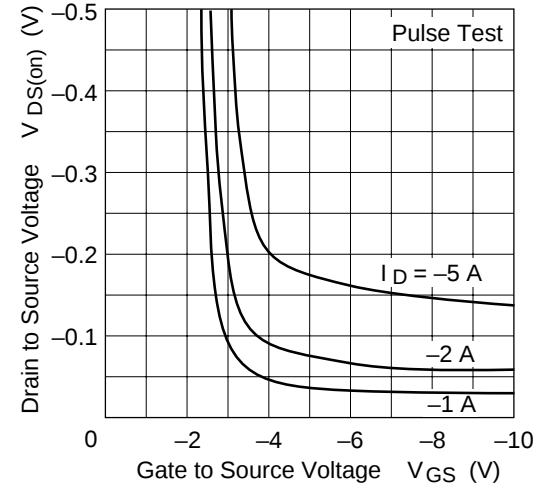
Main Characteristics



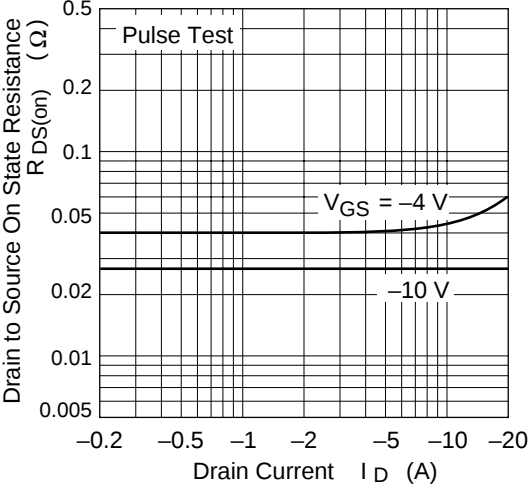
Note 4 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)



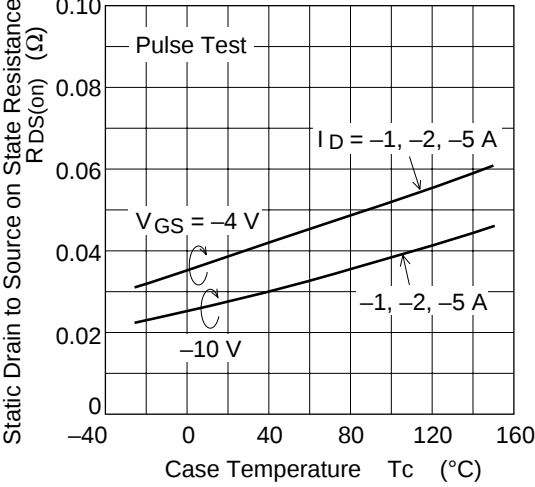
Drain to Source Saturation Voltage vs. Gate to Source Voltage



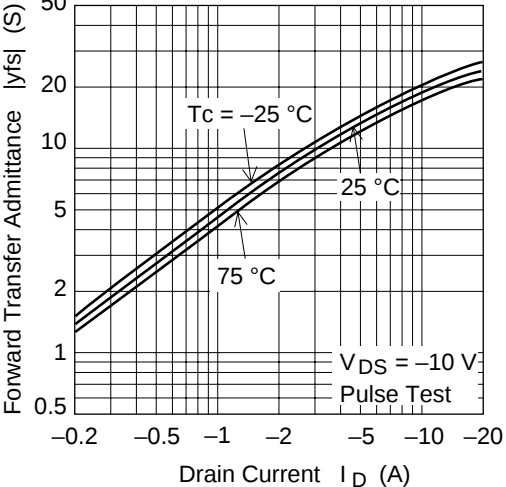
Static Drain to Source on State Resistance vs. Drain Current



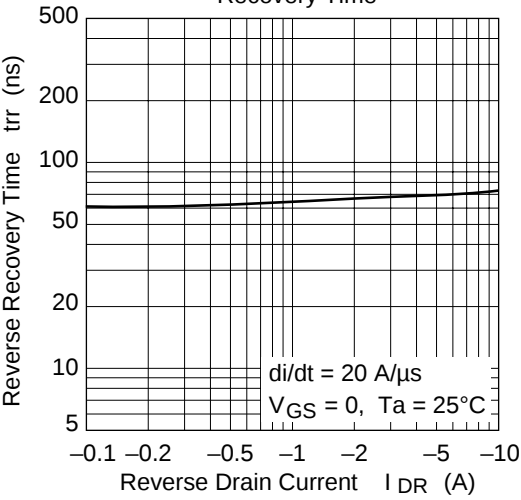
Static Drain to Source on State Resistance vs. Temperature



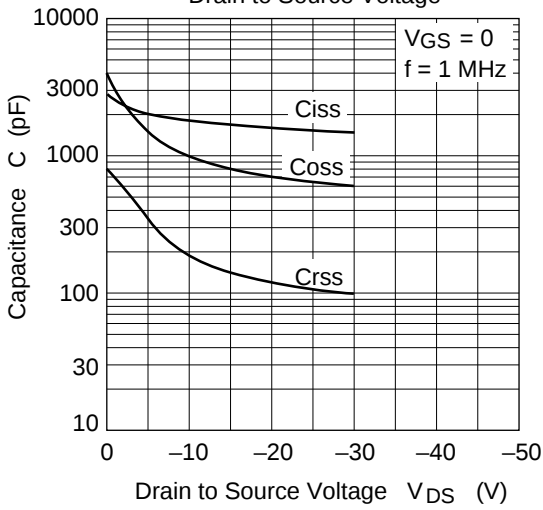
Forward Transfer Admittance vs. Drain Current



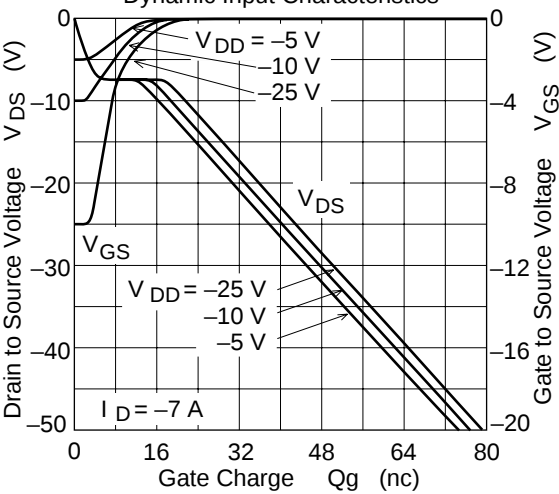
Body-Drain Diode Reverse Recovery Time



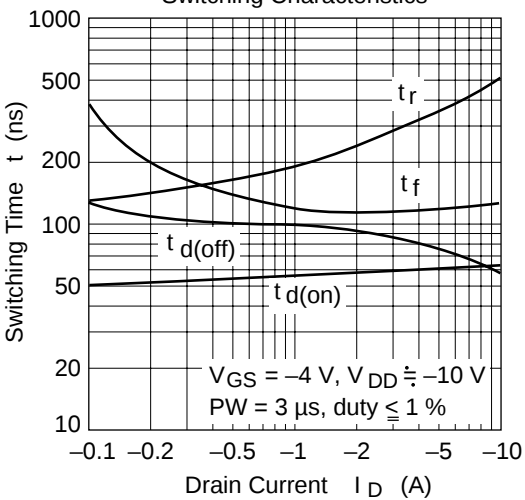
Typical Capacitance vs. Drain to Source Voltage

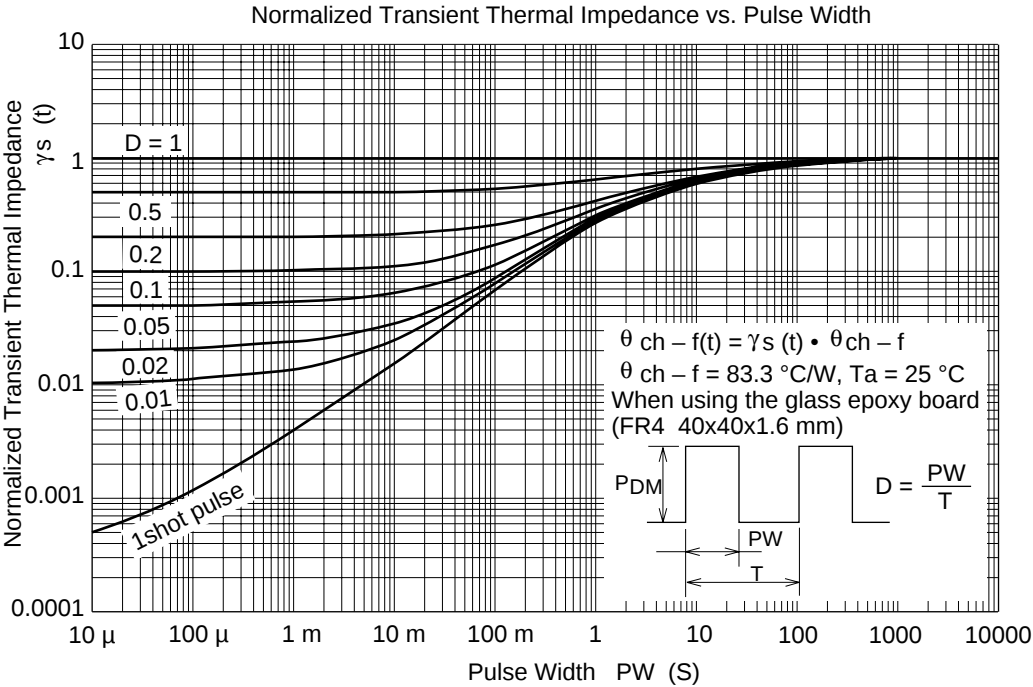
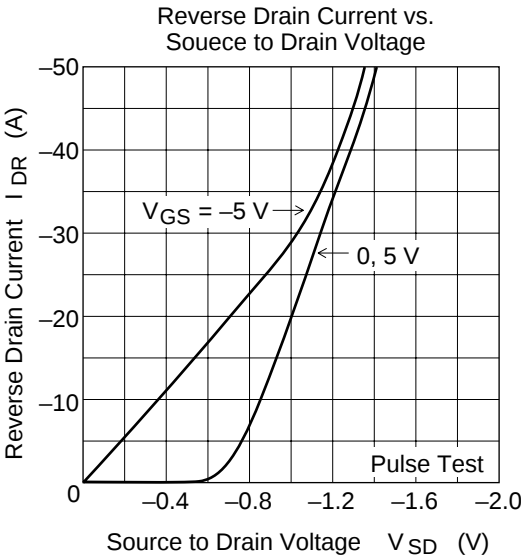


Dynamic Input Characteristics

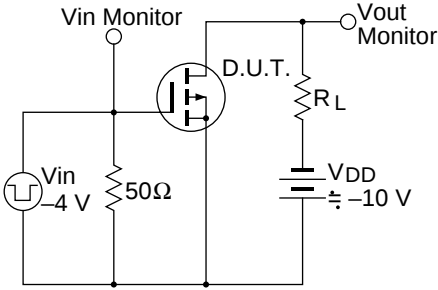


Switching Characteristics

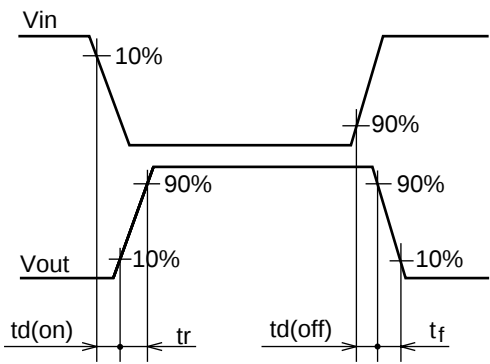




Switching Time Test Circuit

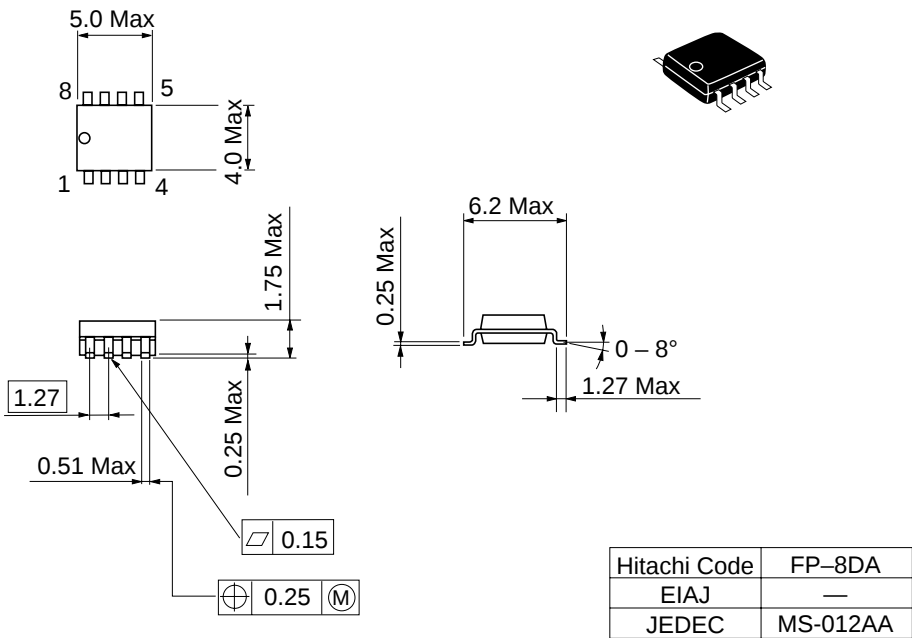


Switching Time Waveform



Package Dimensions

Unit: mm



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