

HD74HC4024

7-stage Binary Counter

HITACHI

ADE-205-533 (Z)
1st. Edition
Sep. 2000

Description

The HD74HC4024 is a 7-stage counter. This device is incremented on the falling edge (negative transition) of the input clock, and all its output is reset to a low level by applying a logical high on its reset input.

Features

- High Speed Operation: t_{pd} (Clock to Q_1) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

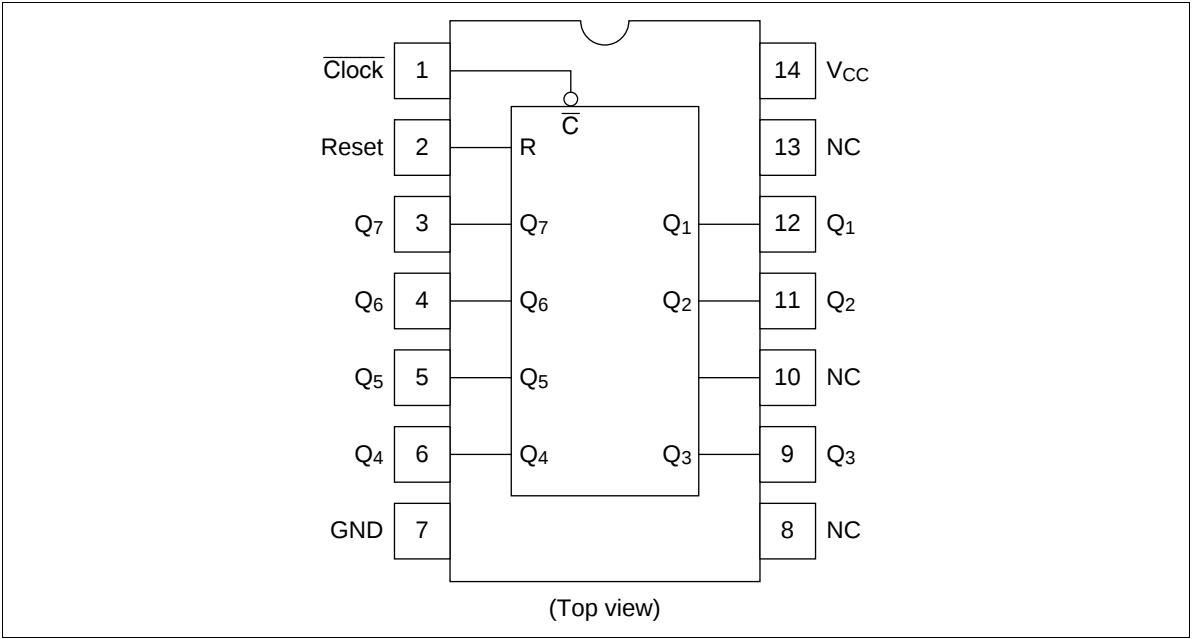
Function Table

Clock	Reset	Outputs State
L	L	No change
L	H	All outputs are low
H	L	No change
H	H	All outputs are low
	L	No change
	H	All outputs are low
	L	Advance to next state
	H	All outputs are low

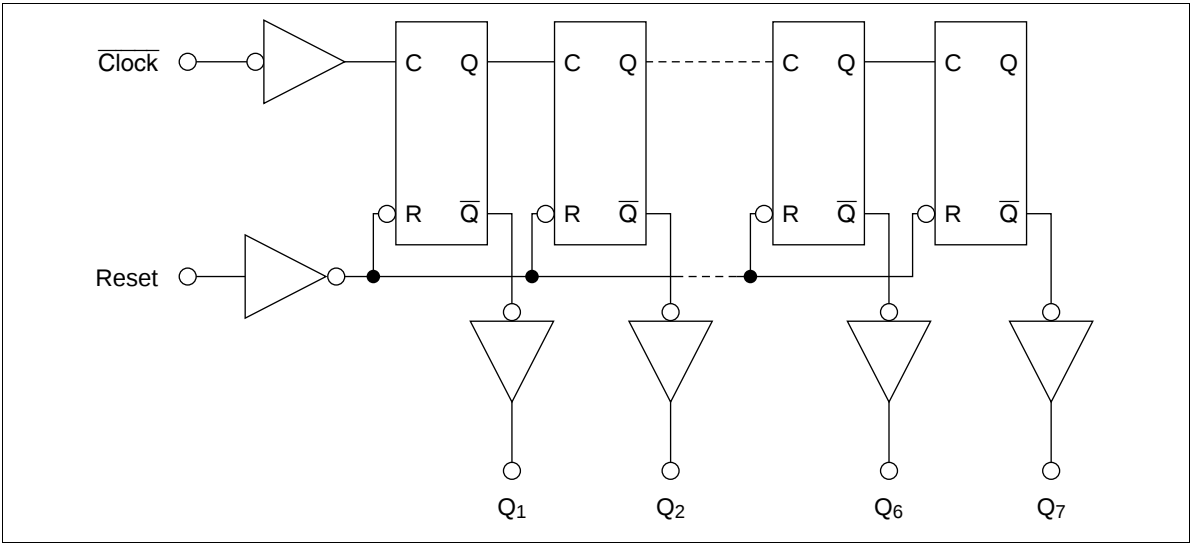


HD74HC4024

Pin Arrangement



Block Diagram



DC Characteristics

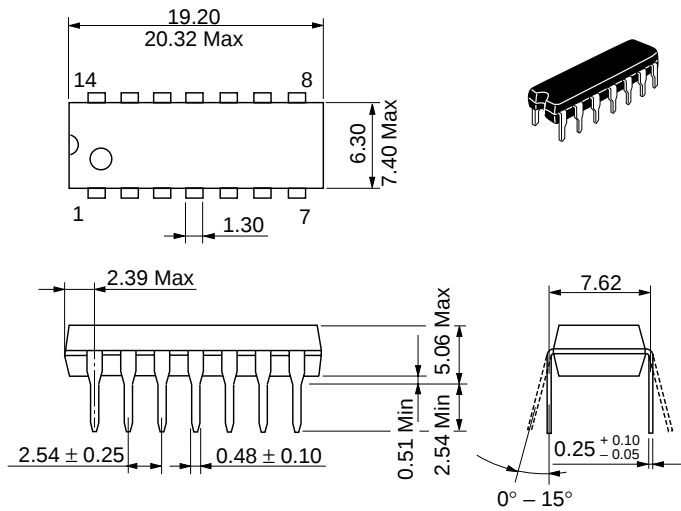
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = −40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = −20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = −4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = −5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t _{PLH}	2.0	—	—	185	—	230	ns	Clock to Q ₁
		4.5	—	14	37	—	46		
		6.0	—	—	31	—	39		
	t _{PHL}	2.0	—	—	185	—	230	ns	Clock to Q ₁
		4.5	—	14	37	—	46		
		6.0	—	—	31	—	39		
	t _{PHL}	2.0	—	—	185	—	230	ns	Reset to output
		4.5	—	13	37	—	46		
		6.0	—	—	31	—	39		
Removal time	t _{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	0	—	25	—		
		6.0	17	—	—	21	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	
		4.5	16	4	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns	
	t _{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

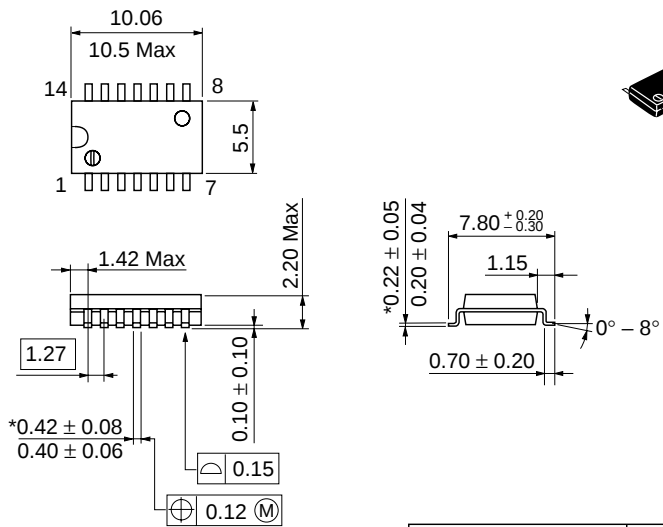
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

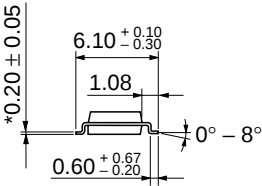
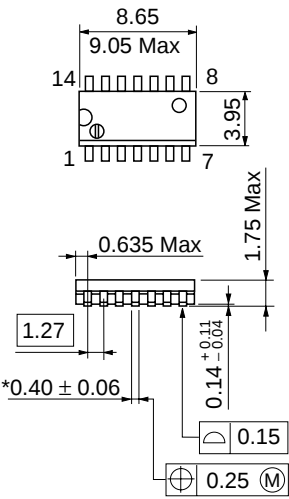
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

Unit: mm



*Pd plating

Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

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