HD74HC173

4-bit D-type Register (with 3-state outputs)

HITACHI

ADE-205-459 (Z)
1st. Edition
Sep. 2000

Description

The four D type Flip-Flops operate synchronously from a common clock. The 3-state outputs allow the device to be used in bus organized systems. The outputs are placed in the 3-stage mode when either of the output disable pins are in the logic high level.

The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic high level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Clearing is enabled by taking the clear input to a logic high level. The data outputs change state on the positive going edge of the clock.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

Function Table

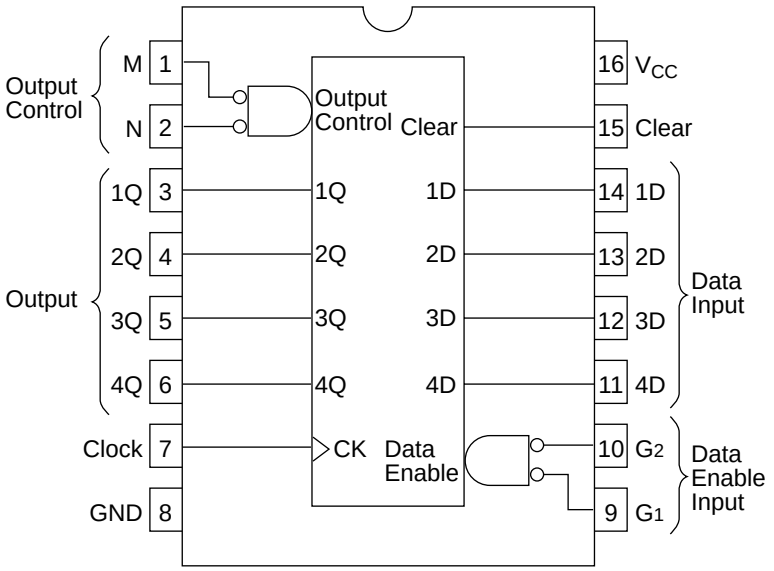
Inputs

		Data Enable			
Clear	**Clock**	**G_1**	**G_2**	**Data D**	**Output Q**
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	⎍	H	X	X	Q_0
L	⎍	X	H	X	Q_0
L	⎍	L	L	L	L
L	⎍	L	L	H	H

Note: When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

Hitachi semiconductor

Pin Arrangement

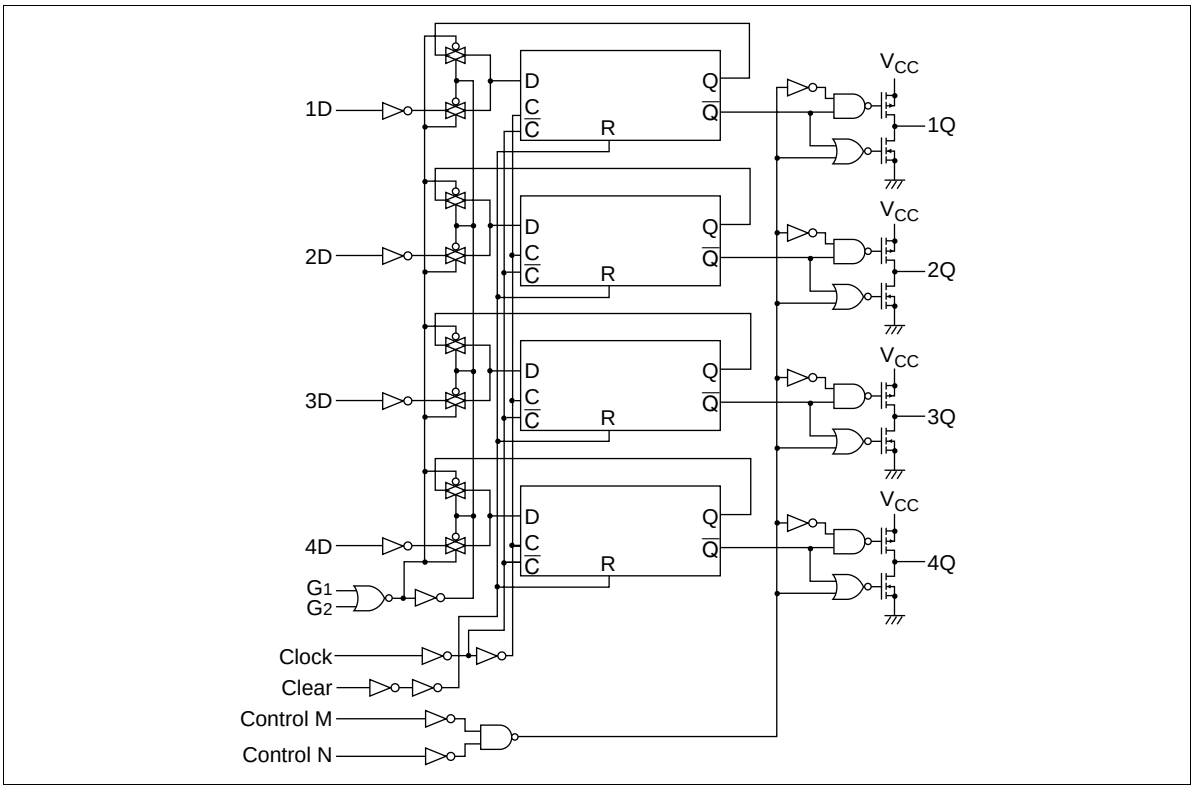


(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V
DC current drain per pin	I_{OUT}	±35	mA
DC current drain per VCC, GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Block Diagram



DC Characteristics

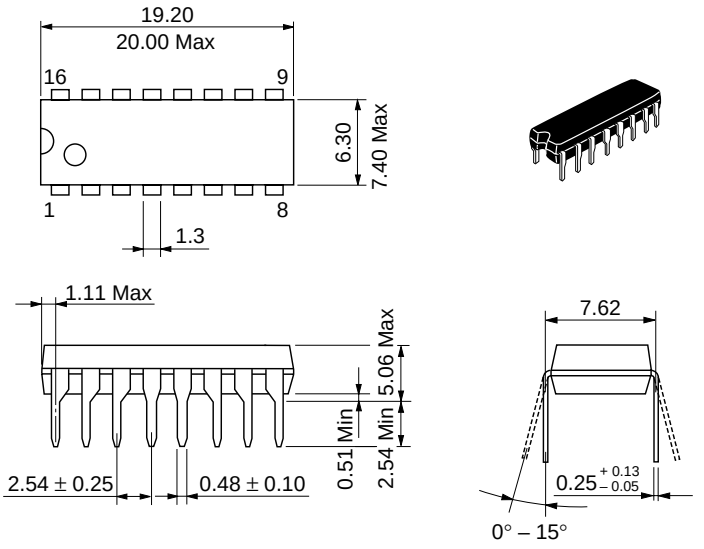
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 7.8 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	175	—	220	ns	Clock to Q
	t_{PHL}	4.5	—	14	35	—	44		
		6.0	—	—	30	—	37		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	4	—	25	—		
		6.0	17	–	—	21	—		
Removal time	t_{rem}	2.0	90	—	—	115	—	ns	
		4.5	18	0	—	23	—		
		6.0	15	—	—	20	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	–2	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	4	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	Cin	—	—	5	10	—	10	pF	

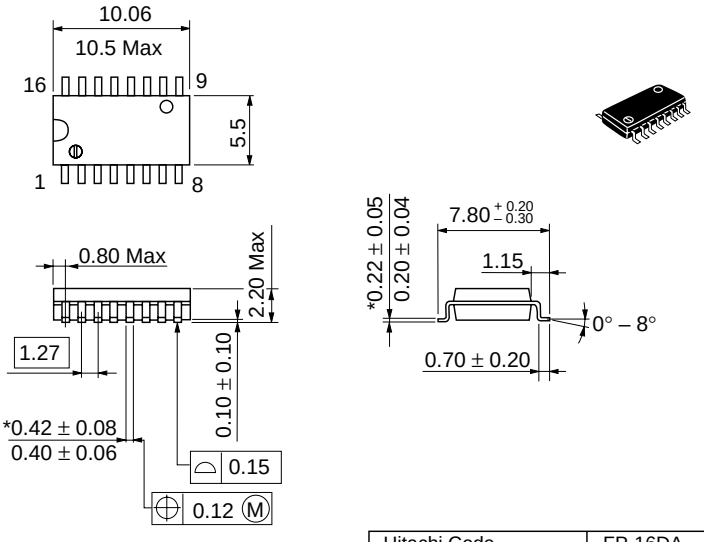
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

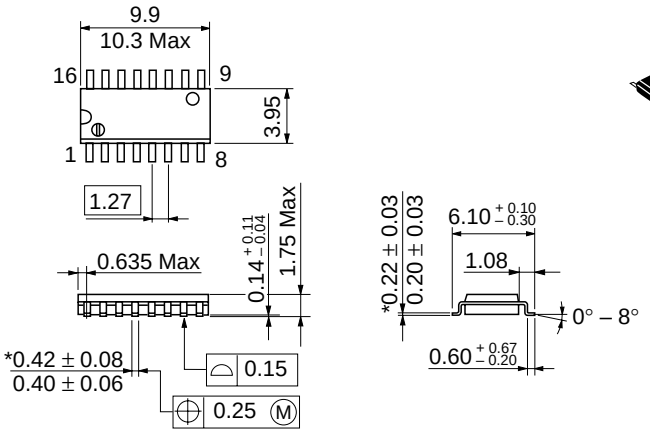
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http://semiconductor.hitachi.com/
Europe : http://www.hitachi-eu.com/hel/ecg
Asia : http://sicapac.hitachi-asia.com
Japan : http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic Components Group
Dornacher Straβe 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 585160

Hitachi Asia Ltd.
Hitachi Tower
16 Collyer Quay #20-00,
Singapore 049318
Tel : <65>-538-6533/538-8577
Fax : <65>-538-6933/538-3877
URL : http://www.hitachi.com.sg

Hitachi Asia Ltd.
(Taipei Branch Office)
4/F, No. 167, Tun Hwa North Road,
Hung-Kuo Building,
Taipei (105), Taiwan
Tel : <886>-(2)-2718-3666
Fax : <886>-(2)-2718-8180
Telex : 23222 HAS-TP
URL : http://www.hitachi.com.tw

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower,
World Finance Centre,
Harbour City, Canton Road
Tsim Sha Tsui, Kowloon,
Hong Kong
Tel : <852>-(2)-735-9218
Fax : <852>-(2)-730-0281
URL : http://www.hitachi.com.hk

Colophon 2.0