HD74AC175

Quad D-Type Flip-Flop

HITACHI

ADE-205-377 (Z)
1st. Edition
Sep. 2000

Description

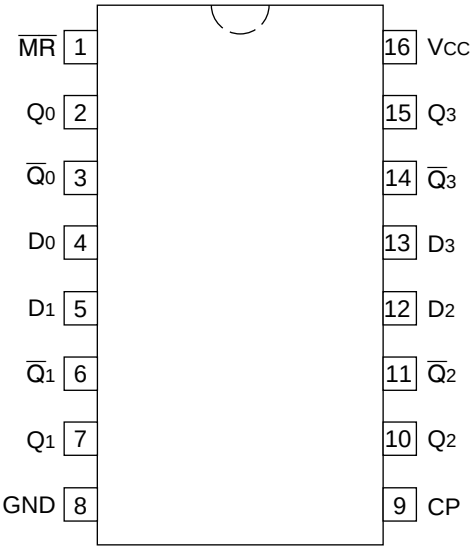
The HD74AC175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the Low-to-High clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when Low.

Features

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Outputs Source/Sink 24 mA

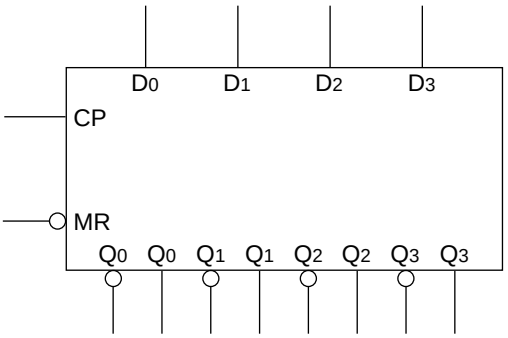
Hitachi semiconductor

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

D_0 to D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0 to Q_3	True Outputs
$\overline{Q}_0$ to $\overline{Q}_3$	Complement Outputs

Functional Description

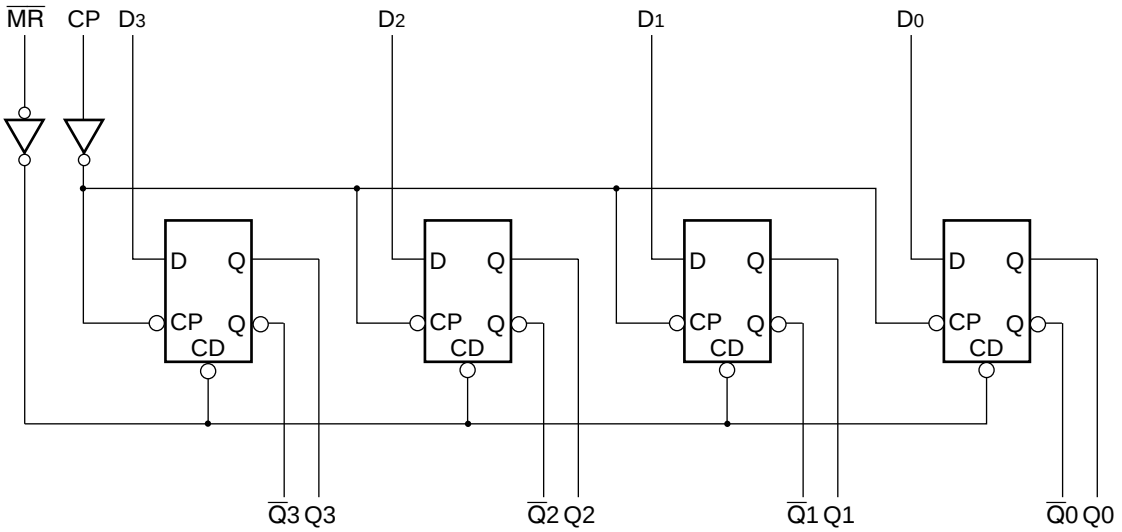
The HD74AC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the Low-to-High clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A Low input on the Master Reset ($\overline{MR}$) will force all Q outputs Low and $\overline{Q}$ outputs High independent of Clock or Data inputs. The HD74AC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	**Outputs**	
@ t_n, $\overline{MR}$ = H	**@ t_{n+1}**	
Dn	Qn	$\overline{Q}$n
L	L	H
H	H	L

H : High Voltage Level
L : Low Voltage Level
t_n : Bit Time before Clock Pulse
t_{n+1}: Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C

AC Characteristics

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Maximum clock	f_{max}	3.3	149	—	—	139	—	MHz
frequency		5.0	187	—	—	187	—	
Propagation delay	t_{PLH}	3.3	1.0	9.5	12.0	1.0	13.5	ns
CP to Q_n or $\overline{Q}_n$		5.0	1.0	7.0	9.0	1.0	9.5	
Propagation delay	t_{PHL}	3.3	1.0	8.5	13.0	1.0	14.5	ns
CP to Q_n or $\overline{Q}_n$		5.0	1.0	6.0	9.5	1.0	10.5	
Propagation delay	t_{PLH}	3.3	1.0	7.5	12.5	1.0	13.5	ns
$\overline{MR}$ to $\overline{Q}_n$		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay	t_{PHL}	3.3	1.0	8.5	11.0	1.0	12.5	ns
$\overline{MR}$ to Q_n		5.0	1.0	6.0	8.5	1.0	9.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF	Ta = –40°C to +85°C C_L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW	t_{su}	3.3	2.0	4.5	4.5	ns
D_n to CP		5.0	1.0	3.0	3.0	
Hold time, HIGH or LOW	t_h	3.3	0	1.0	1.0	ns
D_n to CP		5.0	0	1.0	1.0	
CP pulse width HIGH or LOW	t_w	3.3	2.5	4.5	4.5	ns
		5.0	2.0	3.5	3.5	
$\overline{MR}$ pulse width, LOW	t_w	3.3	2.5	4.5	5.0	ns
		5.0	2.0	3.5	3.5	
Recovery time $\overline{MR}$ to CP	t_{rec}	3.3	–2.0	0.0	0.0	ns
		5.0	–1.0	0.0	0.0	

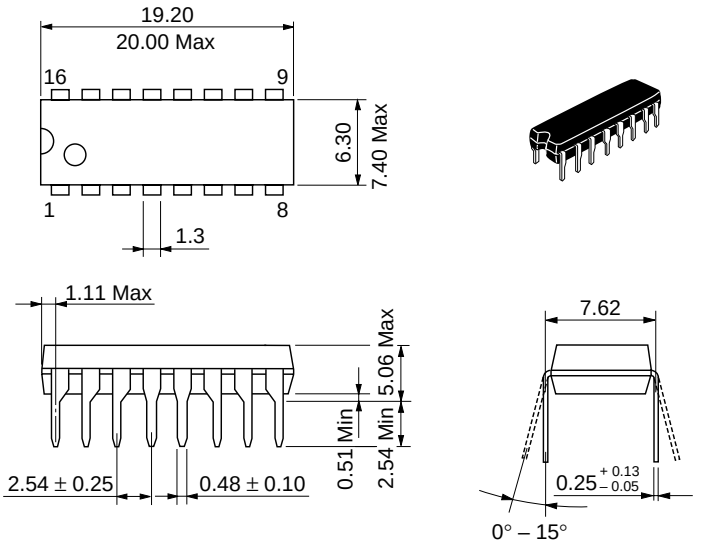
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	45.0	pF	V_{CC} = 5.0 V

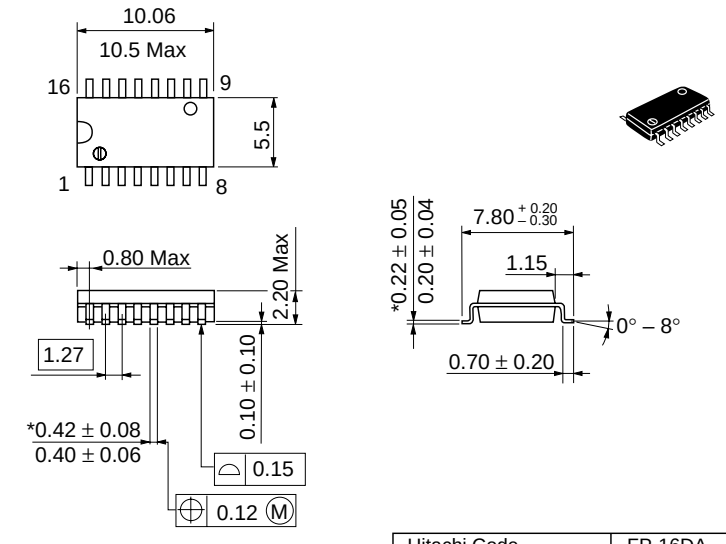
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

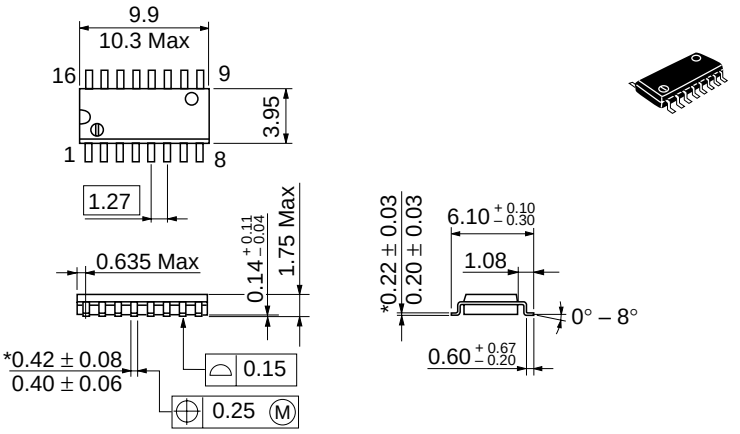
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

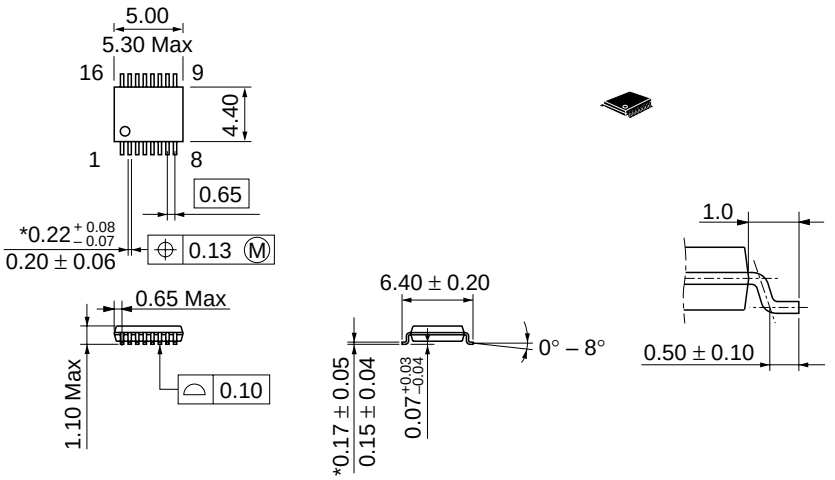
Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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