

HD74AC164/HD74ACT164

Serial-In, Parallel-Out Shift Register

HITACHI

ADE-205-373 (Z)
1st. Edition
Sep. 2000

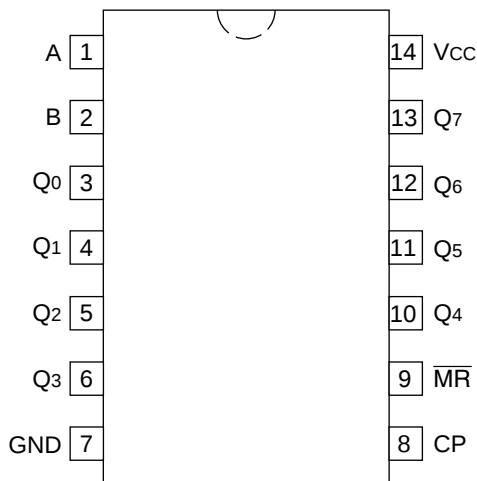
Description

The HD74AC164/HD74ACT164 is a high-speed 8-bit serial-in/parallel-out shift register. Serial data is entered through a 2-input AND gate synchronous with the Low-to-High transition of the clock. The device features an asynchronous Master Reset which clears the register, setting all outputs Low independent of the clock.

Features

- Outputs Source/Sink 24 mA
- HD74ACT164 has TTL-Compatible Inputs

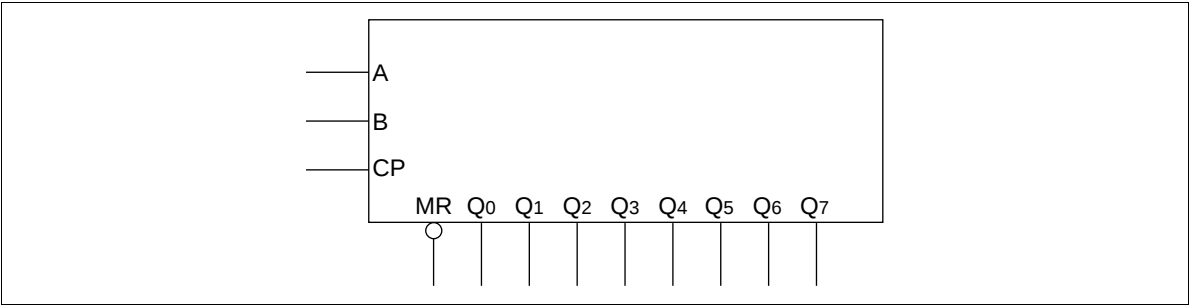
Pin Arrangement



(Top view)

HD74AC164/HD74ACT164

Logic Symbol



Pin Names

- A, B Data Inputs
- CP Clock Pulse Input (Active Rising Edge)
- $\overline{\text{MR}}$ Master Reset Input (Active Low)
- Q_0 to Q_7 Outputs

Functional Description

The HD74AC164/HD74ACT164 is an edge-triggered 8-bit shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (A or B); either of these inputs can be used as an active High Enable for data entry through the other inputs. An unused input must be tied High.

Each Low-to-High transition on the Clock (CP) input shifts data one place to the right and enters into Q_0 the logical AND of the two data inputs ($A \cdot B$) that existed before the rising clock edge. A Low level on the Master Reset ($\overline{\text{MR}}$) input overrides all other inputs and clears the register asynchronously, forcing all Q outputs Low.

Mode Select Table

Operating Mode	Inputs			Outputs	
	$\overline{MR}$	A	B	Q_0	Q_1 to Q_7
Reset (Clear)	L	X	X	L	L to L
Shift	H	L	L	L	q_0 to q_6
	H	L	H	L	q_0 to q_6
	H	H	L	L	q_0 to q_6
	H	H	H	H	q_0 to q_6

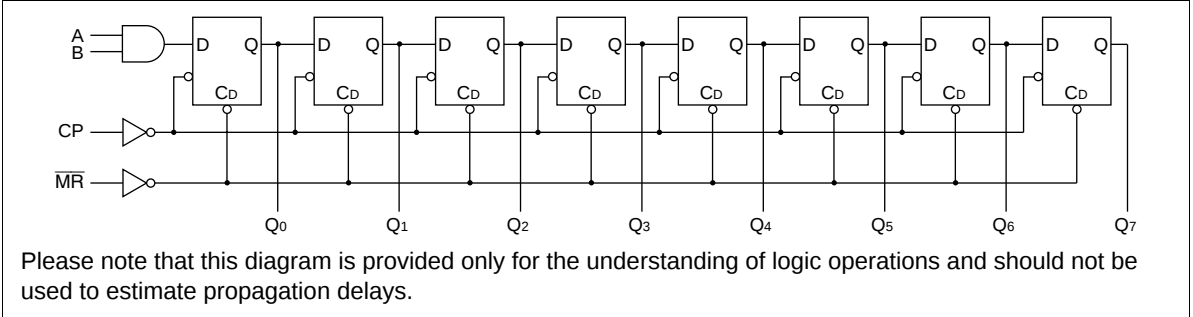
H : High Voltage Level

L : Low Voltage Level

X : Immaterial

q_n : Lower case letters indicate the state of the referenced input or output one setup time prior to the Low-to-High clock transition.

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^{\circ}C$
Maximum additional I_{CC}/input (HD74ACT164)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$

HD74AC164/HD74ACT164

AC Characteristics: HD74AC164

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	125	—	—	100	—	MHz
		5.0	150	—	—	125	—	
Propagation delay CP to Q _n	t _{PLH}	3.3	1.0	8.5	13.0	1.0	13.5	ns
		5.0	1.0	6.5	10.0	1.0	10.5	
Propagation delay CP to Q _n	t _{PHL}	3.3	1.0	8.5	13.0	1.0	14.5	
		5.0	1.0	6.5	10.0	1.0	10.5	
Propagation delay $\overline{\text{MR}}$ to Q _n	t _{PHL}	3.3	1.0	9.5	16.0	1.0	18.0	
		5.0	1.0	7.5	11.5	1.0	13.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC164

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF		Unit
			Typ	Guaranteed Minimum			
Setup time A or B to CP	t _{su}	3.3	3.0	5.5	6.0		ns
		5.0	2.0	4.6	4.5		
Hold time CP to A or B	t _h	3.3	−1.5	0.0	0.0		
		5.0	−1.5	0.0	0.0		
Pulse width CP or $\overline{\text{MR}}$	t _w	3.3	2.0	5.5	7.0		
		5.0	2.0	4.5	5.0		
Recovery time $\overline{\text{MR}}$ or CP	t _{rec}	3.3	0.0	2.0	2.0		
		5.0	0.0	2.0	2.0		

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT164

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF			Ta = -40°C to +85°C CL = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay CP to Q _n	t_{PLH}	5.0	1.0	9.0	11.5	1.0	12.5	ns
Propagation delay CP to Q _n	t_{PHL}	5.0	1.0	9.0	11.5	1.0	12.5	
Propagation delay MR to Q _n	t_{PHL}	5.0	1.0	9.5	13.0	1.0	14.5	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT164

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF		Ta = -40°C to +85°C CL = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time A or B to CP	t_{su}	5.0	2.5	7.0	8.0	ns
Hold time CP to A or B	t_h	5.0	0.0	1.5	1.5	
Pulse width CP or $\overline{MR}$	t_w	5.0	4.5	7.0	8.0	
Recovery time $\overline{MR}$ or CP	t_{rec}	5.0	0.0	2.0	2.0	

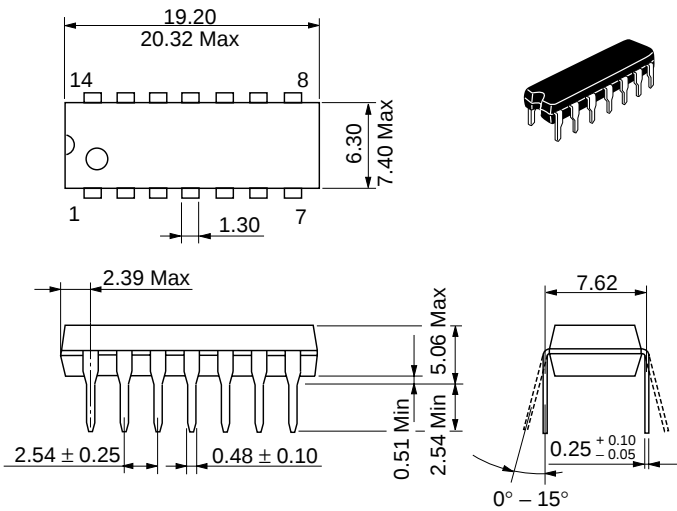
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5$ V
Power dissipation capacitance	C_{PD}	20.0	pF	$V_{CC} = 5.0$ V

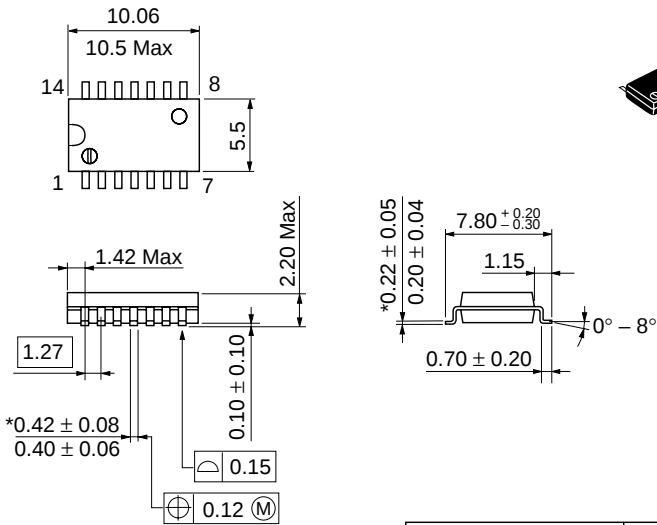
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

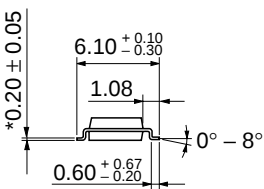
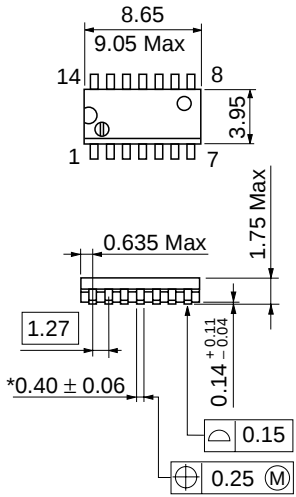
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

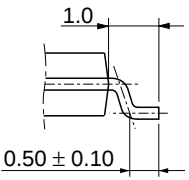
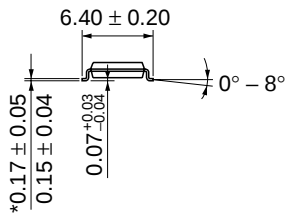
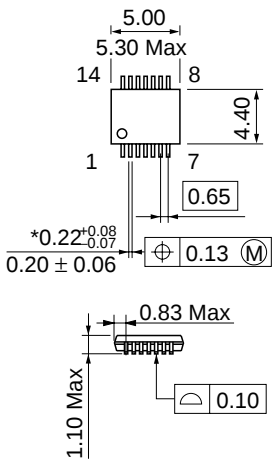
Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.13 g

*Pd plating

Unit: mm



Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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