HD74BC573A

Octal D Type Transparent Latches With 3 State Outputs

HITACHI

ADE-205-021A (Z)
2nd. Edition
Mar. 1993

Description

The HD74BC573A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range
  Ta = –40 to + 85°C

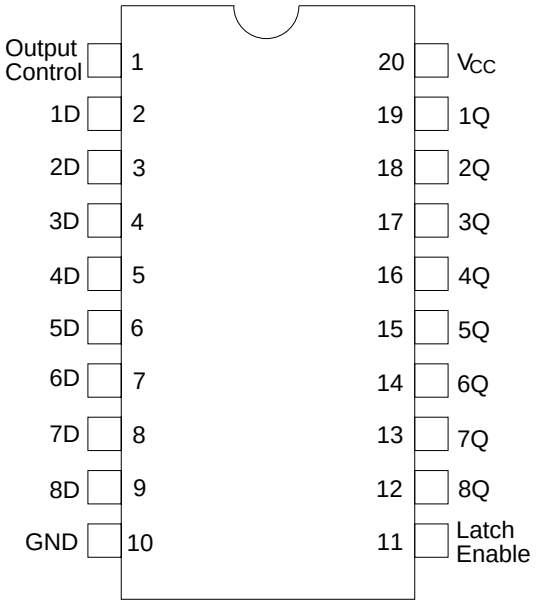
Function Table

Output Control	Latch Enable	Data	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H : High leve
L : Low level
X : Immaterial
Z : High impedance
Q_0 : Level of Q before the indicated steady input conditions were established

Hitachi semiconductor

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input diode current	I_{IK}	±30	mA
Input voltage	V_{IN}	–0.5 to +7.5	V
Output voltage	V_{OUT}	–0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	–0.5 to +5.5	V
Storage temperature	Tstg	–65 to +150	°C

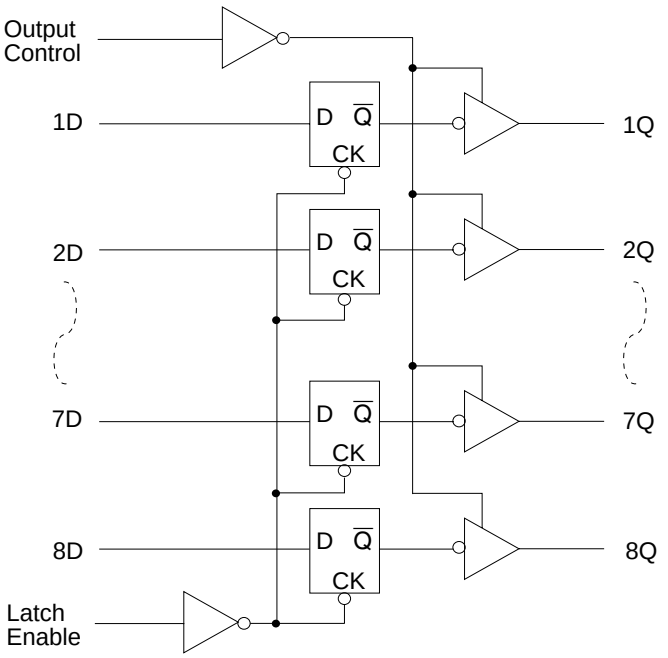
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	—	V_{CC}	V
Output voltage	V_{OUT}	0	—	V_{CC}	V
Operating temperature	Topr	–40	—	85	°C
Input rise/fall time*[1]	t_r, t_f	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics (Ta = –40°C to +85°C)

Item	Symbol	V_{cc} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}		2.0	—	V	
	V_{IL}		—	0.8	V	
Output voltage	V_{OH}	4.5	2.4	—	V	I_{OH} = –3 mA
		4.5	2.0	—	V	I_{OH} = –15 mA
	V_{OL}	4.5	—	0.4	V	I_{OL} = 24 mA
		4.5	—	0.5	V	I_{OL} = 48 mA
Input diode voltage	V_{IK}	4.5	—	–1.2	V	I_{IN} = –18 mA
Input current	I_I	5.5	—	–250	µA	V_{IN} = 0 V
		5.5	—	1.0	µA	V_{IN} = 5.5 V
		5.5	—	100	µA	V_{IN} = 7.0 V
Short circuit output current*[1]	I_{OS}	5.5	–100	–225	mA	V_{IN} = 0 or 5.5 V
Off state output current	I_{OZH}	5.5	—	50	µA	V_O = 2.7 V
	I_{OZL}	5.5	—	–50	µA	V_O = 0.5 V
Supply current	I_{CCL}	5.5	—	29.5	mA	V_{IN} = 0 or 5.5 V All outputs is “L”
	I_{CCH}	5.5	—	2.5	mA	V_{IN} = 0 or 5.5 V All outputs is “H”
	I_{CCZ}	5.5	—	2.5	mA	V_{IN} = 0 or 5.5 V All outputs is “Z”
	I_{CCT}*[2]	5.5	—	1.5	mA	V_{IN} = 3.4 or 0.5 V

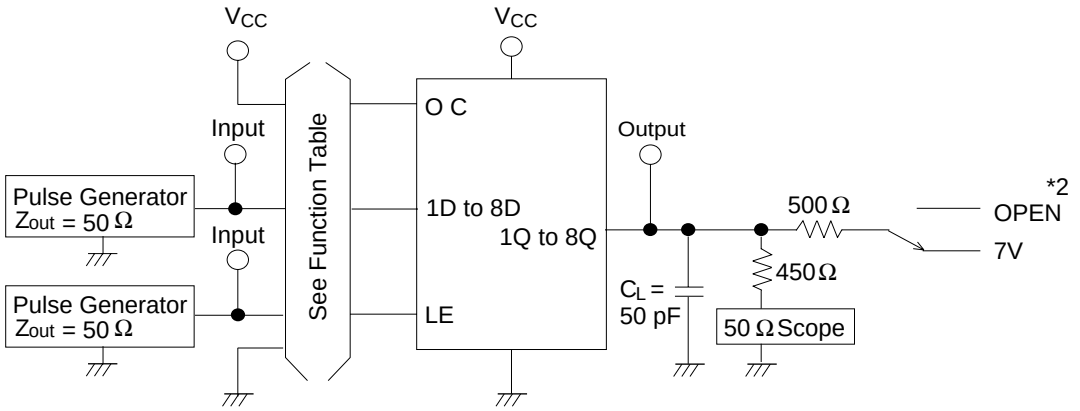
Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2. When input by the TTL level, it shows I_{CC} increase at per one input pin.

Switching Test Method (C_L = 50 pF)

Item		Symbol	Ta = 25°C, V_{cc} = 5.0 V Min	Ta = 25°C, V_{cc} = 5.0 V Max	Ta = –40 to 85°C, V_{cc} = 5.0 V ±10% Min	Ta = –40 to 85°C, V_{cc} = 5.0 V ±10% Max	Unit	Test conditions
Propagation delay time	D → Q	t_{PLH}	3.0	8.0	3.0	10.0	ns	See under figure
		t_{PHL}	3.0	8.0	3.0	10.0		
	LE → Q	t_{PLH}	3.0	8.0	3.0	10.0	ns	
		t_{PHL}	3.0	8.0	3.0	10.0		
Output enable time		t_{ZH}	3.0	9.0	3.0	11.0	ns	
		t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time		t_{HZ}	3.0	8.0	3.0	10.0	ns	
		t_{LZ}	3.0	8.0	3.0	10.0		
Setup time		t_S(H)	2.0	—	2.0	—	ns	
		t_S(L)	2.0	—	2.0	—		
Hold time		t_h(H)	2.0	—	2.0	—	ns	
		t_h(L)	2.0	—	2.0	—		
Pulse width		t_w	6.0	—	6.0	—	ns	
Input capacitanse		C_{IN}	3.0 (Typ)		—		pF	V_{IN} = V_{CC} or GND
Output capacitance		C_O	15.0 (Typ)		—		pF	V_O = V_{CC} or GND

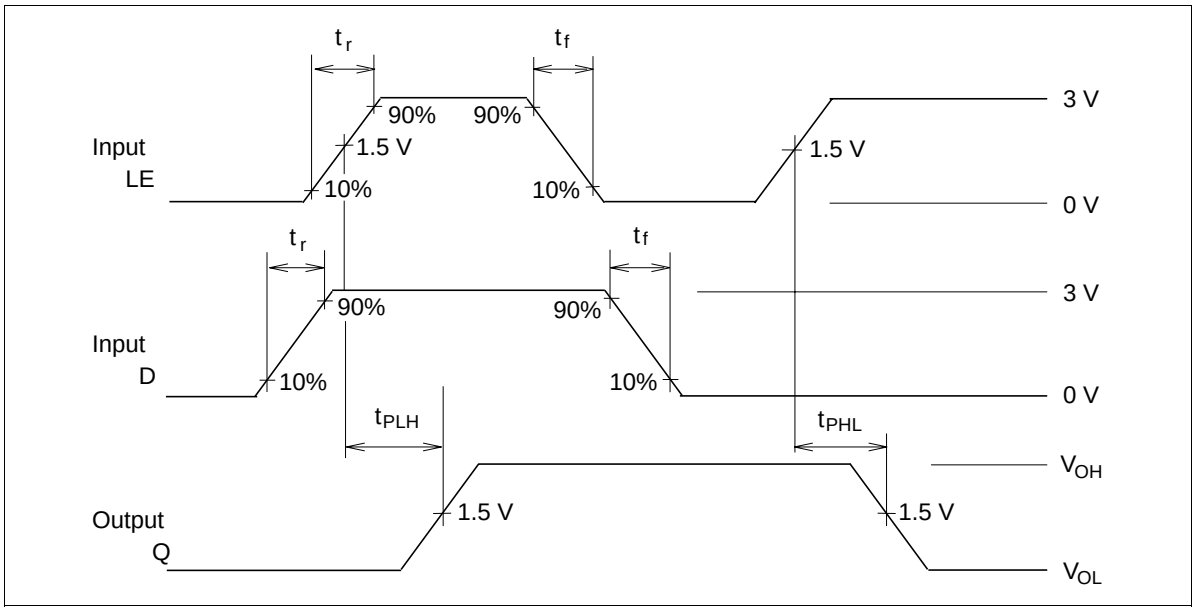
Test Circuit



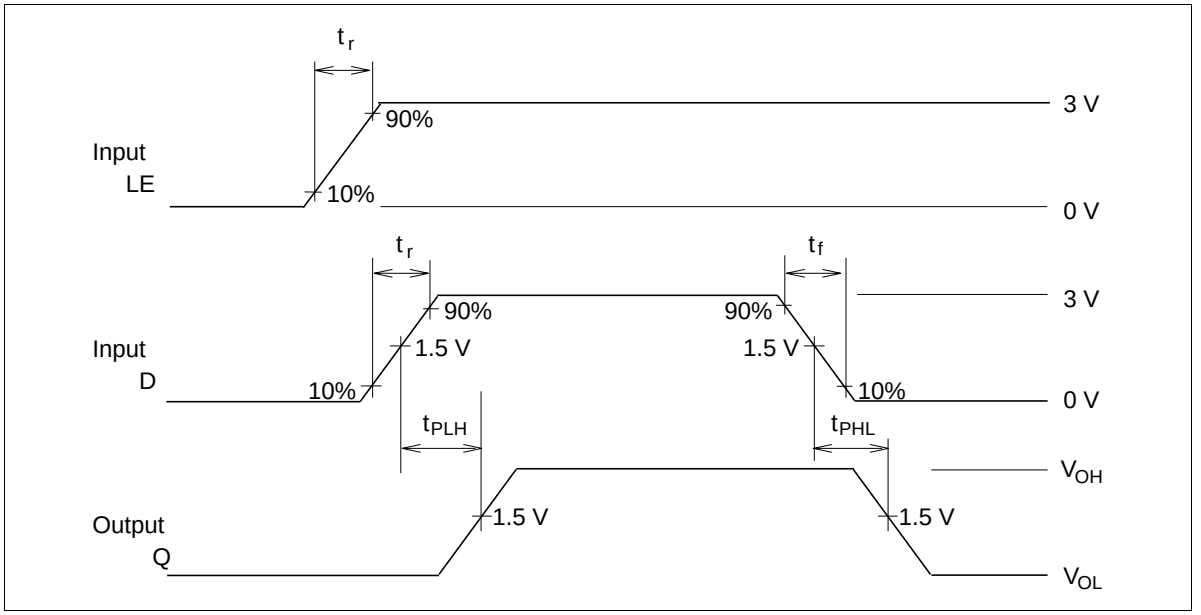
Notes: 1. C_L includes probe and jig capacitance.

2. OPEN: t_{PLH}, t_{PHL}, t_{ZH}, t_{HZ}, t_h, t_S, t_w
   7 V: t_{ZL}, t_{LZ}

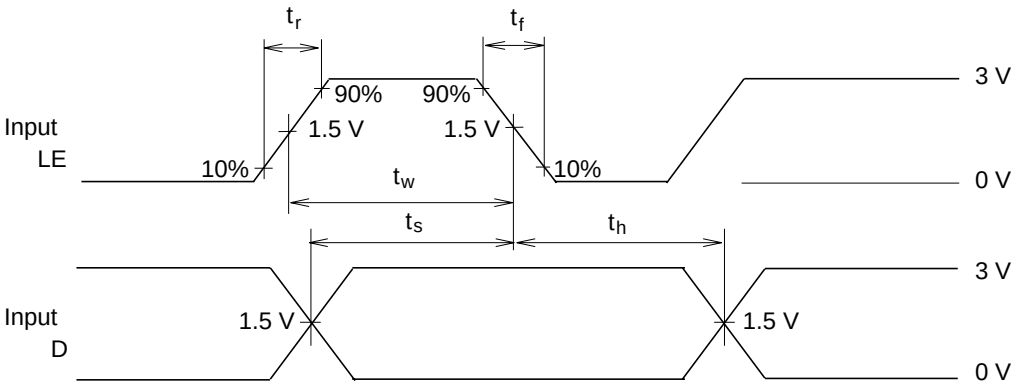
Waveforms-1



Waveforms-2

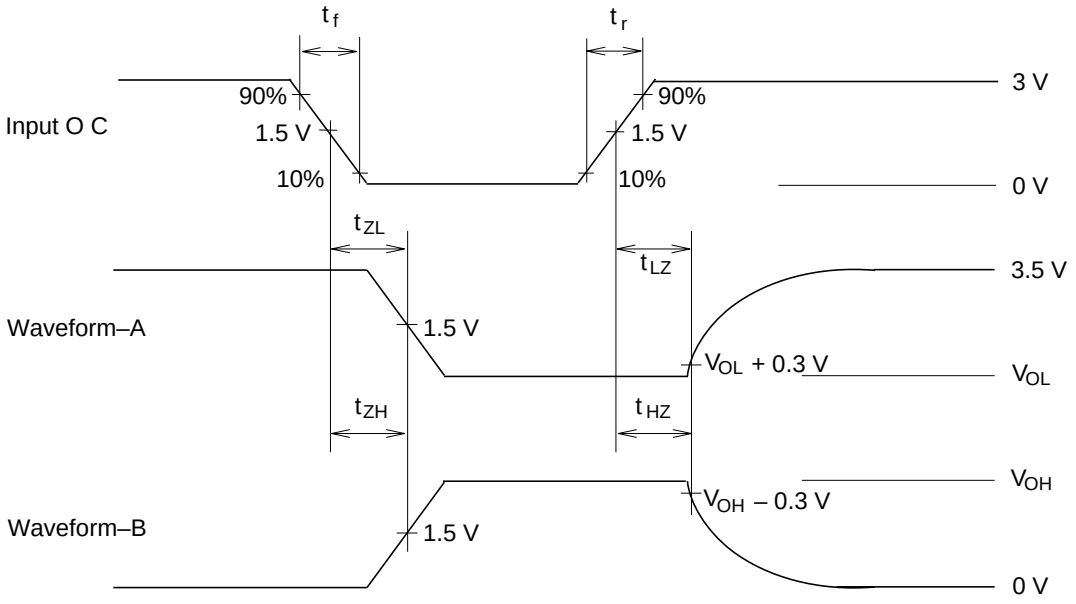


Waveforms-3



Notes: 1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform: PRR =1 MHz, duty cycle 50%

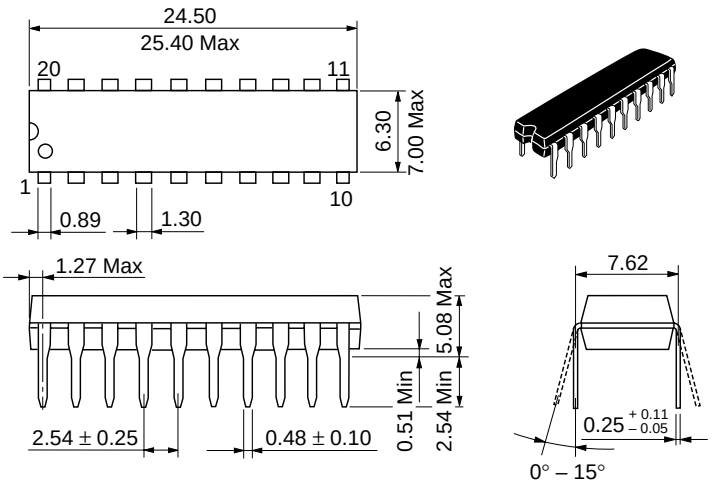
Waveforms-4



Notes: 1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform: PRR = 1 MHz, duty cycle 50%
3. Waveform-A shows input conditions such that the output is “L” level when enable by the output control.
4. Waveform-B shows input conditions such that the output is “H” level when enable by the output control.

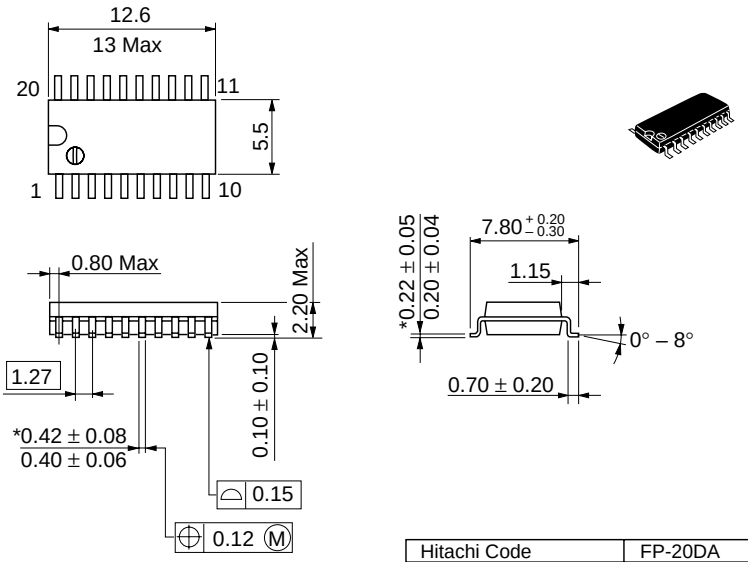
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

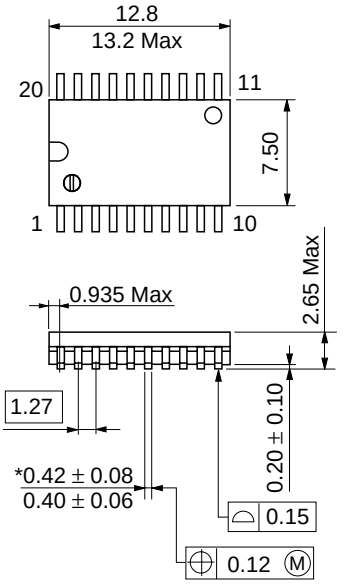
Unit: mm

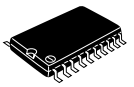


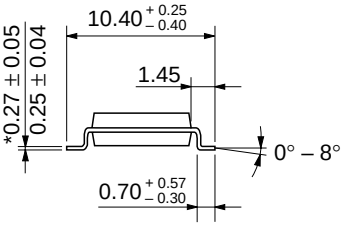
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

Unit: mm



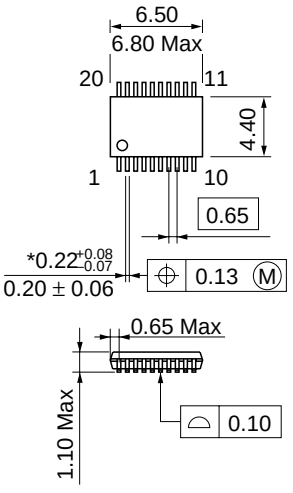


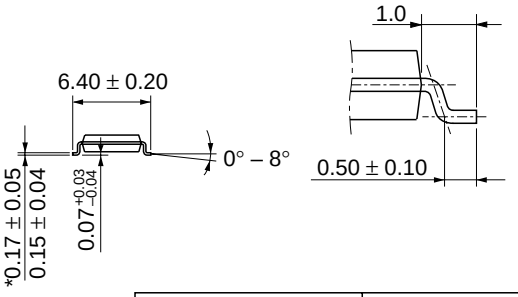


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.07 g

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