8Mx64 bit SDRAM SO DIMM Z-Series

based on 8Mx8 SDRAM, LVTTL, 2/4-Banks & 4K/8K-Refresh

HYM7V64800/ HYM7V64801/ HYM7V64830/ HYM7V64831

DESCRIPTION

The HYM7V64800/ 64801/ 64830/ 64831 Z-Series are high speed 3.3-Volt synchronous dynamic RAM Modules composed of eight 8Mx8 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E^2PROM on a 144-pin Zig Zag Dual pin glass-epoxy printed circuit board. One 0.22μF and one 0.0022μF decoupling capacitors per each SDRAM are mounted on the module.

The HYM7V64800/ 64801/ 64830/ 64831 Z-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 64M bytes memory. All addresses, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidths.

FEATURES

- 144-Pin Unbuffered SO DIMM
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms or 8192 refresh cycles every 128ms
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual or Quad internal banks with single pulsed /RAS
- Auto precharge/precharge all banks by A10 flag
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 1,2,3 clocks
- Support clock suspend/power down mode by CKE0
- Data mask function by DQM
- Mode register set programming
- Burst termination command
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

Part No.	Max. Frequency	SDRAM Bank	Refresh	Package	Plating
HYM7V64800TZG - 10/12/15	100/ 83/ 66 MHz	2 Banks	4K	TSOP	Gold
HYM7V64801TZG - 10/12/15	100/ 83/ 66 MHz	4 Banks	4K	TSOP	Gold
HYM7V64830TZG - 10/12/15	100/ 83/ 66 MHz	2 Banks	8K	TSOP	Gold
HYM7V64831TZG - 10/12/15	100/ 83/ 66 MHz	4 Banks	8K	TSOP	Gold

PIN DESCRIPTION

Pin Name	Pin Type	Description
CK0, CK1	INPUT	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
CKE0	INPUT	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0	INPUT	Chip select; Functions command mask(NOP).
/RAS	INPUT	Row address strobe; See functional truth table in 8Mx8 Data Sheets for details.
/CAS	INPUT	Column address strobe; See functional truth table in 8Mx8 Data Sheets for details.
/WE	INPUT	Write Enable; See functional truth table in 8Mx8 Data Sheets for details.
DQM0-7	INPUT	Data Input / Output Mask
DQ0-DQ63	INPUT/ OUTPUT	Data Input / Output; Include inputs, outputs, or Hi-z state.
V_{CC}	SUPPLY	Power Supplies; 3.3V±0.3V
V_{SS}	SUPPLY	Ground
SDA	INPUT/ OUTPUT	Serial Address and Data Input / Output.
SCL	INPUT	Serial Clock

HYM7V64800/HYM7V64830 Z-Series (2Bank 8Mx8 SDRAM Based)

Pin Name	Pin Type	Description
BA0	INPUT	Bank select address inputs; Select one of dual banks during both /RAS and /CAS activity.
A0-A12	INPUT	Address Inputs; A0-A8; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A9-A12; X addresses only.

HYM7V64801/HYM7V64831 Z-Series (4Bank 8Mx8 SDRAM Based)

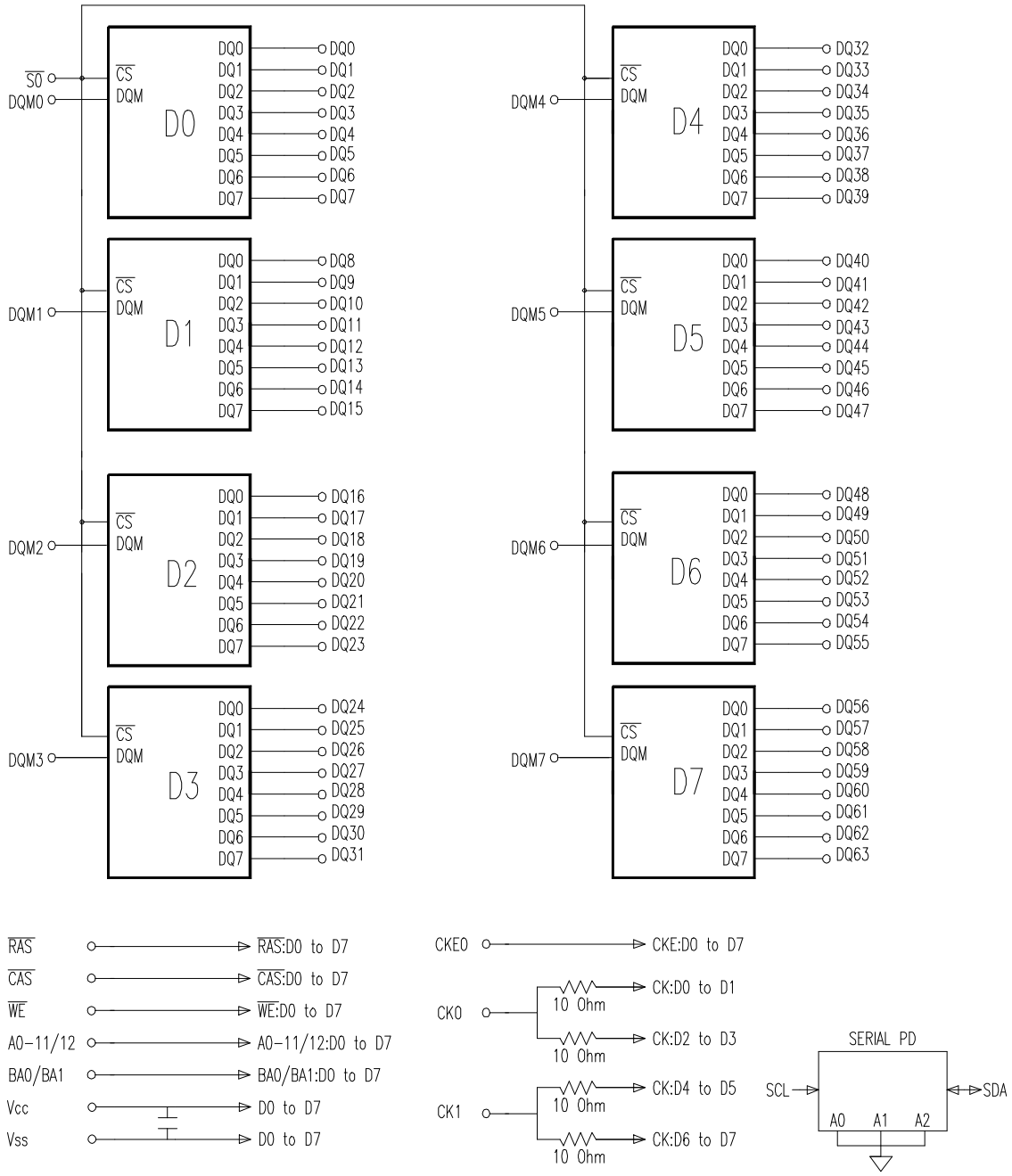
Pin Name	Pin Type	Description
BA0, BA1	INPUT	Bank address inputs; Select one of quad banks during both /RAS and /CAS activity.
A0-A11	INPUT	Address Inputs; A0-A8; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A9-A11; X addresses only.

PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	2	Vss	73	DU	74	CK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	*BA1
39	DQ9	40	DQ41	111	A10(AP)	112	A11
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	Vcc	46	Vcc	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	NC	58	NC	129	Vcc	130	Vcc
59	NC	60	NC	131	DQ28	132	DQ60
61	CK0	62	CKE0	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	/RAS	66	/CAS	137	DQ31	138	DQ63
67	/WE	68	NC	139	Vss	140	Vss
69	/S0	70	*A12	141	SDA	142	SCL
71	NC	72	NC	143	Vcc	144	Vcc

Note : 1. BA1 is used for HYM7V64801/HYM7V64831 Z-Series (4 Bank 8Mx8 Based)
2. A12 is used for HYM7V64800/HYM7V64830 Z-Series (2 Bank 8Mx8 Based)

BLOCK DIAGRAM



I-1 SERIAL PRESENCE DETECT

[HYM7V64800/HYM7V64830 Z-Series; 2 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	2 Banks; 13	0Dh	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	64 Bits	40h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	tCLK (A) 10ns (B) 12ns (C) 15ns	 (A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	tAC (A) 8ns (B) 9ns (C) 10ns	 (A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	None	00h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	None	00h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 2 Bank 8Mx8 Based	 2 Banks	 02h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	tCLK (A) 12ns (B) 15ns (C) 15ns	 (A) C0h (B) F0h (C) F0h	3

I-2 SERIAL PRESENCE DETECT

[HYM7V64800/HYM7V64830 Z-Series; 2 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	 (A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCLK (A) 30ns (B) 30ns (C) 30ns	 (A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	 (A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	 (A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	 (A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	64MB	10h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	 (A) Decimal 242 (B) Decimal 86 (C) Decimal 187	 (A) F2h (B) 56h (C) BBh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

Note : 1. The bank address is excluded.
2. In interleaved type. the burst lengths supported is 1,2,4,8.
3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
* All above data can be changed, if the JEDEC standard is modified.

II-1 SERIAL PRESENCE DETECT

[HYM7V64801/HYM7V64831 Z-Series; 4 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	4 Banks; 12	0Ch	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	1 Bank	01h	
BYTE6	Data Width of This Assembly	64 Bits	40h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	t_{CK} (A) 10ns (B) 12ns (C) 15ns	 (A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	t_{AC} (A) 8ns (B) 9ns (C) 10ns	 (A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	None	00h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	None	00h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	t_{CCD}=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 4 Bank 8Mx8 Based	4 Banks	04h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	t_{CK} (A) 12ns (B) 15ns (C) 15ns	 (A) C0h (B) F0h (C) F0h	3

II-2 SERIAL PRESENCE DETECT [HYM7V64801/HYM7V64831 Z-Series; 4 Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	 (A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCK (A) 30ns (B) 30ns (C) 30ns	 (A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	 (A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	 (A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	 (A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	64MB	10h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	 (A) Decimal 243 (B) Decimal 87 (C) Decimal 188	 (A) F3h (B) 57h (C) BCh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

Note : 1. The bank address is excluded.
2. In interleaved type. the burst lengths supported is 1,2,4,8.
3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
* All above data can be changed, if the JEDEC standard is modified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8	W
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS* (T_A=0°C to 70°C)

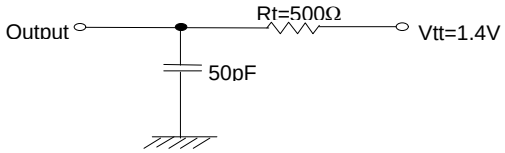
Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	
Vss	Power Supply Voltage	0	0	0	V	
V_{IH}	Input High Voltage	2.0	-	V_{CC} + 0.4	V	LVTTL
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	LVTTL

RECOMMENDED AC OPERATING CONDITIONS* (T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

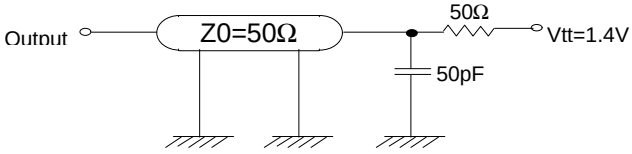
Symbol	Parameter	Value	Unit	Note
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4/0.4	V	LVTTL
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V	LVTTL
tr / tf	Input Rise/Fall Time	1	ns	
Voutref	Output Reference Voltage	1.4	V	LVTTL
C_L	Output Load Capacitance for Access Time Measurement	Note	pF	

Note : Output load to measure access times is equivalent to two TTL gates and one capacitance(50pF).

Note : * DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS(I)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Note
I_{LI}	Input Leakage Current	V_I=0 to 3.6V, All other pins not undertest=0V	-8	8	μA	
I_{LO}	Output Leakage Current	D_{OUT} is disabled, V_O=0 to 3.6V	-1	1	μA	
V_{OL}	Output Low Voltage	I_O=2.0mA	-	0.4	V	LVTTL
V_{OH}	Output High Voltage	I_O=-2.0mA	2.4	-	V	LVTTL

DC CHARACTERISTICS(II)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition		Max.	Unit	Note
I_{CC1}	Operating current	Burst Length=1, One bank active t_{RAS}≥t_{RAS}(min), t_{RP}≥t_{RP}(min), I_O=0mA	10ns	680	mA	Note 2
			12ns	560		
			15ns	480		
I_{CC2P}	Precharge Standby Current in Power Down Mode	CKE≤V_{IL}(max)		16	mA	
I_{CC2N}	Precharge Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{CC}-0.2V or ≤0.2V		96	mA	LVTTL[1]
I_{CC3P}	Active Standby Current in Power Down Mode	CKE≤V_{IL}(max), All banks active		24	mA	
I_{CC3N}	Active Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{CC}-0.2V or ≤0.2V All banks active		280	mA	LVTTL[1]
I_{CC4}	Operating Current (Burst Mode)	t_{CLK}≥t_{CLK}(min), t_{RAS}≥t_{RAS}(min), I_O=0mA, /CAS Latency=3	10ns	1200	mA	Note 2
			12ns	960		
			15ns	800		
I_{CC5}	Refresh Current	t_{RC}≥t_{RC}(min), Two banks active (8K/128ms)	10ns	880	mA	Note 2
			12ns	720		
			15ns	600		
		t_{RC}≥t_{RC}(min), Four banks active (4K/64ms)	10ns	1280	mA	Note 2
			12ns	1040		
			15ns	840		
I_{CC6}	Self Refresh Current	CKE≤0.2V		16	mA	

Note :

1. It depends on the number of each pin's transition. It is assumed there is no transition to measure this current.
2. I_{CC1} depends on output loads and cycle rates. Specified values are obtained with the output open. In addition this I_{CC1} is measured on condition that addresses are changed only one time during t_{CLK}(Min.)

AC CHARACTERISTICS

Synchronous Characteristics(I)

Parameter	100MHz (10ns)			83MHz (12ns)			66MHz (15ns)			Unit
/CAS Latency	3	2	1	3	2	1	3	2	1	Latency
Frequency	100	83	33	83	66	33	66	66	33	MHz
Clock Cycle Time	10	12	30	12	15	30	15	15	30	ns
t_{RCD}	3	2	1	3	2	1	3	2	1	CLK(s)
t_{RAS}	5	4	2	4	4	2	3	4	2	CLK(s)
t_{RP}	3	3	1	3	2	1	3	2	1	CLK(s)
t_{RC}	8	7	3	7	6	3	-	6	3	CLK(s)
t_{RRD}	3	2	1	2	2	2	2	2	2	CLK(s)
t_{DPL}	1	1	1	1	1	1	-	1	1	CLK(s)
t_{DAL}	4	3	2	3	3	2	-	3	2	CLK(s)
t_{SRE}	1	1	1	1	1	1	-	1	1	CLK(s)
t_T	1			1			1			ns
Refresh Cycle	8K/128ms, 4K/64ms									Cycles
Asynchronous Characteristic	50ns Part									ns

Note : t_{RRD} -Bank Active to Active Command
t_{DPL} -D_{IN} to Precharge Command
t_{DAL} -D_{IN} to Active(Ref.) Command (After Write with Autoprecharge)
t_{SRE} -Self Refresh Exit Time

Synchronous Characteristics(II)

Symbol	Parameter		-10		-12		-15		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AC}	Access Time from CLK	/CAS Lat.=3	-	8	-	9	-	10	ns	
		/CAS Lat.=2	-	9	-	9	-	10	ns	
		/CAS Lat.=1	-	24	-	24	-	24	ns	
t_{CH}	CLK High Level Width		3.5	-	3.5	-	3.5	-	ns	
t_{CL}	CLK Low Level Width		3.5	-	3.5	-	3.5	-	ns	
t_{OH}	Data-out Hold Time		3	-	3	-	3	-	ns	
t_{OLZ}	Data-out Low-Impedance Time		3	-	3	-	3	-	ns	
t_{OHZ}	Data-out High-Impedance Time		0	8	0	9	0	10	ns	
t_{DS}	Data-in Set-up Time		3	-	3	-	3	-	ns	
t_{DH}	Data-in Hold Time		1	-	1	-	1	-	ns	
t_{AS}	Address Set-up Time		3	-	3	-	3	-	ns	
t_{AH}	Address Hold Time		1	-	1	-	1	-	ns	
t_{CKS}	CKE Set-up Time		3	-	3	-	3	-	ns	
t_{CKH}	CKE Hold Time		1	-	1	-	1	-	ns	
t_{CS}	Command Set-up Time		3	-	3	-	3	-	ns	
t_{CH}	Command Hold Time		1	-	1	-	1	-	ns	
t_{PDE}	Power Down Exit Set-up Time		3	-	3	-	3	-	ns	

Latency

Symbol	Parameter		Latency
t_{CKED}	CKE to CLK Suspend / Power Down Mode Entry		1
t_{DQMOZ}	DQM to Data Output in Hi-z		2
t_{DQMIM}	DQM to Data Input Mask		0
t_{WTL}	Write Command to Data Input Valid		0
t_{PROZ}	Precharge Command to Data Output in Hi-z	/CAS Latency=1	1
		/CAS Latency=2	2
		/CAS Latency=3	3
t_{MRD}	Mode Register Set to New Command		1
t_{CCD}	Min. Column Address to Column Address Delay		1
t_{PPD}	Min. Precharge to Precharge Time		1

Note :
1. All voltages referenced V_{SS}(Ground).
2. An initial pause of 100μS is required after power-on followed by Power On Sequence & Auto Refresh before proper device operation is achieved.
3. AC measurements assume t_T=1ns.
4. Reference level for measuring timing of input signals is 1.40V for LVTTL
   Transition times are measured between V_{IH} and V_{IL}.
5. An access time is measured at 1.40V for LVTTL

CAPACITANCE

(T_A=25°C, f=1MHz)

Symbol	Parameter	Pin	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	A0-A11/12, BA0/BA1	-	60	pF
C_{IN2}	Input Capacitance	/RAS, /CAS, /WE	-	60	pF
C_{IN3}	Input Capacitance	/S0	-	60	pF
C_{IN4}	Input Capacitance	CK0, CK1	-	40	pF
C_{IN5}	Input Capacitance	CKE0		60	pF
C_{IN6}	Input Capacitance	DQM0-DQM7	-	15	pF
C_{OUT}	Output Capacitance	DQ0-DQ63	-	15	pF

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET(WRITE)

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	/CAS Latency			BT	Burst Length		

A3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round)

A6	A5	A4	/CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full page[1]

Note : 1. Full page burst supports only sequential type.

TEST MODE

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
0	0	0	0	1	X	X	X	X	X	X	X	Refresh Counter Test

Note : Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using ′Precharge All banks′.

BURST LENGTH AND SEQUENCE

Burst Length	Initial Address	Burst Type	
	A2 A1 A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4,……,m 1,2,3,4,5,……,0 : : m,0,1,2,3,……,m-1	Not supported

Table 1. Address sequence for different burst lengths

Note : 4Mbit x 2banks x 8I/O - Initial addresses: A8-A0, Page length: 1024, m=1023
2Mbit x 4banks x 8I/O - Initial addresses: A8-A0, Page length: 1024, m=1023

PACKAGE DIMENSION