HYM7V72A400B F-Series

Unbuffered 4Mx72 bit SDRAM MODULE
based on 2Mx8 SDRAM, LVTTL, 4K-Refresh

DESCRIPTION

The HYM7V72A400B is high speed 3.3Volt synchronous dynamic RAM module consisting of sixteen 2Mx8 bit Synchronous DRAMs in TSOPII and 8-pin TSSOP 2K bit EEPROM on a 168-pin glass-epoxy circuit board. Two 0.22μF and two 0.0022μF decoupling capacitors are mounted for each SDRAM.

The HYM7V72A400B is a gold plated socket type Dual In-line Memory Module suitable for easy interchange and addition of 32M byte memory. All address, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipelined to achieve very high bandwidth.

FEATURES

- 168Pin Unbuffered DIMM
- Serial Presence Detect with EEPROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual internal banks with single pulsed /RAS
- Auto precharge/precharge all banks by A10 flag
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 1,2,3 clocks
- Support clock suspend/power down mode by CKE0/1
- Data mask function by DQMB
- Mode register set programming
- Burst termination command
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

Part No.	Max. Frequency	Power	Package	Plating
HYM7V72A400BTFG -10/12/15	100/83/67MHz	-	TSOP	GOLD

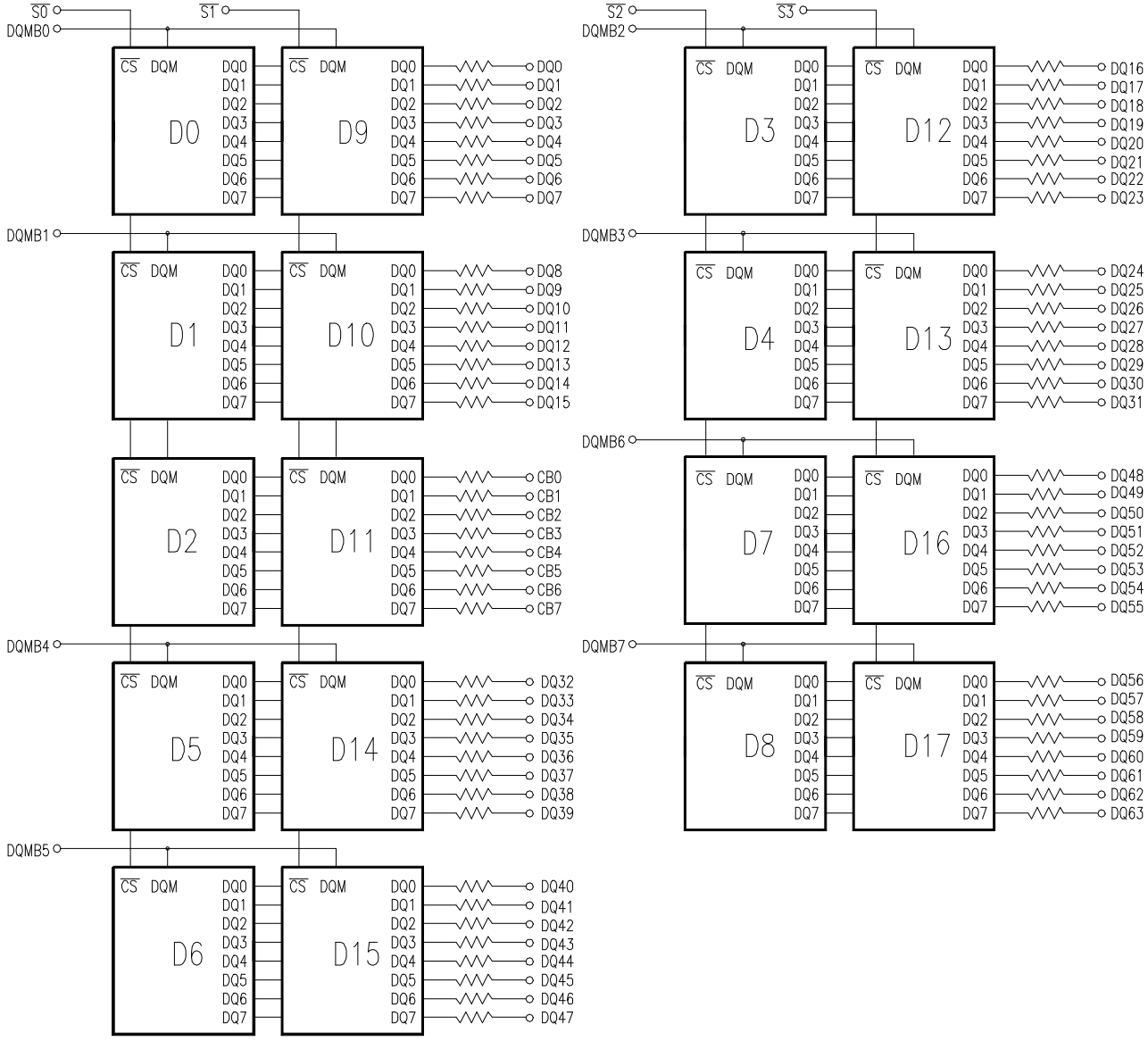
PIN DESCRIPTION

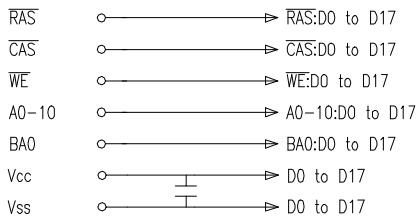
Pin Name	Pin Type	Description
CK0 - CK3	INPUT	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
CKE0, CKE1	INPUT	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
BA0	INPUT	Bank address inputs; Select either one of dual banks during both /RAS and /CAS activity.
A0-A10	INPUT	Address Inputs; A0-A8; X&Y address, Opcode for mode register set. A9 ; X address only. A10 ; X address, Precharge flag.
/S0 - /S3	INPUT	Chip select; Functions command mask(NOP).
/RAS	INPUT	Row address strobe; See functional truth table for details.
/CAS	INPUT	Column address strobe; See functional truth table for details.
/WE	INPUT	Write Enable; See functional truth table for details.
DQMB0-7	INPUT	Data Input / Output Mask
DQ0-DQ63 CB0-CB7	INPUT/ OUTPUT	Data Input / Output; Include inputs, outputs, or Hi-z state.
V_{CC}	SUPPLY	Power Supplies; 3.3V±0.3V
V_{SS}	SUPPLY	Ground
SDA	INPUT/ OUTPUT	Serial Address and Data Input / Output.
SCL	INPUT	Serial Clock
SA0-SA2	INPUT	Address in EEPROM for Socket Presence.

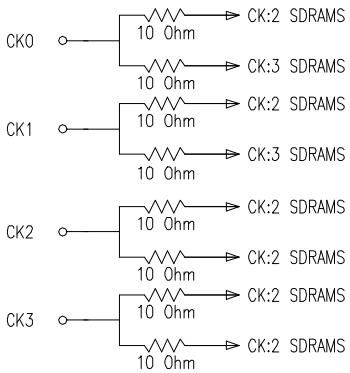
PIN NAME

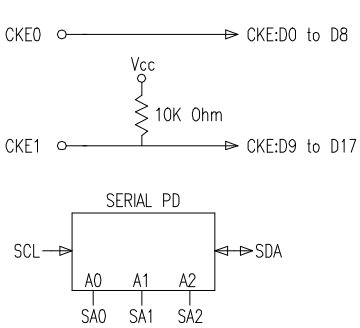
#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	VSS	85	VSS	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	DU	73	VCC	115	/RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CK2	121	A9	163	CK3
38	A10(AP)	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	NC	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CK1	167	SA2
42	CK0	84	VCC	126	NC	168	VCC

BLOCK DIAGRAM









Note : 1. The serial resistor values of DQs are 10 Ohms.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Byte Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	11	0Bh	1
BYTE4	# of Column Addresses on This Assembly	9	09h	1
BYTE5	# of Module Banks on This Assembly	2 Bank	02h	
BYTE6	Data Width of This Assembly	72 Bits	48h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3, 10 part @ /CAS Latency=3, 12 part @ /CAS Latency=3, 15 part	 10ns 12ns 15ns	 A0h C0h F0h	
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, 10 part @ /CAS Latency=3, 12 part @ /CAS Latency=3, 15part	 8ns 8.5ns 9ns	 80h 85h 90h	
BYTE11	DIMM Configuration Type	ECC	02h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	x8	08h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 CLK	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device	2 Banks	02h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Non Buffered and Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Single bit write, Precharge All, Auto Precharge)		0Eh	

Note: 1. The bank address is excluded.
2. In interleaved type. the burst lengths supported is 1,2,4,8.

SERIAL PRESENCE DETECT

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE23	SDRAM Cycle Time			
	@ /CAS Latency=2, 10 part	15ns	F0h	
	@ /CAS Latency=2, 12 part	18ns	30h	
	@ /CAS Latency=2, 15 part	22.5ns	75h	
BYTE24	SDRAM Access Time from Clock			
	@ /CAS Latency=2, 10 part	9ns	90h	
	@ /CAS Latency=2, 12 part	9.5ns	95h	
	@ /CAS Latency=2, 15 part	10ns	A0h	
BYTE25	SDRAM Cycle Time			
	@ /CAS Latency=1, 10 part	30ns	78h	
	@ /CAS Latency=1, 12 part	36ns	90h	
	@ /CAS Latency=1, 15 part	45ns	B4h	
BYTE26	SDRAM Access Time from Clock			
	@ /CAS Latency=1, 10 part	10ns	28h	
	@ /CAS Latency=1, 12 part	10.5ns	2Ah	
	@ /CAS Latency=1, 15 part	11ns	2Ch	
BYTE27	Minimum Row Pre-charge Time			
	@ /CAS Latency=3, 10 part	30ns	1Eh	
	@ /CAS Latency=3, 12 part	36ns	24h	
	@ /CAS Latency=3, 15 part	45ns	2Dh	
BYTE28	Minium Rpw Active to Row Active Delay			
	@ /CAS Latency=3, 10 part	20ns	14h	
	@ /CAS Latency=3, 12 part	24ns	18h	
	@ /CAS Latency=3, 15 part	30ns	1Eh	
BYTE29	Minium /RAS to /CAS Delay			
	@ /CAS Latency=3, 10 part	30ns	1Eh	
	@ /CAS Latency=3, 12 part	36ns	24h	
	@ /CAS Latency=3, 15 part	45ns	2Dh	
BYTE30	Minimum /RAS Pulse width			
	@ /CAS Latency=3, 10 part	60ns	3Ch	
	@ /CAS Latency=3, 12 part	70ns	46h	
	@ /CAS Latency=3, 15 part	80ns	50h	
BYTE31	Module Bank Density	16MB	04h	
BYTE32-61	Superset Information (May Be Used in Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62	-		
	10 part		F7h	
	12 part		95h	
	15 part		68h	
BYTE64-127	Manufacturer Information(Optional)	-	00h	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-0.5 to 4.6	V
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	18	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED AC OPERATING CONDITIONS* (T_A=0°C to 70°C, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Value	Unit
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4 / 0.4	V
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V
tr / tf	Input Rise/Fall Time	1 / 1	ns
Voutref	Output Reference Voltage	1.4	V
C_L	Output Load Capacitance for Access Time Measurement	Note1	pF

Note: 1. Output load to measure access times(tAC, tOH, etc.) varies to clock frequency. A load is equivalent to one TTL gate and one capacitance.

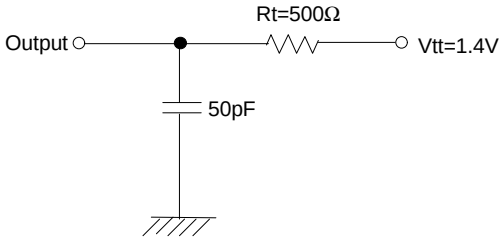
RECOMMENDED DC OPERATING CONDITIONS* (T_A=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}, V_{DDQ}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{DD}+0.3	V
V_{IL}	Input Low Voltage	-0.5	-	0.8	V

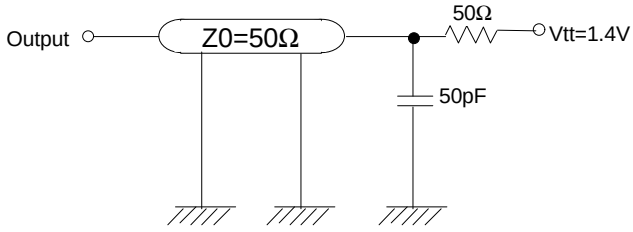
Note :
1.All voltages are referenced to Vss = 0V
2.VIH(max) is acceptable 4.6V AC pulse width with ≤ 10ns of duration
3.VIL(max) is acceptable –1.5V AC pulse width with ≤ 10ns of duration.

OUTPUT LOAD CIRCUIT

DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS I (T_A=0°C to 70°C, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Any Input Pins)	V_{SS}<V_{IN}<V_{DD}+1.0 All other pins not under test=Vss	-90	90	µA
I_{LO}	Output Leakage Current (High impedance State)	V_{SS}<V_{OUT}<V_{DD} Both Banks in idle state	-10	10	µA
V_{OL}	Output Low Voltage	I_{OL}=2.0mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}=-2.0mA	2.4	-	V

DC CHARACTERISTICS II (T_A=0°C to 70°C, V_{DD}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter/Condition	t_{CLK}	Speed/Power-Max.			Unit	Note
			-10	-12	-15		
I_{DD1}	/RAS Operating Current per bank No /CAS activity, t_{RC}=t_{RC}(min)	min	1080	900	855	mA	1,2
I_{DD2PD}	Precharge Stand-by Current in Power-Down Mode, CKE<V_{IL}(max)	min ∞	54 36	54 36	54 36	mA	
I_{DD2NP}	Precharge Stand-by Current in Non Power-Down Mode, CKE>V_{IH}(min)	min ∞	360 270	360 270	360 270	mA	3
I_{DD3PD}	Active Stand-by Current in Power-Down Mode, CKE<V_{IL}(max)	min ∞	540 540	540 540	540 540	mA	4
I_{DD3NP}	Active Stand-by Current in Non Power-Down Mode, CKE>V_{IH}(min)	min ∞	900 540	900 540	900 540	mA	3,4
I_{DD4}	Burst Mode Operating Current(/CAS Lat.=3)	min	1080	900	855	mA	2,5,6
I_{DD5}	Auto Refresh Operating Current, t_{RC}=t_{RC}(min)	min	1080	900	855	mA	2
I_{DDS}	Self Refresh Operating Current, CKE<0.2V	- -	36 7.2	36 7.2	36 7.2	mA mA	 L-part

Notes :
1. `No /CAS activity` means that the operating cycle activates row circuits only while it does not command any read or write cycle, what could be called, /CAS activity.
2. All IDD currents except IDDS depend on cycle rate.
3. All input signals are toggled every other clock cycle.
4. Assuming that one bank is active.
5. These IDD Parameters are dependent on output loading.
   Specified values are obtained with the outputs open.
6. Specified values are obtained with the timing that a burst cycle is completed upto its registered burst length without any interrupt cycle. Interrupted burst cycle may consume more power.

CAPACITANCE (T_A=25°C, V_{DD}=3.3V, f=1MHz)

Symbol	Parameter	Pin	Typ.	Max.	Unit
C_{I1}	Input Capacitance	A0-A10,BA0	-	95	pF
C_{I2}	Input Capacitance	/RAS,/CAS,/WE	-	95	pF
C_{I3}	Input Capacitance	/S0 - /S3	-	40	pF
C_{I4}	Input Capacitance	CK0 - CK3	-	35	pF
C_{I5}	Input Capacitance	CKE0.CKE1	-	60	pF
C_{I6}	Input Capacitance	DQMB0-DQMB7	-	25	pF
C_{OUT}	Output Capacitance	DQ0-DQ63, CB0-CB7	-	20	pF

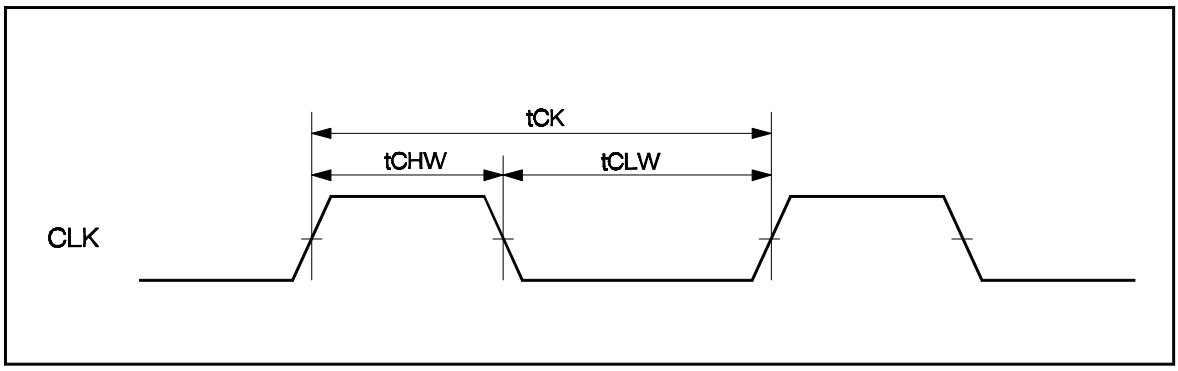
AC CHARACTERISTICS

[PART1] Synchronous Parameters referred to Clock[1,2,3,4]

#	Symbol	Parameter		-10		-12		-15		Unit	Note
				Min.	Max.	Min.	Max.	Min.	Max.		
1	tCK	System Clock Cycle Time	/CAS Lat=3	10	-	12	-	15	-	ns	3,5
			/CAS Lat=2	15	-	18	-	22.5	-	ns	3,5
2	tCHW	CLK High Level Width		3	-	4	-	5	-	ns	2
3	tCLW	CLK Low Level Width		3	-	4	-	5	-	ns	2
4	tAC	Access Time from Clock	/CAS Lat=3	-	8	-	8.5	-	9	ns	3
			/CAS Lat=2	-	9	-	9.5	-	10	ns	3
5	tAA	Read command to DQ access		-	20	-	25	-	30	ns	
6	tAS	Address Set-up Time		3	-	3	-	3	-	ns	2
7	tAH	Address Hold Time		1	-	1.5	-	1.5	-	ns	2
8	tCKS	CKE set-up Time		3	-	3	-	3	-	ns	2
9	tCKH	CKE Hold Time		1	-	1.5	-	1.5	-	ns	2
10	tCS	Command Set-up Time		3	-	3	-	3	-	ns	2
11	tCH	Command Hold Time		1	-	1.5	-	1.5	-	ns	2
12	tDS	Data-in Set-up Time		3	-	3	-	3	-	ns	2
13	tDH	Data-in Hold Time		1	-	1.5	-	1.5	-	ns	2
14	tOH	Data-out Hold Time		3	-	3	-	3	-	ns	2
15	tOLZ	Data-out Low-Z Time		2	-	2	-	2	-	ns	
16	tOHZ	Data-out High-Z Time	/CAS Lat.=3	-	8	-	8.5	-	9	ns	
			/CAS Lat.=2	-	9	-	9.5	-	10	ns	

Notes:

1. An initial pause of 200μS is required after power-up by `Power On Sequence`(JEDEC Standard.) and Auto Refresh before proper device operation is achieved.
2. Assume tR / tF (input rising and hold time) is 1ns. If tr&tf >1ns then [(tr+tf)/2-1]ns should be added to the parameter
3. If clock rising time > 1ns then (tr/2-0.5)ns should be added to the parameter
4. (VIH+VIL)/2 is a reference level for measuring of timing of input signals. Also transition time is measured between VIH and VIL.
5. Voutref is a reference level for measuring of timing of output signals.
6.



[PART2] Asynchronous Parameters like conventional DRAMs.[1,2,3,4]

#	Symbol	Parameter	-10		-12		-15		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
1	tRC	Normal/Refresh cycle Time	100	-	108	-	120	-	ns	
2	tRCD	/RAS -to- /CAS delay Time	30	-	36	-	45	-	ns	3Clk
3	tRAS	Bank Active Time	60	10K	70	10K	80	10K	ns	
4	tRASP	Bank Active Time(full page)	60	400K	70	400K	80	400K	ns	
5	tRP	Bank Precharge Time	30	-	36	-	45	-	ns	
6	tRRD	Bank Active-to-Active Time	20	-	24	-	30	-	ns	
7	tWR	Write Recovery Time	10	-	12	-	15	-	ns	
8	tSRE	Self-Refresh Exit Time	10	-	12	-	15	-	ns	1Clk
9	tT	Transition Time	1	5	1	5	1	5	ns	
10	tPDE	Power Down Exit Time	3	-	4	-	5	-	ns	
11	tREF	Refresh Period	-	64	-	64	-	64	ms	

Notes:

1. An initial pause of 200μS is required after power-up by `Power On Sequence`(JEDEC Standard.) and Auto Refresh before proper device operation is achieved.
2. AC measurements assume tT=1ns
3. (VIH+VIL)/2 is a reference level for measuring of timing of input signals. Also transition time is measured between VIH and VIL.
4. Voutref is a reference level for measuring of timing of output signals.

[PART3] Latency - Fixed Parameters[1]

#	Symbol	Parameter		-10	-12	-15	Unit	Note
				Lat.	Lat.	Lat.		
1	tCKED	CKE to CLK Suspend or Power Down Mode Entry		1	1	1	Clk(s)	
2	tDQMOZ	DQM to Data Output in Hi-Z		2	2	2	Clk(s)	
3	tDQMIM	DQM to Data Input Mask		0	0	0	Clk(s)	
4	tWTL	Write command to Data Input Valid		0	0	0	Clk(s)	2
5	tPROZ	Precharge to Data Output in Hi-Z delay	/CAS Lat.=1	1	1	1	Clk(s)	
			/CAS Lat.=2	2	2	2	Clk(s)	
			/CAS Lat.=3	3	3	3	Clk(s)	
6	tMRD	Mode Register Set to Bank Active		2	2	2	Clk(s)	
7	tCCD	/CAS -to- /CAS command delay		1	1	1	Clk(s)	3

Notes :

1. The latency values in the above table are fixed regardless of clock cycle time.
2. `Write Latency` as JEDEC standard says.
3. Superset of `2N-rule`.

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	Opcode	0	0	/CAS Latency			BT	Burst Length		

A3	Burst Type
0	Sequential
1	Interleaved

A6	A5	A4	/CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length	Remark
0	0	0	1	Used
0	0	1	2	Used
0	1	0	4	Used
0	1	1	8	Used
1	0	0	16	Reserved
1	0	1	32	Reserved
1	1	0	64	Reserved
1	1	1	Full Page	Used[1]

Note : 1. Full page burst supports only sequential type.

TEST MODE

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
X	X	X	X	1	X	X	X	X	X	X	X	Refresh Counter Test

Note: Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using `Precharge All bank`.

PACKAGE DIMENSION