HYM536810E M1-Series

8Mx36 bit FP DRAM MODULE
based on 4Mx4 DRAM, with Parity, 5V, 2K-Refresh

GENERAL DESCRIPTION

The HYM536810E M1-Series is a 8Mx36-bit Fast Page mode CMOS DRAM module consisting of sixteen HY5117400C in 24/26 pin SOJ and eight HY514100A in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. 0.1µF and 0.01µF decoupling capacitors are mounted for each DRAM.
The HYM536810EM1 is Tin plated and HYM536810EMG1 is Gold plated socket type Single In-line Memory Module suitable for easy interchange and addition of 32M byte memory.

FEATURES

- 72-Pin SIMM
- Fast Page Mode Operation
- /CAS-before-/RAS, /RAS-only, Hidden refresh capability
- 2048 refresh cycles / 256ms (L-part)
  2048 refresh cycles / 32ms
- Fast access time and cycle time

Speed	tRAC	tCAC	tPC
50	50ns	15ns	35ns
60	60ns	15ns	40ns
70	70ns	18ns	45ns

- TTL compatible inputs and outputs
- JEDEC standard pinout
- Single power supply of 5.0V ± 10%
- Low power dissipation

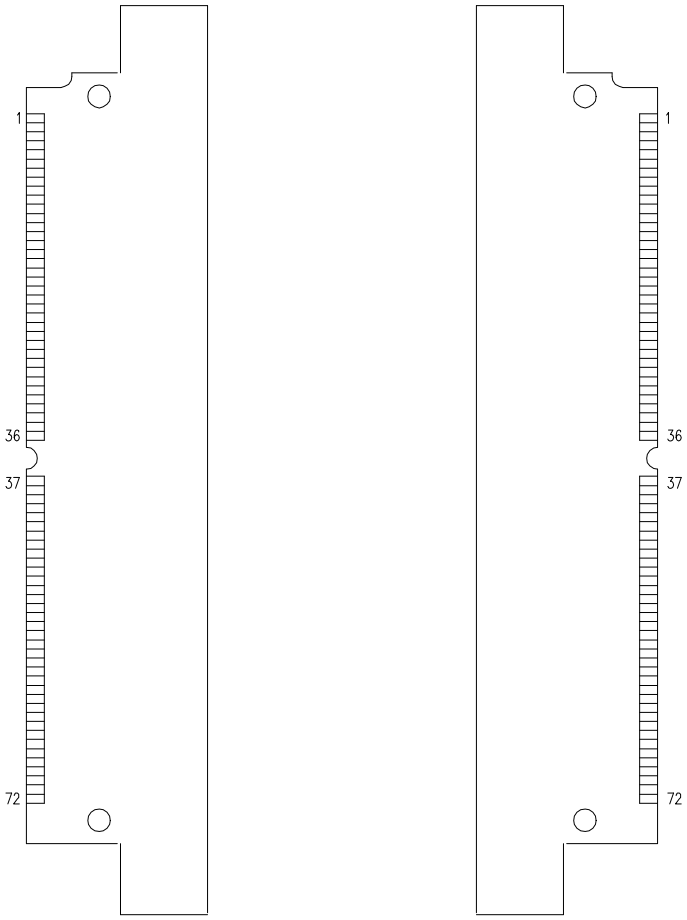
  Max. battery back-up : 61.6mW (L-part)
  Max. CMOS standby : 35.2mW (L-part)
  132mW
  Max. TTL standby : 264mW
  Max. operating

Speed	Power
50	9.26W
60	7.83W
70	6.62W

ORDERING INFORMATION

PART NUMBER	SPEED	FEATURES	PACKAGE	PLATING
HYM536810EM1	50/60/70	FP, 2K, 5V, SOJ	SIMM	Tin
HYM536810EMG1	50/60/70	FP, 2K, 5V, SOJ	SIMM	Gold

PIN CONNECTION



PIN DISCRIPTION

/RAS0~/RAS3	Row Address Strobe
/CAS0~/CAS3	Column Address Strobe
/WE	Write Enable
A0~A10	Address Input
DQ0~DQ35	Data Input/Output
PD1~PD4	Presence Detect
VCC	Power (+5V)
VSS	Ground

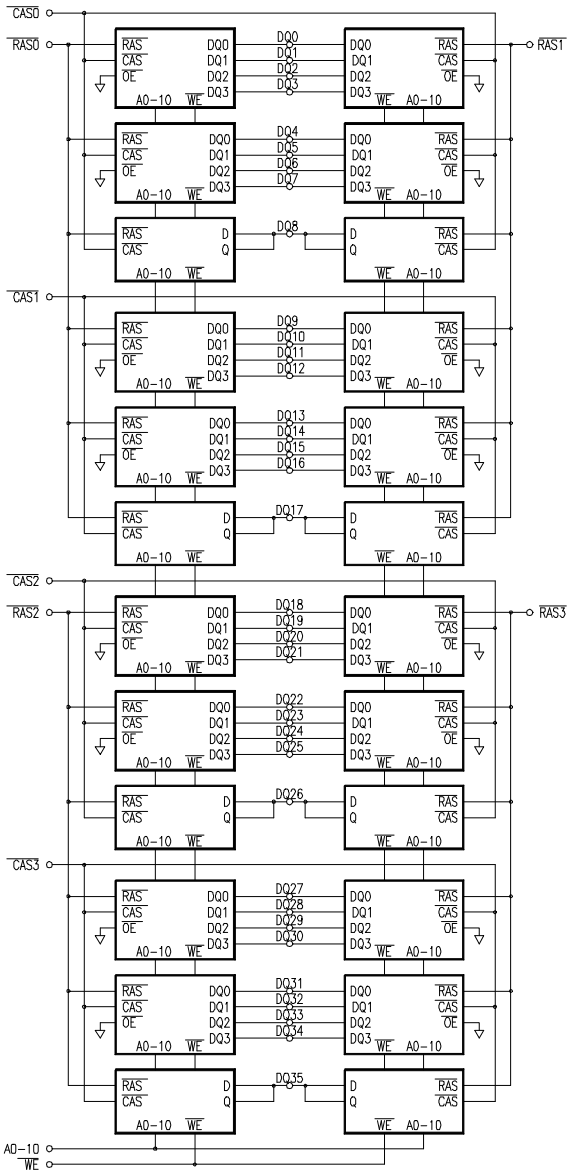
PIN ASSIGNMENTS

#	NAME	#	NAME
1	VSS	37	DQ17
2	DQ0	38	DQ35
3	DQ18	39	VSS
4	DQ1	40	/CAS0
5	DQ19	41	/CAS2
6	DQ2	42	/CAS3
7	DQ20	43	/CAS1
8	DQ3	44	/RAS0
9	DQ21	45	/RAS1
10	VCC	46	NC
11	NC	47	/WE
12	A0	48	NC
13	A1	49	DQ9
14	A2	50	DQ27
15	A3	51	DQ10
16	A4	52	DQ28
17	A5	53	DQ11
18	A6	54	DQ29
19	A10	55	DQ12
20	DQ4	56	DQ30
21	DQ22	57	DQ13
22	DQ5	58	DQ31
23	DQ23	59	VCC
24	DQ6	60	DQ32
25	DQ24	61	DQ14
26	DQ7	62	DQ33
27	DQ25	63	DQ15
28	A7	64	DQ34
29	NC	65	DQ16
30	VCC	66	NC
31	A8	67	PD1
32	A9	68	PD2
33	/RAS3	69	PD3
34	/RAS2	70	PD4
35	DQ26	71	NC
36	DQ8	72	VSS

PRESENCE DETECT PINS

Speed	PD1	PD2	PD3	PD4
50	NC	VSS	VSS	VSS
60	NC	VSS	NC	NC
70	NC	VSS	VSS	NC

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	23.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

DC CHARACTERISTICS

(T_A=0°C to 70°C, VCC=5.0V ± 10% and VSS=0V, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current 2K Ref	UNIT
ICC1	Operating Current	/RAS and /CAS cycling tRC=tRC (min.)	50 60 70	1680 1420 1200	mA
ICC2	TTL Standby Current	/RAS=/CAS ≥ VIH other inputs ≥ VSS		48	mA
ICC3	/RAS-only Refresh Current	/CAS=VIH, /RAS cycling tRC=tRC (min.)	50 60 70	1680 1420 1200	mA
ICC4	Fast Page Mode Current	/RAS=VIL, /CAS, Address cycling tPC=tPC (min.)	50 60 70	1040 920 800	mA
ICC5	CMOS Standby Current	/RAS = /CAS ≥ VCC-0.2V	 L-part	24 6.4	mA mA
ICC6	/CAS-before-/RAS Refresh Current	/RAS and /CAS cycling tRC=tRC (min.)	50 60 70	1680 1420 1200	mA
ICC7	Battery Back-up Current (L-part)	tRC = 125µs /CAS = CBR cycling or 0.2V /OE & /WE = VCC - 0.2V Address = VCC-0.2V or 0.2V DQ = VCC-0.2V, 0.2V or open	tRAS ≤ 300ns	7.2	mA
			tRAS ≤ 1µs	11.2	mA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
ILI	Input Leakage current (Any Input)	VSS ≤ VIN ≤ VCC + 1.0 All other pins not under test = VSS	-240	240	µA
ILO	Output Leakage current (Any Input)	VSS ≤ VOUT ≤ VCC /RAS & /CAS at VIH	-20	20	µA
VOL	Output Low Voltage	IOL = 4.2mA	-	0.4	V
VOH	Output High Voltage	IOH = -5.0mA	2.4	-	V

NOTE

1. ICC1, ICC3, ICC4 and ICC6 depend on output loading and cycle rates(tRC and tPC).
2. Specified values are obtained with outputs unloaded.
3. ICC is specified as an average current. In ICC1, ICC3, ICC6, address can be changed only once while /RAS=VIL. In ICC4, address can be changed maximum once while /CAS=VIH within one Fast Page mode cycle time tPC.
4. Only /RAS(max.) = 1µs is applied to refresh of battery backup but tRAS(max.) = 10µs is applied to normal functional operation.
5. ICC5(max.) = 6.4mA and ICC7 are applied to L-part only.

AC CHARACTERISTICS

(T_A=0°C to 70°C, VCC=5.0V ± 10% and VSS=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM536810E M1-Series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	90	-	110	-	130	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	140	-	160	-	180	-	ns	
3	tPC	Fast Page Mode Cycle Time	35	-	40	-	45	-	ns	
4	tPRWC	FP Mode Read-Modify-Write Cycle Time	61	-	70	-	78	-	ns	
5	tRAC	Access Time from /RAS	-	50	-	60	-	70	ns	4,5,6
6	tCAC	Access Time from /CAS	-	15	-	15	-	20	ns	4,5
7	tAA	Access Time from Column Address	-	25	-	30	-	35	ns	4,6
8	tCPA	Access Time from Column Precharge	-	30	-	35	-	40	ns	4
9	tCLZ	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Out Buffer Turn-Off Delay Time from /CAS	0	10	0	13	0	20	ns	7
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	2
12	tRP	/RAS Precharge Time	30	-	40	-	50	-	ns	
13	tRAS	/RAS Pulse Width	50	10K	60	10K	70	10K	ns	
14	tRASP	/RAS Pulse Width (Fast Page Mode)	50	200K	60	200K	70	200K	ns	
15	tRSH	/RAS Hold Time	15	-	15	-	20	-	ns	
16	tCSH	/CAS Hold Time	50	-	60	-	70	-	ns	
17	tCAS	/CAS Pulse Width	15	10K	15	10K	20	10K	ns	
18	tRCD	/RAS to /CAS Delay Time	18	37	20	45	20	52	ns	5
19	tRAD	/RAS to Column Address Delay Time	10	25	15	30	15	35	ns	6
20	tCRP	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	10
21	tCP	/CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tRAL	Column Address to /RAS Lead Time	25	-	30	-	35	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	tRCH	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	8
29	tRRH	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	8
30	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
31	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
32	tRWL	Write Command to /RAS Lead Time	15	-	15	-	20	-	ns	
33	tCWL	Write Command to /CAS Lead Time	15	-	15	-	20	-	ns	

AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HYM536810E M1-Series						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	9
35	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	9
36	tREF	Refresh Period (2048 cycles)	-	32	-	32	-	32	ms	
		Refresh Period (L-part)	-	256	-	256	-	256	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	9,10
38	tCWD	/CAS to /WE Delay Time	33	-	38	-	43	-	ns	10
39	tRWD	/RAS to /WE Delay Time	70	-	83	-	95	-	ns	10
40	tAWD	Column Address to /WE Delay Time	45	-	53	-	60	-	ns	10
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	9
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	9
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	9
44	tCPT	/CAS Precharge Time (CBR Counter Test)	25	-	30	-	35	-	ns	
45	tCPWD	/WE Delay Time from /CAS Precharge	47	-	54	-	62	-	ns	10
46	tRHCP	/RAS Hold Time from /CAS Precharge	30	-	35	-	40	-	ns	
47	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
48	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	

NOTE

1. An initial pause of 200μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.)
3. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70°C) is assured.
4. Measured at VOH=2.4V and VOL=0.4V with a load equivalent to 2 TTL loads and 100pF.
5. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC
6. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA
7. tOFF(max.), tOEZ(max.) define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
8. Either tRCH or tRRH must be satisfied for a read cycle..
9. These parameters are referred to /CAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
10. tWCS, tRWD, tCWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≥ tWCS(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If tCWD ≥ tCWD(min.), tRWD ≥ tRWD(min.) and tCPWD ≥ tCPWD(min.), then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.

CAPACITANCE

(T_A=25°C, VCC=5.0V ± 10%, VSS=0V and f = 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0~A10)	-	144	pF
CIN2	Input Capacitance (/RAS0~/RAS3)	-	54	pF
CIN3	Input Capacitance (/CAS0~/CAS3)	-	54	pF
CIN4	Input Capacitance (/WE)	-	172	pF
CDQ	Data Input /Output Capacitance (DQ0~DQ35)	-	24	pF

PACKAGE INFORMATION

72 pin Single In-line Memory Module (SOJ Mounted)