16Mx72 bit SDRAM Unbuffered DIMM F-Series

based on 8Mx8 SDRAM, LVTTL, 2/4-Banks & 4K/8K-Refresh

HYM7V72A1600/ HYM7V72A1601/ HYM7V72A1630/ HYM7V72A1631

DESCRIPTION

The HYM7V72A1600/ 72A1601/ 72A1630/ 72A1 631 F-Series are high speed 3.3-Volt synchronous dynamic RAM Modules composed of eighteen 8Mx8 bit Synchronous DRAMs in 54-pin TSOPII and 8-pin TSSOP 2K bit E^2PROM on a 168-pin glass-epoxy printed circuit board. Two 0.22μF and two 0.0022μF decoupling capacitors per each SDRAM are mounted on the module.

The HYM7V72A1600/ 72A1601/ 72A1630/ 72A1631 F-Series are gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 128M bytes memory. All addresses, data and control inputs are latched on the rising edge of the master clock input. The data paths are internally pipe-lined to achieve very high bandwidths.

FEATURES

- 168-Pin Unbuffered DIMM with ECC
- Serial Presence Detect with Serial E^2PROM
- Meets all the other JEDEC specifications
- Single 3.3V±0.3V power supply
- All device pins are LVTTL compatible
- 4096 refresh cycles every 64ms or 8192 refresh cycles every 128ms
- Fully synchronous ; all inputs referenced to positive edge of system clock
- Dual or Quad internal banks with single pulsed /RAS
- Auto precharge/precharge all banks by A10 flag
- Possible to assert random column address every clock cycle
- Interleaved auto refresh mode
- Programmable burst lengths and sequences
  - 1,2,4,8,full page for Sequential type
  - 1,2,4,8 for Interleave type
- Programmable /CAS latency ; 1,2,3 clocks
- Support clock suspend/power down mode by CKE0, CKE1
- Data mask function by DQM
- Mode register set programming
- Burst termination command
- Self refresh provides minimum power, full internal refresh control

ORDERING INFORMATION

Part No.	Max. Frequency	SDRAM Bank	Refresh	Package	Plating
HYM7V72A1600TFG - 10/12/15	100/ 83/ 66 MHz	2 Banks	4K	TSOP	Gold
HYM7V72A1601TFG - 10/12/15	100/ 83/ 66 MHz	4 Banks	4K	TSOP	Gold
HYM7V72A1630TFG - 10/12/15	100/ 83/ 66 MHz	2 Banks	8K	TSOP	Gold
HYM7V72A1631TFG - 10/12/15	100/ 83/ 66 MHz	4 Banks	8K	TSOP	Gold

PIN DESCRIPTION

Pin Name	Pin Type	Description
CK0-CK3	INPUT	System Clock Input; All other inputs except CKE are registered to the SDRAM on the rising edge of CLK.
CKE0, CKE1	INPUT	Clock Enable; Controls internal clock signal and when deactivated, the SDRAM will be either one of the states among power down, suspend, or self refresh.
/S0-/S3	INPUT	Chip select; Functions command mask(NOP).
/RAS	INPUT	Row address strobe; See functional truth table in 8Mx8 Data Sheets for details.
/CAS	INPUT	Column address strobe; See functional truth table in 8Mx8 Data Sheets for details.
/WE	INPUT	Write Enable; See functional truth table in 8Mx8 Data Sheets for details.
DQM0-7	INPUT	Data Input / Output Mask
DQ0-DQ63	INPUT/ OUTPUT	Data Input / Output; Include inputs, outputs, or Hi-z state.
CB0-CB7	INPUT/ OUTPUT	Check Bit Input / Output; Include inputs, outputs, or Hi-z state.
V_{CC}	SUPPLY	Power Supplies; 3.3V±0.3V
V_{SS}	SUPPLY	Ground
SDA	INPUT/ OUTPUT	Serial Address and Data Input / Output.
SCL	INPUT	Serial Clock
SA0-SA2	INPUT	Addresses in Serial E^2PROM for Socket Presence.

HYM7V72A1600/HYM7V72A1630 F-Series (2Bank 8Mx8 SDRAM Based)

Pin Name	Pin Type	Description
BA0	INPUT	Bank select address inputs; Select one of dual banks during both /RAS and /CAS activity.
A0-A12	INPUT	Address Inputs; A0-A8; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A9-A12; X addresses only.

HYM7V72A1601/HYM7V72A1631 F-Series (4Bank 8Mx8 SDRAM Based)

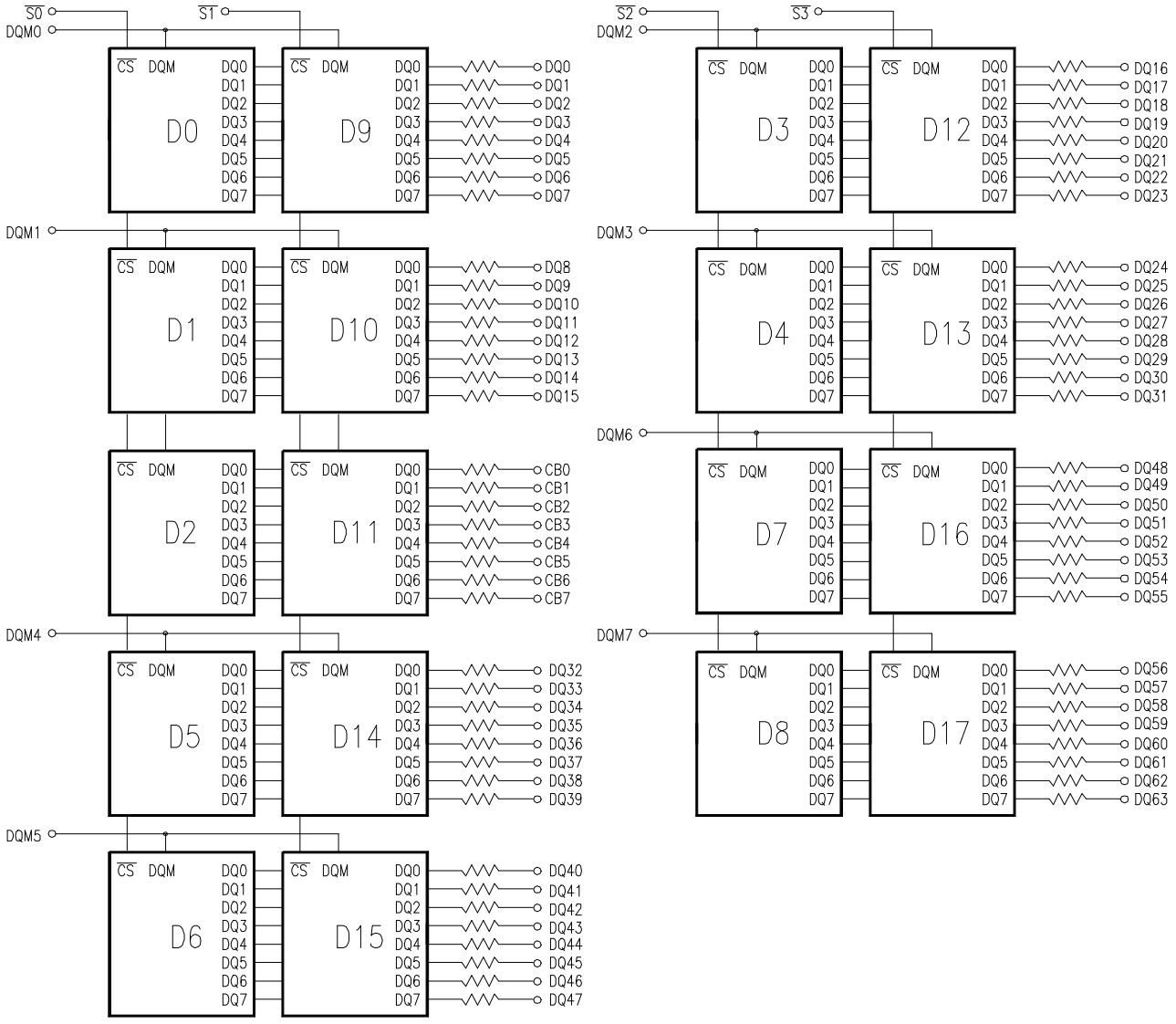
Pin Name	Pin Type	Description
BA0, BA1	INPUT	Bank address inputs; Select one of quad banks during both /RAS and /CAS activity.
A0-A11	INPUT	Address Inputs; A0-A8; X&Y addresses, A0-A13; Opcode for mode register set, A10; Precharge flag, A9-A11; X addresses only.

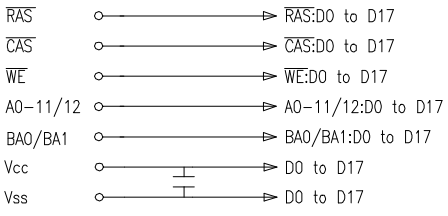
PIN NAME

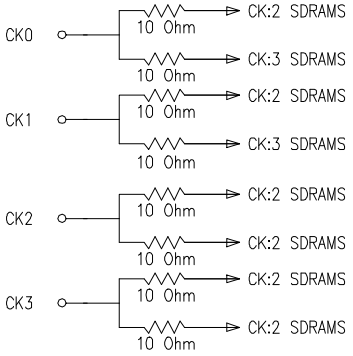
#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	/S2	87	DQ33	129	/S3
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	Vcc	48	DU	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	VREF, NC	104	DQ47	146	VREF, NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	/WE	69	DQ24	111	/CAS	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	/S0	72	DQ27	114	/S1	156	DQ59
31	DU	73	Vcc	115	/RAS	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10(AP)	80	NC	122	BA0	164	NC
39	* BA1	81	NC	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	* A12	168	Vcc

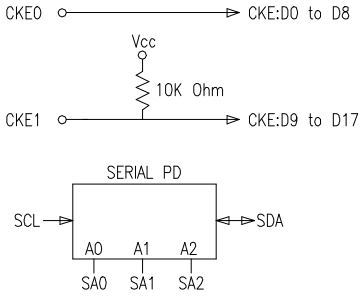
Note : 1. BA1 is used for HYM7V72A1601/HYM7V72A1631 F-Series (4 Bank 8Mx8 Based)
2. A12 is used for HYM7V72A1600/HYM7V72A1630 F-Series (2 Bank 8Mx8 Based)

BLOCK DIAGRAM









Note : 1. The serial resistor values of DQs are 10 Ohms.

I-1 SERIAL PRESENCE DETECT

[HYM7V72A1600/HYM7V72A1630 F-Series; 2 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	2 Banks; 13	0Dh	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	2 Banks	02h	
BYTE6	Data Width of This Assembly	72 Bits	48h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	tCLK (A) 10ns (B) 12ns (C) 15ns	 (A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	tAC (A) 8ns (B) 9ns (C) 10ns	 (A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	ECC	02h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	x8	08h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 2 Bank 8Mx8 Based	 2 Banks	 02h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	tCLK (A) 12ns (B) 15ns (C) 15ns	 (A) C0h (B) F0h (C) F0h	3

I-2 SERIAL PRESENCE DETECT [HYM7V72A1600/HYM7V72A1630 F-Series; 2Banks: Continued]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	 (A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCLK (A) 30ns (B) 30ns (C) 30ns	 (A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	 (A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	 (A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	 (A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	64MB	10h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	 (A) Decimal 5 (B) Decimal 105 (C) Decimal 206	 (A) 05h (B) 69h (C) CEh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

Note : 1. The bank address is excluded.
2. In interleaved type. the burst lengths supported is 1,2,4,8.
3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
* All above data can be changed, if the JEDEC standard is modified.

II-1 SERIAL PRESENCE DETECT

[HYM7V72A1601/HYM7V72A1631 F-Series; 4 Banks]

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE0	# of Bytes Written into Serial Memory at Module Manufacturer	128 Bytes	80h	
BYTE1	Total # of Bytes of SPD Memory Device	256 Bytes	08h	
BYTE2	Fundamental Memory Type	SDRAM	04h	
BYTE3	# of Row Addresses on This Assembly	4 Banks; 12	0Ch	1
BYTE4	# of Column Addresses on This Assembly	9	09h	
BYTE5	# of Module Banks on This Assembly	2 Banks	02h	
BYTE6	Data Width of This Assembly	72 Bits	48h	
BYTE7	Data Width of This Assembly(Continued)	-	00h	
BYTE8	Voltage Interface Standard of This Assembly	LVTTL	01h	
BYTE9	SDRAM Cycle Time @ /CAS Latency=3	tCLK (A) 10ns (B) 12ns (C) 15ns	 (A) A0h (B) C0h (C) F0h	3
BYTE10	SDRAM Access Time from Clock @ /CAS Latency=3, @Cycle Time=10ns @ /CAS Latency=3, @Cycle Time=12ns @ /CAS Latency=3, @Cycle Time=15ns	tAC (A) 8ns (B) 9ns (C) 10ns	 (A) 80h (B) 90h (C) A0h	3
BYTE11	DIMM Configuration Type	ECC	02h	
BYTE12	Refresh Rate/Type	15.625µs / Self Refresh Supported	80h	
BYTE13	Primary SDRAM Width	x8	08h	
BYTE14	Error Checking SDRAM Width	x8	08h	
BYTE15	Minimum Clock Delay Back to Back Random Column Address	tCCD=1 Latency	01h	
BYTE16	Burst Lengths Supported	1,2,4,8,Full Page	8Fh	2
BYTE17	# of Banks on SDRAM Device 4 Bank 8Mx8 Based	 4 Banks	 04h	
BYTE18	CAS # Latency	/CAS Latency=1,2,3	07h	
BYTE19	CS # Latency	/CS Latency=0	01h	
BYTE20	Write Latency	/WE Latency=0	01h	
BYTE21	SDRAM Module Attributes (Neither Buffered nor Registered)	-	00h	
BYTE22	SDRAM Module Attributes General (Burst read, Precharge All, Auto Precharge)	-	06h	
BYTE23	SDRAM Cycle Time @ /CAS Latency=2	tCLK (A) 12ns (B) 15ns (C) 15ns	 (A) C0h (B) F0h (C) F0h	3

II-2 SERIAL PRESENCE DETECT(HYM7V72A1601/HYM7V72A1631 F-Series; 4Banks:Continued)

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE	NOTE
BYTE24	SDRAM Access Time from Clock @ /CAS Latency=2, @Cycle Time=12ns @ /CAS Latency=2, @Cycle Time=15ns @ /CAS Latency=2, @Cycle Time=15ns	tAC (A) 9ns (B) 9ns (C) 10ns	 (A) 90h (B) 90h (C) A0h	3
BYTE25	SDRAM Cycle Time @ /CAS Latency=1	tCLK (A) 30ns (B) 30ns (C) 30ns	 (A) 78h (B) 78h (C) 78h	3
BYTE26	SDRAM Access Time from Clock @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns @ /CAS Latency=1, @Cycle Time=30ns	tAC (A) 24ns (B) 24ns (C) 24ns	 (A) 60h (B) 60h (C) 60h	3
BYTE27	Minimum Row Pre-charge Time @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRP (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE28	Minimum Row Active to Row Active Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRRD (A) 30ns (B) 24ns (C) 30ns	 (A) 1Eh (B) 18h (C) 1Eh	3
BYTE29	Minimum /RAS to /CAS Delay @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRCD (A) 30ns (B) 36ns (C) 45ns	 (A) 1Eh (B) 24h (C) 2Dh	3
BYTE30	Minimum /RAS Pulse width @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	tRAS (A) 50ns (B) 48ns (C) 45ns	 (A) 32h (B) 30h (C) 2Dh	3
BYTE31	Module Bank Density	64MB	10h	
BYTE32-61	Superset Information (May Be Used in the Future)	-	00h	
BYTE62	SPD Revision	-	01h	
BYTE63	Checksum for Byte 0-62 @/CAS Latency=3, @Cycle Time=10ns @/CAS Latency=3, @Cycle Time=12ns @/CAS Latency=3, @Cycle Time=15ns	 (A) Decimal 6 (B) Decimal 106 (C) Decimal 207	 (A) 06h (B) 6Ah (C) CFh	3
BYTE64-127	Manufacturer Information	-	-	
BYTE128-255	Unused Storage Locations	Undefined	Undefined	

Note : 1. The bank address is excluded.
2. In interleaved type. the burst lengths supported is 1,2,4,8.
3. In case of (A): 10ns, (B): 12ns, and (C): 15ns part.
* All above data can be changed, if the JEDEC standard is modified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin relative to V_{SS}	-1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	-1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	18	W
T_{SOLDER}	Soldering Temperature·Time	260·10	°C·sec

Note : Operation at above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS*

(T_A=0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V_{CC}	Power Supply Voltage	3.0	3.3	3.6	V	
Vss	Power Supply Voltage	0	0	0	V	
V_{IH}	Input High Voltage	2.0	-	V_{CC} + 0.4	V	LVTTL
V_{IL}	Input Low Voltage	-0.3	-	0.8	V	LVTTL

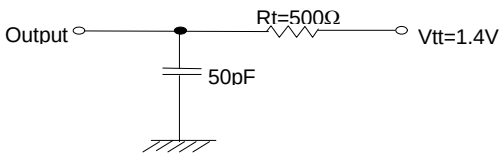
RECOMMENDED AC OPERATING CONDITIONS*

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

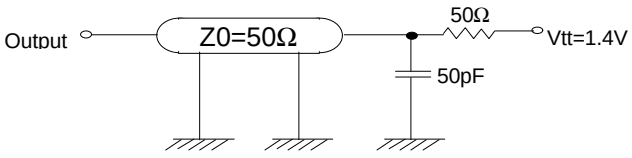
Symbol	Parameter	Value	Unit	Note
V_{IH} / V_{IL}	AC Input High/Low Level Voltage	2.4/0.4	V	LVTTL
Vtrip	Input Timing Measurement Reference Level Voltage	1.4	V	LVTTL
tr / tf	Input Rise/Fall Time	1	ns	
Voutref	Output Reference Voltage	1.4	V	LVTTL
C_L	Output Load Capacitance for Access Time Measurement	Note	pF	

Note : Output load to measure access times is equivalent to two TTL gates and one capacitance(50pF).

Note : * DC Output Load Circuit



AC Output Load Circuit



DC CHARACTERISTICS(I)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition	Min.	Max.	Unit	Note
I_{LI}	Input Leakage Current	V_I=0 to 3.6V, All other pins not undertest=0V	-18	18	μA	
I_{LO}	Output Leakage Current	D_{OUT} is disabled, V_O=0 to 3.6V	-2	2	μA	
V_{OL}	Output Low Voltage	I_O=2.0mA	-	0.4	V	LVTTL
V_{OH}	Output High Voltage	I_O=-2.0mA	2.4	-	V	LVTTL

DC CHARACTERISTICS(II)

(T_A=0°C to 70°C, V_{CC}=3.3V±10%, V_{SS}=0V)

Symbol	Parameter	Test Condition		Max.	Unit	Note
I_{CC1}	Operating current	Burst Length=1, One bank active t_{RAS}≥t_{RAS}(min), t_{RP}≥t_{RP}(min), I_O=0mA	10ns	1080	mA	Note 2
			12ns	945		
			15ns	855		
I_{CC2P}	Precharge Standby Current in Power Down Mode	CKE≤V_{IL}(max)		36	mA	
I_{CC2N}	Precharge Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{CC}-0.2V or ≤0.2V		216	mA	LVTTL[1]
I_{CC3P}	Active Standby Current in Power Down Mode	CKE≤V_{IL}(max), All banks active		54	mA	
I_{CC3N}	Active Standby Current in Non Power Down Mode	CKE≥V_{IH}(min), All other pins≥V_{CC}-0.2V or ≤0.2V All banks active		630	mA	LVTTL[1]
I_{CC4}	Operating Current (Burst Mode)	t_{CLK}≥t_{CLK}(min), t_{RAS}≥t_{RAS}(min), I_O=0mA, /CAS Latency=3	10ns	1665	mA	Note 2
			12ns	1395		
			15ns	1215		
I_{CC5}	Refresh Current	t_{RC}≥t_{RC}(min), Two banks active (8K/128ms)	10ns	1980	mA	Note 2
			12ns	1620		
			15ns	1350		
		t_{RC}≥t_{RC}(min), Four banks active (4K/64ms)	10ns	2880	mA	Note 2
			12ns	2340		
			15ns	1890		
I_{CC6}	Self Refresh Current	CKE≤0.2V		36 9	mA	L-part

Note :

1. It depends on the number of each pin's transition. It is assumed there is no transition to measure this current.
2. I_{CC1} depends on output loads and cycle rates. Specified values are obtained with the output open. In addition this I_{CC1} is measured on condition that addresses are changed only one time during t_{CLK}(Min.)

AC CHARACTERISTICS

Synchronous Characteristics(I)

Parameter	100MHz (10ns)			83MHz (12ns)			66MHz (15ns)			Unit
/CAS Latency	3	2	1	3	2	1	3	2	1	Latency
Frequency	100	83	33	83	66	33	66	66	33	MHz
Clock Cycle Time	10	12	30	12	15	30	15	15	30	ns
t_{RCD}	3	2	1	3	2	1	3	2	1	CLK(s)
t_{RAS}	5	4	2	4	4	2	3	4	2	CLK(s)
t_{RP}	3	3	1	3	2	1	3	2	1	CLK(s)
t_{RC}	8	7	3	7	6	3	-	6	3	CLK(s)
t_{RRD}	3	2	1	2	2	2	2	2	2	CLK(s)
t_{DPL}	1	1	1	1	1	1	-	1	1	CLK(s)
t_{DAL}	4	3	2	3	3	2	-	3	2	CLK(s)
t_{SRE}	1	1	1	1	1	1	-	1	1	CLK(s)
t_T	1			1			1			ns
Refresh Cycle	8K/128ms, 4K/64ms									Cycles
Asynchronous Characteristic	50ns Part									ns

Note : t_{RRD} -Bank Active to Active Command
t_{DPL} -D_{IN} to Precharge Command
t_{DAL} -D_{IN} to Active(Ref.) Command (After Write with Autoprecharge)
t_{SRE} -Self Refresh Exit Time

Synchronous Characteristics(II)

Symbol	Parameter		-10		-12		-15		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{AC}	Access Time from CLK	/CAS Lat.=3	-	8	-	9	-	10	ns	
		/CAS Lat.=2	-	9	-	9	-	10	ns	
		/CAS Lat.=1	-	24	-	24	-	24	ns	
t_{CH}	CLK High Level Width		3.5	-	3.5	-	3.5	-	ns	
t_{CL}	CLK Low Level Width		3.5	-	3.5	-	3.5	-	ns	
t_{OH}	Data-out Hold Time		3	-	3	-	3	-	ns	
t_{OLZ}	Data-out Low-Impedance Time		3	-	3	-	3	-	ns	
t_{OHZ}	Data-out High-Impedance Time		0	8	0	9	0	10	ns	
t_{DS}	Data-in Set-up Time		3	-	3	-	3	-	ns	
t_{DH}	Data-in Hold Time		1	-	1	-	1	-	ns	
t_{AS}	Address Set-up Time		3	-	3	-	3	-	ns	
t_{AH}	Address Hold Time		1	-	1	-	1	-	ns	
t_{CKS}	CKE Set-up Time		3	-	3	-	3	-	ns	
t_{CKH}	CKE Hold Time		1	-	1	-	1	-	ns	
t_{CS}	Command Set-up Time		3	-	3	-	3	-	ns	
t_{CH}	Command Hold Time		1	-	1	-	1	-	ns	
t_{PDE}	Power Down Exit Set-up Time		3	-	3	-	3	-	ns	

Latency

Symbol	Parameter		Latency
t_{CKED}	CKE to CLK Suspend / Power Down Mode Entry		1
t_{DQMOZ}	DQM to Data Output in Hi-z		2
t_{DQMIM}	DQM to Data Input Mask		0
t_{WTL}	Write Command to Data Input Valid		0
t_{PROZ}	Precharge Command to Data Output in Hi-z	/CAS Latency=1	1
		/CAS Latency=2	2
		/CAS Latency=3	3
t_{MRD}	Mode Register Set to New Command		1
t_{CCD}	Min. Column Address to Column Address Delay		1
t_{PPD}	Min. Precharge to Precharge Time		1

Note :
1. All voltages referenced V_{SS}(Ground).
2. An initial pause of 100μS is required after power-on followed by Power On Sequence & Auto Refresh before proper device operation is achieved.
3. AC measurements assume t_T=1ns.
4. Reference level for measuring timing of input signals is 1.40V for LVTTL
   Transition times are measured between V_{IH} and V_{IL}.
5. An access time is measured at 1.40V for LVTTL

CAPACITANCE

(T_A=25°C, f=1MHz)

Symbol	Parameter	Pin	Typ.	Max.	Unit
C_{IN1}	Input Capacitance	A0-A11/12, BA0/BA1	-	105	pF
C_{IN2}	Input Capacitance	/RAS, /CAS, /WE	-	105	pF
C_{IN3}	Input Capacitance	/S0-/S3	-	35	pF
C_{IN4}	Input Capacitance	CK0-CK3	-	40	pF
C_{IN5}	Input Capacitance	CKE0, CKE1		55	pF
C_{IN6}	Input Capacitance	DQM0-DQM7	-	25	pF
C_{OUT}	Output Capacitance	DQ0-DQ63,CB0-CB7	-	20	pF

PROGRAMMABLE MODE REGISTER

MODE REGISTER SET(WRITE)

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	/CAS Latency			BT	Burst Length		

A3	Burst Type
0	Sequential (Wrap round, Binary-up)
1	Interleave (Wrap round)

A6	A5	A4	/CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	Burst Length
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Full page[1]

Note : 1. Full page burst supports only sequential type.

TEST MODE

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Address
0	0	0	0	1	X	X	X	X	X	X	X	Refresh Counter Test

Note : Test Mode - Used to test the counter of Auto Refresh.
- Exit test mode using 'Precharge All banks'.

BURST LENGTH AND SEQUENCE

Burst Length	Initial Address	Burst Type	
	A2 A1 A0	Sequential	Interleave
2	X X 0	0,1	0,1
	X X 1	1,0	1,0
4	X 0 0	0,1,2,3	0,1,2,3
	X 0 1	1,2,3,0	1,0,3,2
	X 1 0	2,3,0,1	2,3,0,1
	X 1 1	3,0,1,2	3,2,1,0
8	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0 0 1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0 1 0	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0 1 1	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	1 0 1	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	1 1 0	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	1 1 1	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Full page	Note	0,1,2,3,4,……,m 1,2,3,4,5,……,0 : : m,0,1,2,3,……,m-1	Not supported

Table 1. Address sequence for different burst lengths

Note : 4Mbit x 2banks x 8I/O - Initial addresses: A8-A0, Page length: 1024, m=1023
2Mbit x 4banks x 8I/O - Initial addresses: A8-A0, Page length: 1024, m=1023

PACKAGE DIMENSION