TOSHIBA Field Effect Transistor Silicon N·P Channel MOS Type

HN1L03FU

High Speed Switching Applications Analog Switch Applications

Unit in mm

Q1, Q2 common

Low threshold voltage

Q1:
$$V_{th} = 0.8 \sim 2.5 V$$
 Q2: $V_{th} = -0.5 \sim -1.5 V$

- High speed
- Small package

Q1 Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	50	V
Gate-Source voltage	V _{GSS}	10	V
Drain current	I _D	50	mA

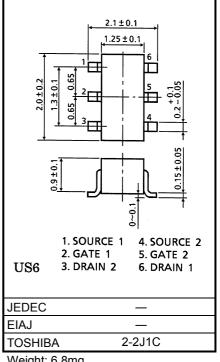
Q2 Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	-20	V
Gate-Source voltage	V_{GSS}	-7	V
Drain current	I _D	-50	mA

Maximum Ratings (Q1, Q2 Common) (Ta = 25°C)

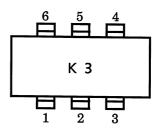
Characteristic	Symbol	Rating	Unit
Drain power dissipation	P _{D*}	200	mW
Channel temperature	T _{ch}	150	°C
Storage temperature range	T _{stg}	-55~150	°C

Total rating

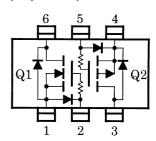


Weight: 6.8mg

Marking



Equivalent Circuit (Top View)



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damage to property.

In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..

TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or



Q1 Electrical Characteristics (Ta = 25°C)

Chara	cteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	rrent	I _{GSS}	V _{GS} = 10V, V _{DS} = 0	_	_	1	μΑ
Drain-Source brevoltage	eakdown	V (BR) DSS	I _D = 100μA, V _{GS} = 0	50	_	_	V
Drain cut-off cur	rent	I _{DSS}	V _{DS} = 50V, V _{GS} = 0	_	_	1	μA
Gate threshold v	oltage	V _{th}	V _{DS} = 5V, I _D = 0.1mA	0.8	_	2.5	V
Forward transfer admittance	-	Y _{fs}	V _{DS} = 5V, I _D = 10mA	20	_	_	mS
Drain-Source Of	N resistance	R _{DS} (ON)	I _D = 10mA, V _{GS} = 4.0V	_	20	50	Ω
Input capacitance		C _{iss}	$V_{DS} = 5V, V_{GS} = 0,$ f = 1MHz	_	6.3	_	pF
Reverse transfer capacitance	r	C _{rss}	V _{DS} = 5V, V _{GS} = 0, f = 1MHz	_	1.3	_	pF
Output capacitance		C _{oss}	V _{DS} = 5V, V _{GS} = 0, f = 1MHz	_	5.7	_	pF
Switching time	Turn-on time	t _{on}	V _{DD} = 5V, I _D = 10mA, V _{GS} = 0~4.0V	_	0.11	_	μs
	Turn-off time	t _{off}	V _{DD} = 5V, I _D = 10mA, V _{GS} = 0~4.0V	_	0.15	_	μs

Q2 Electrical Characteristics (Ta = 25°C)

Chara	cteristic	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cu	rrent	I _{GSS}	V _{GS} = -7V, V _{DS} = 0	_	_	-1	μΑ
Drain-Source brevoltage	eakdown	V _{(BR) DSS}	$I_D = -100\mu A, V_{GS} = 0$	-20	_	_	>
Drain cut-off cur	rent	I _{DSS}	$V_{DS} = -20V, V_{GS} = 0$	_	_	-1	μΑ
Gate threshold v	roltage	V _{th}	$V_{DS} = -3V$, $I_{D} = -0.1mA$	-0.5	_	-1.5	٧
Forward transfer	admittance	Y _{fs}	$V_{DS} = -3V$, $I_{D} = -10mA$	15	_	_	mS
Drain-Source Of	N resistance	R _{DS} (ON)	$I_D = -10$ mA, $V_{GS} = -2.5$ V	_	20	40	Ω
Input capacitanc	е	C _{iss}	$V_{DS} = -3V$, $V_{GS} = 0$, $f = 1MHz$	_	10.4	_	pF
Reverse transfer capacitance		C _{rss}	$V_{DS} = -3V$, $V_{GS} = 0$, $f = 1MHz$	_	2.8	_	pF
Output capacitance		C _{oss}	$V_{DS} = -3V, V_{GS} = 0,$ f = 1MHz	_	8.4	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = -3V$, $I_{D} = -10mA$, $V_{GS} = 0 \sim -2.5V$	_	0.15	_	μs
	Turn-off time	t _{off}	$V_{DD} = -3V$, $I_{D} = -10mA$, $V_{GS} = 0 \sim -2.5V$	_	0.13	_	μs

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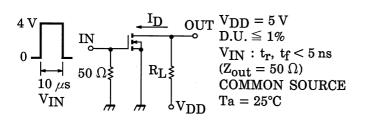
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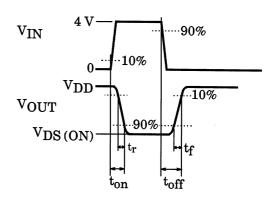
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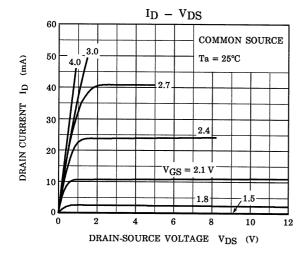
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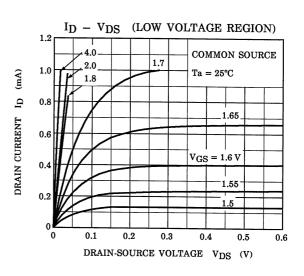
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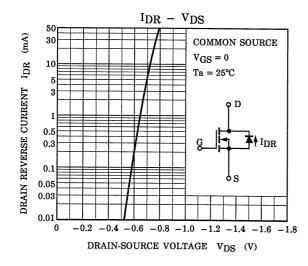
Switching Time Test Circuit

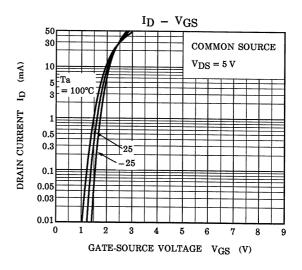




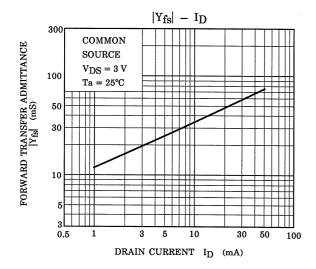


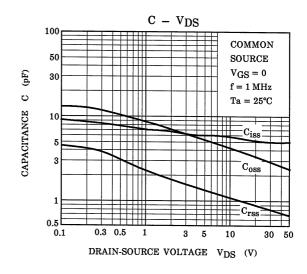


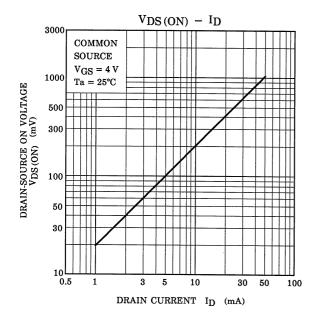


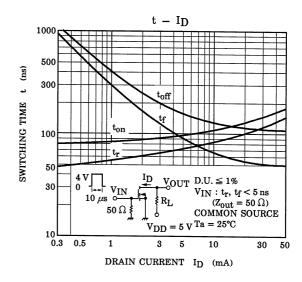


Q1 (Nch MOS FET)



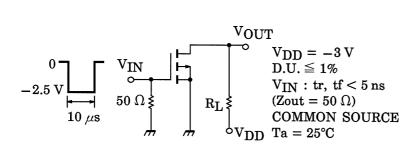


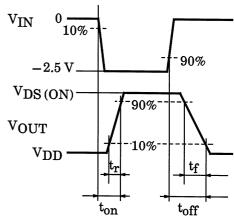


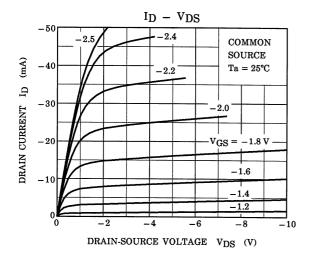


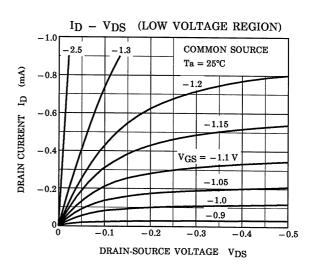
Q2 (Pch MOS FET)

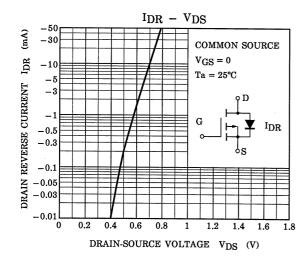
Switching Time Test Circuit

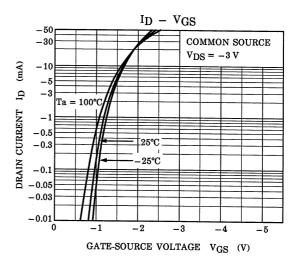




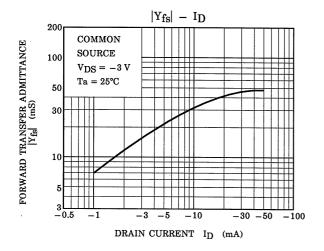


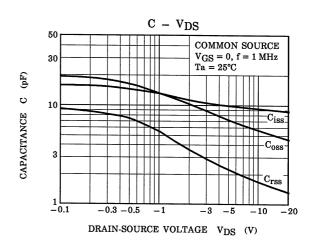


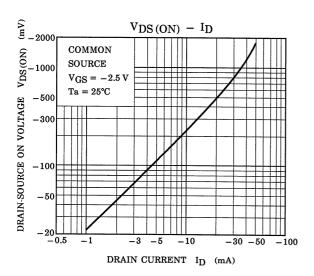


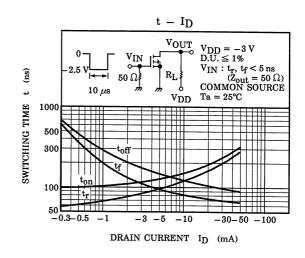


Q2 (Pch MOS FET)

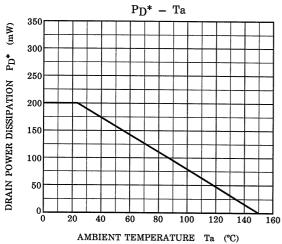








(Q1, Q2 common)



* : Total Rating