

DESCRIPTION

The HY62UF16201A / HY62QF16201A / HY62EF16201A / HY62SF16201A is a high speed, super low power and 2Mbit full CMOS SRAM organized as 131,072 words by 16bits. The HY62UF16201A / HY62QF16201A / HY62EF16201A / HY62SF16201A uses high performance full CMOS process technology and is designed for high speed and low power circuit technology. It is particularly well-suited for the high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

FEATURES

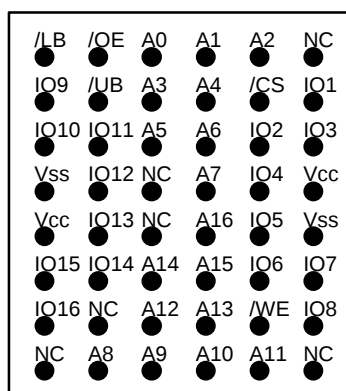
- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL/SL-part)
 - 1.5V(min) data retention
- Standard pin configuration
 - 48ball CSP

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature (°C)
				LL	SL	
HY62UF16201A	3.0	55/70/85	15	10	2	0~70(Normal)
HY62UF16201A-I	3.0	55/70/85	15	10	2	-40~85(E.T.)
HY62QF16201A	2.5	70/85/100	10	10	2	0~70(Normal)
HY62QF16201A-I	2.5	70/85/100	10	10	2	-40~85(E.T.)
HY62EF16201A	2.0	85/100/120	10	10	2	0~70(Normal)
HY62EF16201A-I	2.0	85/100/120	10	10	2	-40~85(E.T.)
HY62SF16201A	1.8	100/120/150	10	10	2	0~70(Normal)
HY62SF16201A-I	1.8	100/120/150	10	10	2	-40~85(E.T.)

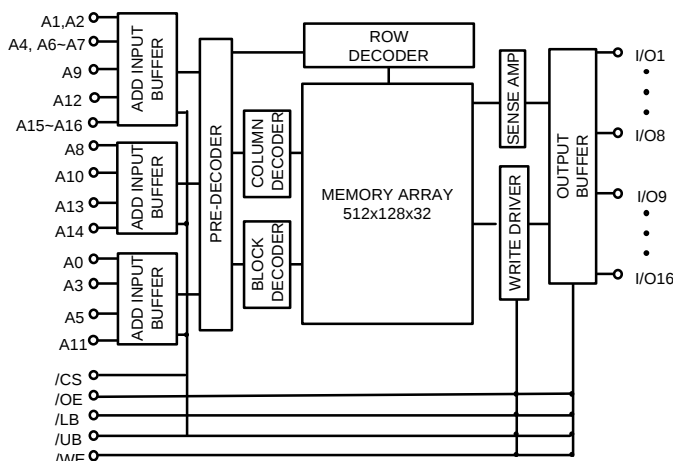
Note 1. E.T. : Extended Temperature, Normal : Normal Temperature

2. Current value is max.

PIN CONNECTION (Top View)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Funtion	Pin Name	Pin Funtion
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A16	Address Input
/OE	Output Enable	Vcc	Power(3.0V/2.5V/2.0V/1.8V)
/LB	Lower Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62UF16201ALLM	55/70/85	LL-part		CSP
HY62UF16201ASLM	55/70/85	SL-part		CSP
HY62UF16201ALLM-I	55/70/85	LL-part	E.T.	CSP
HY62UF16201ASLM-I	55/70/85	SL-part	E.T.	CSP
HY62QF16201ALLM	70/85/100	LL-part		CSP
HY62QF16201ASLM	70/85/100	SL-part		CSP
HY62QF16201ALLM-I	70/85/100	LL-part	E.T.	CSP
HY62QF16201ASLM-I	70/85/100	SL-part	E.T.	CSP
HY62EF16201ALLM	85/100/120	LL-part		CSP
HY62EF16201ASLM	85/100/120	SL-part		CSP
HY62EF16201ALLM-I	85/100/120	LL-part	E.T.	CSP
HY62EF16201ASLM-I	85/100/120	SL-part	E.T.	CSP
HY62SF16201ALLM	100/120/150	LL-part		CSP
HY62SF16201ASLM	100/120/150	SL-part		CSP
HY62SF16201ALLM-I	100/120/150	LL-part	E.T.	CSP
HY62SF16201ASLM-I	100/120/150	SL-part	E.T.	CSP

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit	Remark
V _{IN} , V _{OUT}	Input/Output Voltage	-0.2 to 3.6	V	
V _{CC}	Power Supply	-0.2 to 4.6	V	
T _A	Operating Temperature	0 to 70	°C	HY62UF16201A
				HY62QF16201A
				HY62EF16201A
				HY62SF16201A
		-40 to 85	°C	HY62UF16201A-I
				HY62QF16201A-I
				HY62EF16201A-I
				HY62SF16201A-I
T _{STG}	Storage Temperature	-55 to 150	°C	
P _D	Power Dissipation	1.0	W	
T _{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C•sec	

Note

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Product	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	HY62UF16201A-(I)	2.7	3.0	3.6	V
		HY62QF16201A-(I)	2.2	2.5	2.8	V
		HY62EF16201A-(I)	1.8	2.0	2.2	V
		HY62SF16201A-(I)	1.6	1.8	2.0	
V _{SS}	Ground	HY62UF16201A-(I)	0	0	0	V
		HY62QF16201A-(I)				
		HY62EF16201A-(I)				
		HY62SF16201A-(I)				
V _{IH}	Input High Voltage	HY62UF16201A-(I)	2.2	-	V _{CC} +0.3	V
		HY62QF16201A-(I)	2.0	-	V _{CC} +0.3	V
		HY62EF16201A-(I)	1.6	-	V _{CC} +0.3	V
		HY62SF16201A-(I)	1.4		V _{CC} +0.3	V
V _{IL}	Input Low Voltage	HY62UF16201A-(I)	-0.3(1)	-	0.4	V
		HY62QF16201A-(I)				
		HY62EF16201A-(I)				
		HY62SF16201A-(I)				

Note : 1. V_{IL} = -1.5V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Not Selected	Hi-Z	Hi-Z	I _{SB} , I _{SB1}
L	H	H	X	X	Output Disabled	Hi-Z	Hi-Z	I _{CC}
L	X	X	H	H	Not Selected	Hi-Z	Hi-Z	I _{SB} , I _{SB1}
L	H	L	L	H	Read	DOUT	Hi-Z	I _{CC1}
			H	L		Hi-Z	DOUT	
			L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	Hi-Z	I _{CC1}
			H	L		Hi-Z	DIN	
			L	L		DIN	DIN	

Note:

1. H=V_{IH}, L=V_{IL}, X=don't care

2. UB, LB(Upper, Lower Byte enable)

These active LOW inputs allow individual bytes to be written or read.

When LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.

When UB is LOW, data is written or read to the upper byte, I/O 9 -I/O 16.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.7V~3.6V/2.5V±10%/2.0V±10%/1.8V±10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.)

Sym	Parameter		Test Condition		Min	Typ	Max	Unit
I _{LI}	Input Leakage Current		V _{SS} ≤ V _{IN} ≤ V _{CC}		-1	-	1	uA
I _{LO}	Output Leakage Current		V _{SS} ≤ V _{OUT} ≤ V _{CC} , /CS = V _{IH} or /OE = V _{IH} or /WE = V _{IL} /UB = V _{IH} or /LB = V _{IH}		-1	-	1	uA
I _{CC}	Operating Power Supply Current	HY62UF16201A-(I)	/CS = V _{IL} , V _{IN} = V _{IH} or V _{IL} I _{I/O} = 0mA	V _{CC} = 3.0V	-	8	15	mA
		HY62QF16201A-(I)		V _{CC} = 2.5V/2V/1.8V	-	5	10	mA
		HY62EF16201A-(I)						
		HY62SF16201A-(I)						
I _{CC1}	Average Operating Current	HY62UF16201A-(I)	/CS = V _{IL} , Min Duty Cycle = 100% I _{I/O} = 0mA		-	-	80	mA
		HY62QF16201A-(I)			-	-	60	mA
		HY62EF16201A-(I)			-	-	40	mA
		HY62SF16201A-(I)			-	-	35	mA
I _{SB}	TTL Standby Current (TTL Input)	HY62UF16201A-(I)	/CS = V _{IH} or /CS = V _{IL} , /UB, /LB = V _{IH}		-	-	1	mA
		HY62QF16201A-(I)			-	-	0.5	mA
		HY62EF16201A-(I)			-	-	0.5	mA
		HY62SF16201A-(I)			-	-	0.5	mA
I _{SB1}	Standby Current (CMOS Input)		/CS ≥ V _{CC} - 0.2V or /CS ≤ V _{SS} + 0.2V, /UB, /LB ≥ V _{CC} - 0.2V	SL	-	-	2	uA
				LL	-	-	10	uA
V _{OL}	Output Low Voltage	HY62UF16201A-(I)	V _{CC} = 3.0V	I _{OL} = 2.1mA	-	-	0.4	V
		HY62QF16201A-(I)	V _{CC} = 2.5V	I _{OL} = 0.5mA				
		HY62EF16201A-(I)	V _{CC} = 2.0V	I _{OL} = 0.33mA				
		HY62SF16201A-(I)	V _{CC} = 1.8V	I _{OL} = 0.26mA				
V _{OH}	Output High Voltage	HY62UF16201A-(I)	V _{CC} = 3.0V	I _{OH} = -1.0mA	2.2	-	-	V
		HY62QF16201A-(I)	V _{CC} = 2.5V	I _{OH} = -0.5mA	2.0	-	-	V
		HY62EF16201A-(I)	V _{CC} = 2.0V	I _{OH} = -0.44mA	1.6	-	-	V
		HY62SF16201A-(I)	V _{CC} = 1.8V	I _{OH} = -0.44mA	1.4	-	-	V

Note : Typical values are at V_{CC} = 3.0V/2.5V/2.0V/1.8V, T_A = 25°C

AC CHARACTERISTICS

V_{cc} = 2.7V~3.6V, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

#	Symbol	Parameter	-55		-70		-85		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	55	-	70	-	85	-	ns
2	tAA	Address Access Time	-	55	-	70	-	85	ns
3	tACS	Chip Select Access Time	-	55	-	70	-	85	ns
4	tOE	Output Enable to Output Valid	-	35	-	40	-	45	ns
5	tBA	/LB, /UB Access Time	-	55	-	70	-	85	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	5	-	5	-	5	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	30	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	30	ns
12	tOH	Output Hold from Address Change	10	-	10	-	10	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	55	-	70	-	85	-	ns
14	tCW	Chip Selection to End of Write	50	-	60	-	70	-	ns
15	tAW	Address Valid to End of Write	50	-	60	-	70	-	ns
16	tBW	/LB, /UB Valid to End of Write	50	-	60	-	70	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	45	-	50	-	55	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	20	0	25	0	30	ns
21	tDW	Data to Write Time Overlap	25	-	30	-	35	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	5	-	5	-	ns

V_{cc} = 2.5V±10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

#	Symbol	Parameter	-70		-85		-10		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	70	-	85	-	100	-	ns
2	tAA	Address Access Time	-	70	-	85	-	100	ns
3	tACS	Chip Select Access Time	-	70	-	85	-	100	ns
4	tOE	Output Enable to Output Valid	-	40	-	45	-	50	ns
5	tBA	/LB, /UB Access Time	-	70	-	85	-	100	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	5	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	5	-	5	-	5	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	30	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	30	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	30	ns
12	tOH	Output Hold from Address Change	10	-	10	-	15	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	70	-	85	-	100	-	ns
14	tCW	Chip Selection to End of Write	60	-	70	-	80	-	ns
15	tAW	Address Valid to End of Write	60	-	70	-	80	-	ns
16	tBW	/LB, /UB Valid to End of Write	60	-	70	-	80	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	50	-	55	-	75	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	25	0	30	0	35	ns
21	tDW	Data to Write Time Overlap	30	-	35	-	45	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	5	-	10	-	ns

V_{CC} = 2.0V±10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tBA	/LB, /UB Access Time	-	85	-	100	-	120	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	20	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	5	-	10	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	5	-	5	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	40	ns
12	tOH	Output Hold from Address Change	10	-	15	-	15	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	85	-	100	-	120	-	ns
14	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
15	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
16	tBW	/LB, /UB Valid to End of Write	70	-	80	-	100	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	55	-	75	-	85	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	0	35	0	40	ns
21	tDW	Data to Write Time Overlap	35	-	45	-	50	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	5	-	10	-	10	-	ns

V_{CC} = 1.8V±10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

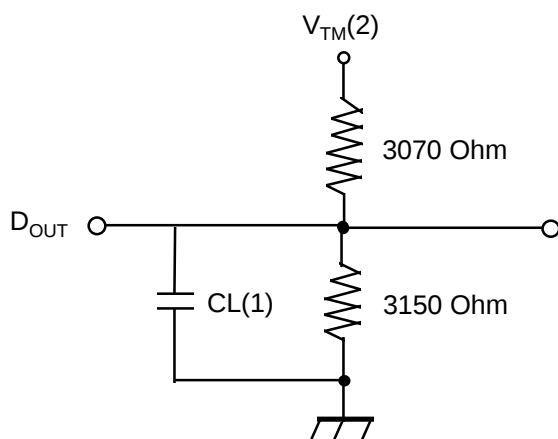
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
READ CYCLE									
1	tRC	Read Cycle Time	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tBA	/LB, /UB Access Time	-	100	-	120	-	150	ns
6	tCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
7	tOLZ	Output Enable to Output in Low Z	5	-	10	-	10	-	ns
8	tBLZ	/LB, /UB Enable to Output in Low Z	5	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	40	0	50	ns
12	tOH	Output Hold from Address Change	15	-	15	-	15	-	ns
WRITE CYCLE									
13	tWC	Write Cycle Time	100	-	120	-	150	-	ns
14	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
15	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
16	tBW	/LB, /UB Valid to End of Write	80	-	100	-	120	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	75	-	85	-	100	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
21	tDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal) / -40°C to 85°C (E.T.), unless otherwise specified

PARAMETER		Value
Input Pulse Level	HY62UF16201A-(I)	0.4V to 2.2V
	HY62QF16201A-(I)	0.4V to 2.2V
	HY62EF16201A-(I)	0.4V to 1.8V
	HY62SF16201A-(I)	0.4V to 1.6V
Input Rise and Fall Time		5ns
Input and Output Timing Reference Level	HY62UF16201A-(I)	1.5V
	HY62QF16201A-(I)	1.1V
	HY62EF16201A-(I)	0.9V
	HY62SF16201A-(I)	0.8V
Output Load		CL = 100pF + 1TTL Load

AC TEST LOADS



Note

1. Including jig and scope capacitance
2. $V_{TM} = 2.8V$ for $V_{CC} = 3.0V$: HY62UF16201A-(I)
 $V_{TM} = 2.3V$ for $V_{CC} = 2.5V$: HY62QF16201A-(I)
 $V_{TM} = 1.8V$ for $V_{CC} = 2.0V$: HY62EF16201A-(I)
 $V_{TM} = 1.6V$ for $V_{CC} = 1.8V$: HY62SF16201A-(I)

CAPACITANCE

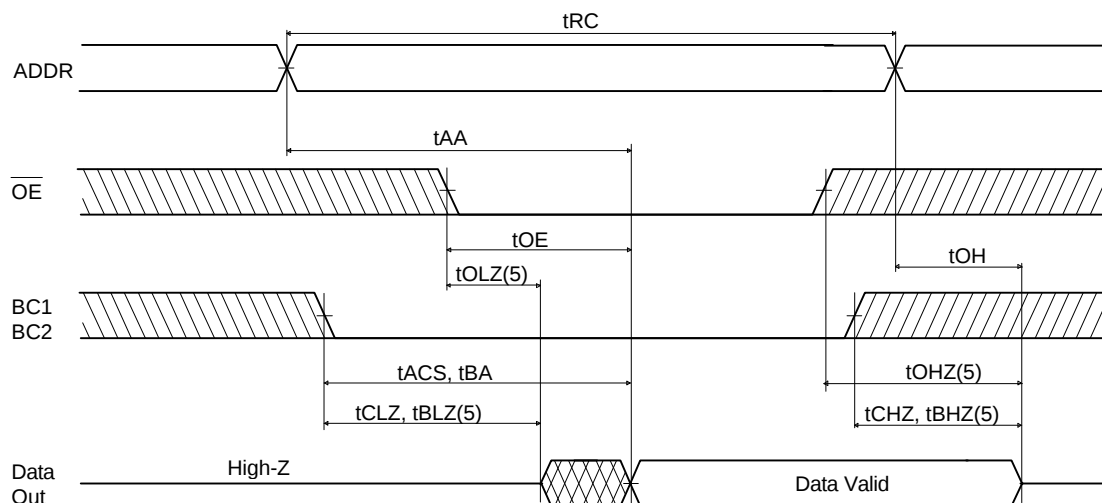
(Temp = 25°C, f= 1.0MHz)

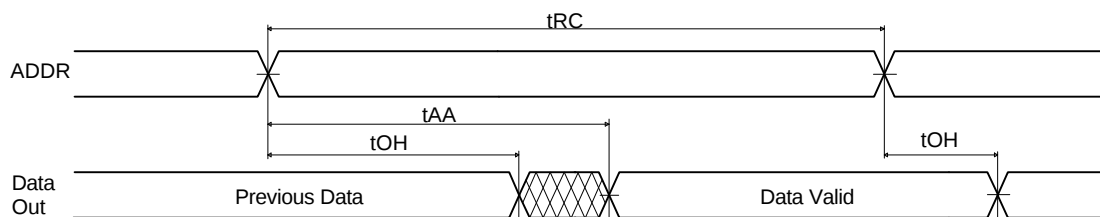
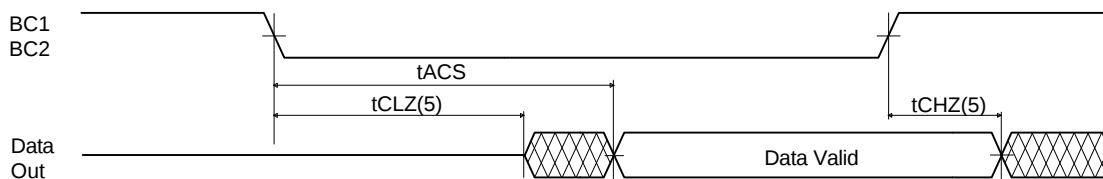
Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /OE)	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O} = 0V$	10	pF

Note : These parameters are sampled and not 100% tested

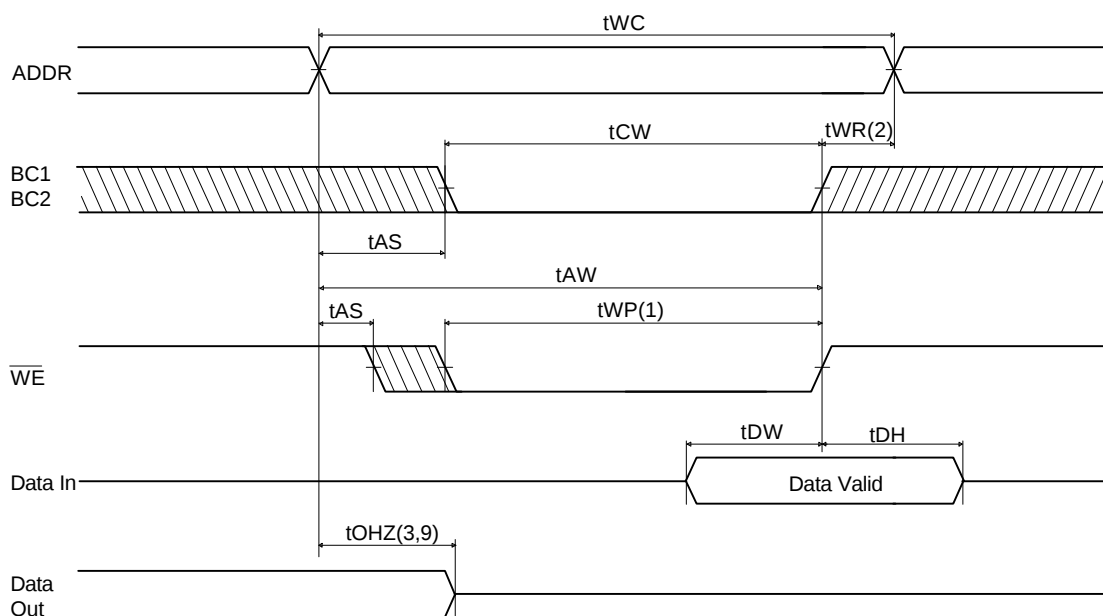
TIMING DIAGRAM

READ CYCLE 1(Note 1)

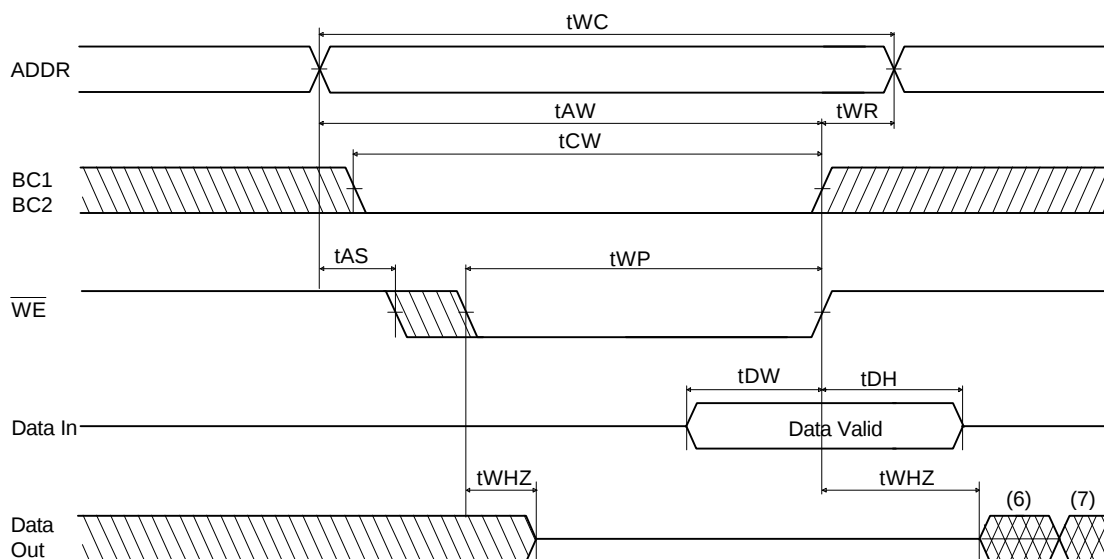


READ CYCLE 2(Note 1,2,4)

READ CYCLE 3(Note 1,3,4)

Notes:

1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB and/or /LB and /CS are in active status.
2. /OE = V_{IL}
3. Transition is measured + 200mV from steady state voltage.
This parameter is sampled and not 100% tested.
4. BC1 in high for the standby, low for active
BC2 in high for the standby, low for active

WRITE CYCLE 1


WRITE CYCLE 2 (Note 5)



Notes:

1. A write occurs whenever a low on the $/WE$ and $/OE$ is low while $/UB$ and/or $/LB$ and $/CS$ are in active state.
2. t_{WR} is measured from the earlier of $/CS$, $/LB$, $/UB$, or $/WE$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $/CS$, $/LB$ and $/UB$ low transition occur simultaneously with the $/WE$ low transition or after the $/WE$ transition, outputs remain in a high impedance state.
5. $/OE$ is continuously low ($/OE = V_{IL}$)
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. Transition is measured +200mV from steady state.
This parameter is sampled and not 100% tested.
9. BC1 in high for the standby, low for active
BC2 in high for the standby, low for active

DATA RETENTION ELECTRIC CHARACTERISTIC

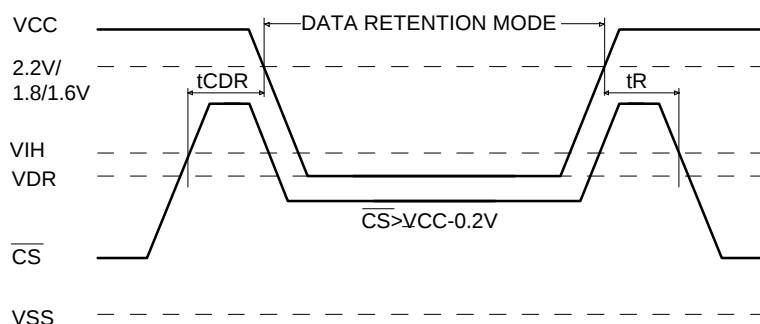
$T_A=0^{\circ}\text{C}$ to 70°C (Normal)/ -40°C to 85°C (E.T.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDR	Vcc for Data Retention	$/CS \geq V_{cc} - 0.2V$	1.5	-	3.6	V
ICCDR	Data Retention Current	$V_{cc}=2.0V, /CS \geq V_{cc} - 0.2V,$ $V_{ss} \leq V_{IN} \leq V_{cc}$	-	-	10	μA
		LL	-	-	2	μA
		SL	-	-	2	μA
TCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
Tr	Operating Recovery Time		tRC(2)	-	-	ns

Notes:

1. Typical values are under the condition of $T_A = 25^{\circ}\text{C}$.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM



Note :

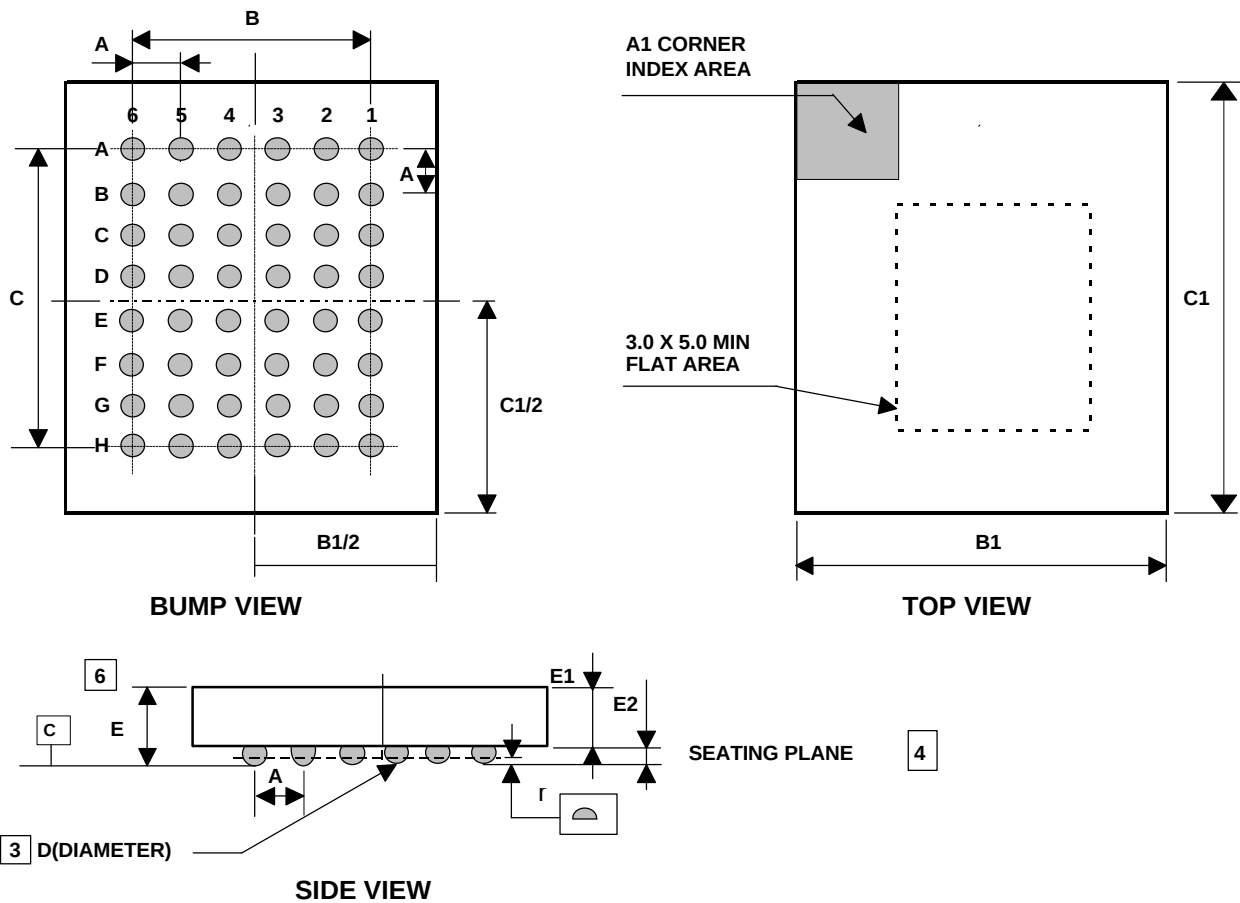
1. 2.2V : HY62UF16201A and HY62UF16201A-I
2.2V : HY62QF16201A and HY62QF16201A-I
1.8V : HY62EF16201A and HY62EF16201A-I
1.6V : HY62SF16201A and HY62SF16201A-I

RELIABILITY SPEC.

TEST	MODE	TEST SPEC.
ESD	HBM	$\geq 2000V$
	MM	$\geq 250V$
LATCH - UP		$\leq -100mA$
		$\geq 100mA$

PACKAGE INFORMATION

48ball Micro Ball Grid Array Package(M)



Symbol	Min.	Typ.	Max.
A	-	0.75	-
B	-	3.75	-
B1			
C	-	5.25	-
C1			
D	0.3	0.35	0.4
E			
E1			
E2			
R			

Note

1. DIMENSIONING AND TOLERANCING PER ASME Y14. 5M-1994.
2. ALL DIMENSIONS ARE MILLIMETERS.
3. DIMENSION "D" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.
5. SOLDER BALL ARRAY MAY BE DEPOPULATED BY OMISSION BALLS FROM A FULL MATRIX. NO SHIFTING OF MATRIX PATTERN IS ALLOWED.
6. THIS IS A CONTROLLING DIMENSION.