User's Guide

GXM12864-18SL

Liquid Crystal Display Module

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CHAPTER 1

Introduction to GXM12864-18 LCM

GXM12864-18SL is a dot matrix graphic LCD module which is fabricated by low power COMS technology. It can display 128*64 dots size LCD panel using a 128*64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

Features

- Display format: 128*64 dots matrix graphic
- STN yellow-green mode
- Easy interface with 8-bit MPU
- Low power consumption
- LED back-light
- Viewing angle: 6 O'clock
- Driving method : 1/64 duty , 1/9 bias
- LCD driver IC: HD61202U(2 个)、HD61203
- Connector: Zebra

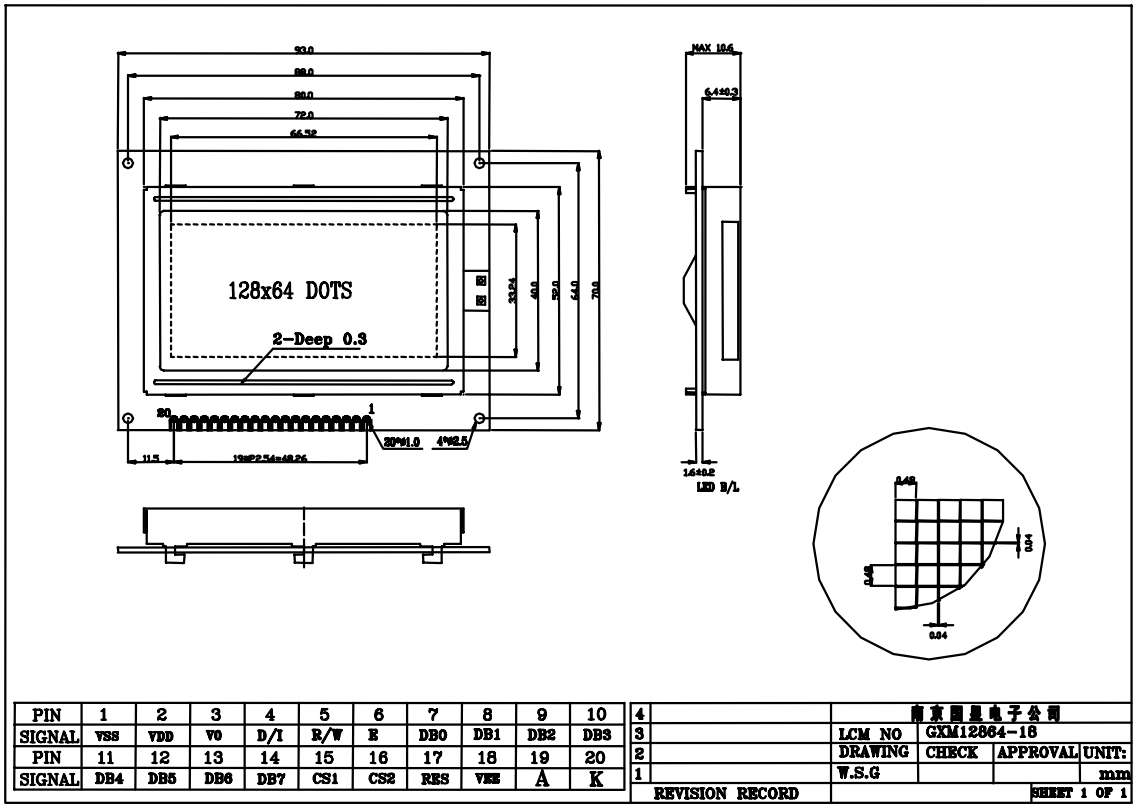
Mechanical Specifications

Item	Dimension	Unit
Viewing Area(W*H)	72.0*40.0	mm
Number of Dots	128.0*64.0	PCS
Dot Size(W*H)	0.48*0.48	mm
Dot Pitch(W*H)	0.52*0.52	mm
Module Size With B/L	93.0*70.0*10.6	mm

Temperature Characteristics

Parameter	Symbol	Rating	Unit
Operating temperature	Topr	-25~+65	℃
Storage temperature	Tstg	-30~+70	℃

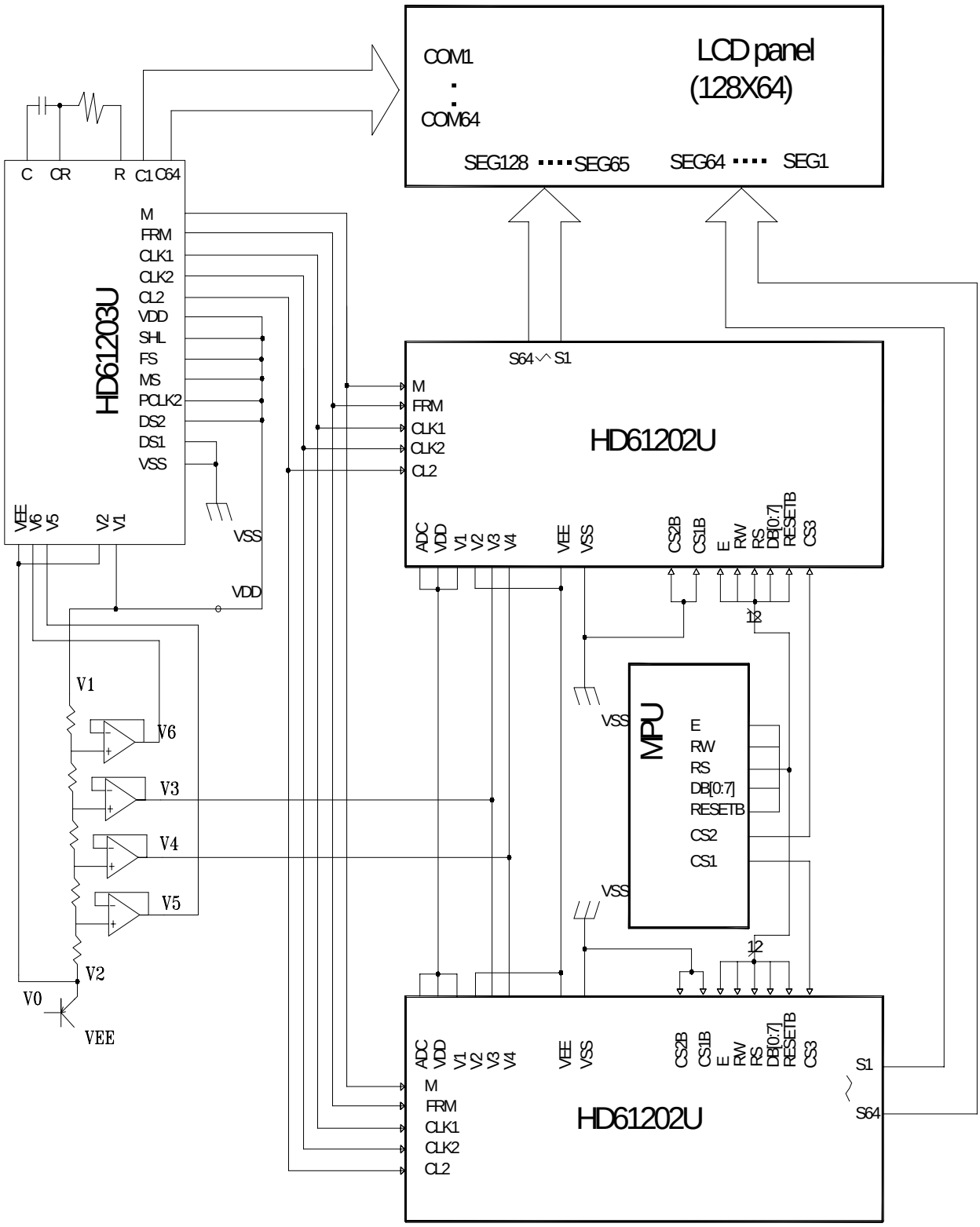
Figure 1. External Dimensions



PIN	1	2	3	4	5	6	7	8	9	10
SIGNAL	VSS	VDD	V0	D/I	R/W	E	DB0	DB1	DB2	DB3
PIN	11	12	13	14	15	16	17	18	19	20
SIGNAL	DB4	DB5	DB6	DB7	CS1	CS2	RES	VEE	A	K

4		南京国显电子公司
3		LCM NO GXM12864-18
2		DRAWING CHECK APPROVAL UNIT:
1		W.S.G mm
REVISION RECORD		SHEET 1 OF 1

Figure 2. Application Diagram



***Note**

1/64 duty, 1/9 bias

$V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5 \geq V_{EE}$

Electro-Optical characteristics

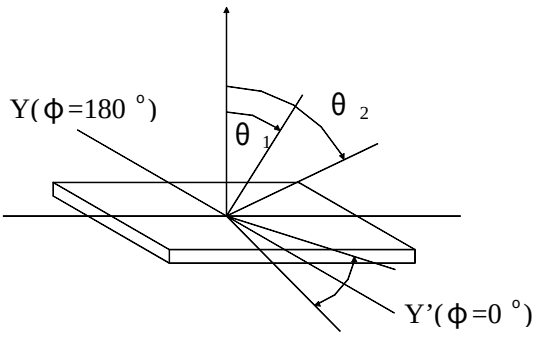
TN Type (Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	40	-	-	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	θ =20° ϕ = 0°	3
Response Time (rise)	t_R	-	110	-	ms	θ =20° ϕ = 0°	4
Response Time (fall)	t_F	-	110	-	ms	θ =20° ϕ = 0°	4

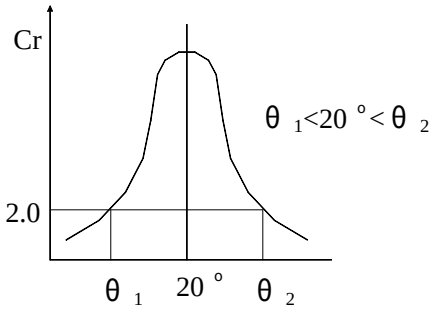
STN Type (Super Twisted Nematic)

Item	Symbol	Min.	Typ.	Max.	Unit	Condition	Note
Viewing Angle	$\frac{\theta_2 - \theta_1}{\phi}$	70 -90	-	+90	deg.	Cr = 2.0	1,2
Contrast Ratio	Cr	-	4	-	-	θ =20° ϕ = 0°	3
Response Time (rise)	t_R	-	110	-	ms	θ =20° ϕ = 0°	4
Response Time (fall)	t_F	-	110	-	ms	θ =20° ϕ = 0°	4

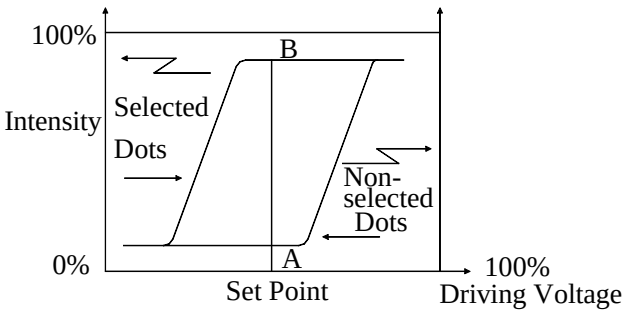
1. Definition of angle θ & ϕ



2. Definition of viewing angle θ_1 & ϕ_2



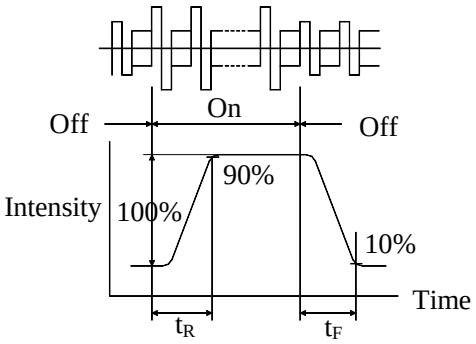
3. Definition of contrast Cr



$Cr = (A / B)^{p}$ Negative : P = -1

Positive : P = +1

4. Definition of optical response



Interface Pin Connections

Pin No.	Symbol	I/O Type	Description
1	VSS	Supply	Ground
2	VDD	Supply	Power supply
3	V0	Supply	LCD driver supply voltage
4	D/I		Data input/output pin of internal shift register **MS SHL DIO1 DIO2** H H Output Output H L Output Output L H Input Output L L Output Input
5	R/W		Read or Write **RW Description** H Data appears at DB[7:0] and can be read by the CPU while E= H CS1B=L,CS2B=L and CS3=H. L Display data DB[7:0] can be written at falling edge of E when CS1B=L, CS2B=L and CS3=H.
6	E		Enable signal **E Description** H Read data in DB[7:0] appears while E= "High". L Display data DB[7:0] is latched at falling edge of E.
7 8 9 10 11 12 13 14	DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7	I/O	Data bus [0~7] Bi-directional data bus
15 16	CS1 CS2	I	Chip selection When CS1=H,CS2=L, select IC1 When CS1=L,CS2=H, select IC2
17	RESETB	I	Reset signal. When RSTB=L 【1】ON/OFF register becomes set by 0.(display off) 【2】display start line register becomes set by 0 (Z-address 0 set, display from line 0) 【3】After releasing reset , this condition can be changed only by instruction.
18	VEE	Power	VEE is connected by the same voltage.
19	A		Back-light anode
20	K		Back-light cathode

Electrical Absolute Maximum Ratings (HD61203U)

Item	Symbol	Limit	Unit	Notes
Power supply voltage(1)	Vcc	-0.3 to +7.0	V	2
Power supply voltage(2)	Vee	Vcc – 17.0 to Vcc +0.3	V	5
Terminal voltage (1)	Vt1	-0.3 to Vcc +0.3	V	2,3
Terminal voltage (2)	Vt2	Vee – 0.3 to Vcc +0.3	V	4,5

Operating temperature	Topr	-30 to +75	℃
Storage temperature	Tstg	-40 to +80	℃

Notes: 1. IF LSIs are used beyond absolute maximum ratings ,they may be premanently Destroyed . We strongly recommend you to use the LSI within electrical characteristic limits for normal operation,because use beyond these conditions will cause malfunction and poor reliability.

2. Based on GND = 0V.

3. Applies to input terminals (except V1L , V1R , V2L , V2R , V5L , V5R , V6L , and I/O Terminals at high impedance.

4. Applies to V1L , V1R , V2L , V2R , V5L , V5R , V6L and V6R .

5. Apply the same value of voltages to V1L and V1R , V2L and V2R , V5L and V5R ,V6L and V6R , Vee (23pin)and Vee (58 pin)respectively.

Maintain Vcc≥V1L = V1R≥V6L=V6R≥V5L =V5R≥V2L =V2R≥V

DC Electrical Characteristics(HD61203U)

(VCC= 2.7 to 5.5V, GND =0V,VCC-VEE=8.0 to 16.0V,Ta= -30 to +75℃)

Test Item	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input high voltage	V_{IH}	0.7×Vcc	-	Vcc	V		1
Input low voltage	V_{IL}	GND	-	0.3×Vcc	V		1
Output high voltage	V_{OH}	Vcc-0.4	-	-	V	I_{OH}= - 0.4mA	2
Output low Voltage	V_{OL}	-	-	0.4	V	I_{OL} =0.4mA	2
VI-XJ on resistance	R_{ON}	-	-	1.5	kΩ	V_{CC} - V_{EE} =10V Load current ±150μA	13
Input leakage current	I_{IL1}	-1.0	-	1.0	μA	V_{IN} =0 to V_{CC}	3
Input leakage current	I_{IL2}	-2.0	-	2.0	μA	V_{IN} = V_{EE} to V_{CC}	4
Operating frequency	fopr1	50	-	600	kHz	Im master mode external clock operation	5
Operating frequency	fopr2	0.5	-	1500	kHz	In slave mode shift register	6
Oscillation frequency	fosc	315	450	585	kHz	Cf=20pF±5% Cf=39 kΩ±2%	7,12
Dissipation current(1)	I_{GG1}	-	-	1.0	mA	In master mode 1/128 duty cycle Cf=20Pf Rf=39 kΩ	8,9
Dissipation current(2)	I_{GG2}	-	-	200	μA	In slave mode 1/128 duty cycle	8,10
Dissipation current	I_{EE}	-	-	100	μA	In master mode 1/128 duty cycle	8,11

Notes:

1. Applies to input terminals FS , DS1 , DS2 , CR , SHL , M/S , and FCS and I/O terminals DL , M , DR , and CL2 in the input state.
2. Applies to output terminals , Ø1, Ø2,and FRM and I/O common terminals DL , M , DR , and CL2 in the output status.
3. Applies to input terminals FS , DS1 , DS2, CR , STB/, SHL, M/S, FCS , CL1 , and TH , I/O terminals DL , M , DR ,and CL2 in the input state and NC terminals.

4. Applies to V1L , V1R, V2L , V2R, V5L, V5R , V6L , and V6R.Donnot connect any lines to ×1 to ×64.
5. External clock is as follows.
   Duty cycle = TH÷(TH+TL) ×100%

	Min	Typ	Max	Unit
Duty cycle	45	50	55	%
Trcp	-	-	50	ns
Trcp	-	-	50	ns

6. Applies to the shift register in the slave mode .For details ,refer to AC characteristics.
7. Connect oscillation resistor(Rf)and oscillation capacitance(Cf) as shown in this figure. Oscillation frequency(fosc) is twice as much as the frequency (f Ø) at Ø1 or twice Ø2.
8. NO lines are connected to output terminals and current folwing through the input circuit is excluded .This value is specified at VIH =Vcc and VIL =GND .
9. This value is specified for current flowing through GND in the following conditions:Internal Oscillation circuit is used .Each terminal of DS1 , DS2 , FS , SHL , M/S , STB/ , and FCS is connected to Vcc and each of CL1 and TH to GND , Oscillator is set as /described in note 7.
10. This value is specified for current flowing through GND under the following conditions:Eachterminals of DS1 , DS2 , FS , SHL , STB/, FCS and CR is connected to Vcc,CL1,TH ,and M/S to GND and the terminals CL2 , M, and CR is connected to Vcc , CL1,TH, and M/S to GND and the terminals Cl2 , M , and DL are respectively connected to terminals CL2, M,and DL of the HD1203U under the condition described in note 9.
11. This value is specified for current flowing through Vee under the condition described in note9. Donnot connect any lines to terminal V.
12. This figure shows a typical relation among oscillation frequency ,Rf and Cf. Oscillation frequency may vary with the mounting conditions.
13. Resistance between terminal X and terminal V (one of V1L , V1R , V2L , V2R ,V5L , V5R , V6L , and V6R)when load current flows through one of the terminals ×1 to× 64 . This value is specified under the following conditions:

$$V_{cc} - V_{EE} = 10\ v$$

$$V_{1L} = V_{1R}\ ,\ V_{6L} = V_{6R} = V_{cc} - 1/7(V_{cc} - V_{EE})$$

$$V_{2L} = V_{2R}\ ,\ V_{5L} = V_{5R} = V_{EE} + 1/7(V_{cc} - V_{EE})$$

The following is a description of the range of power supply voltage for liquid crystal display drive.Apply positive voltage to V1L = V1R and V6L = V6R and negative voltage to V2L=V2R and V5L=V5R within the ΔV range .This range allows stable impedance on driver output (RON).Notice that ΔV depends on power supply voltage V_{CC} -V_{EE}.

14.Specified at +75℃ for die products

CHAPTER 2

Driver IC Function Description

HD61203U Driver IC
64COM graphic driver for dot matrix LCD

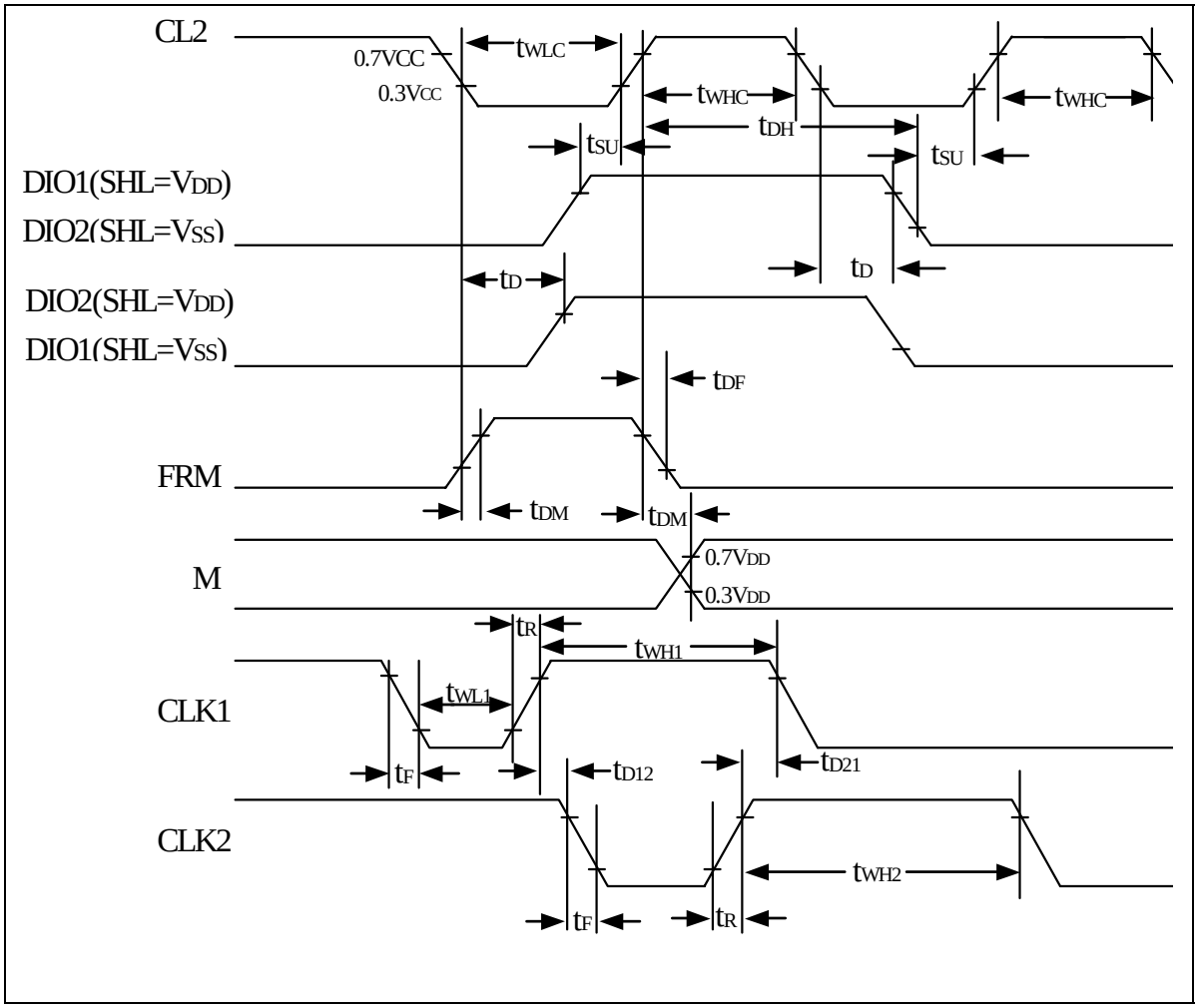
Introduction

The HD61203U is a common signal driver for dot matrix liquid crystal graphic display systems.It gemerates the timing signals (switch signal to convert LCD waveform to AC ,frame synchronous signal) and supplies them to the column driver to control display. It provides 64 driver output lines and the impedance is low enough to drive a large screen .

As the HD61203U is a produced by a CMOS process ,it is fit for use in portable battery-driven equipment utilizing the liquid crystal display´ s low power control display .The user can easily construct a dot matrix liquid crystal graphic display system by combining the HD61203U and the column (segment) driver HD61202U.

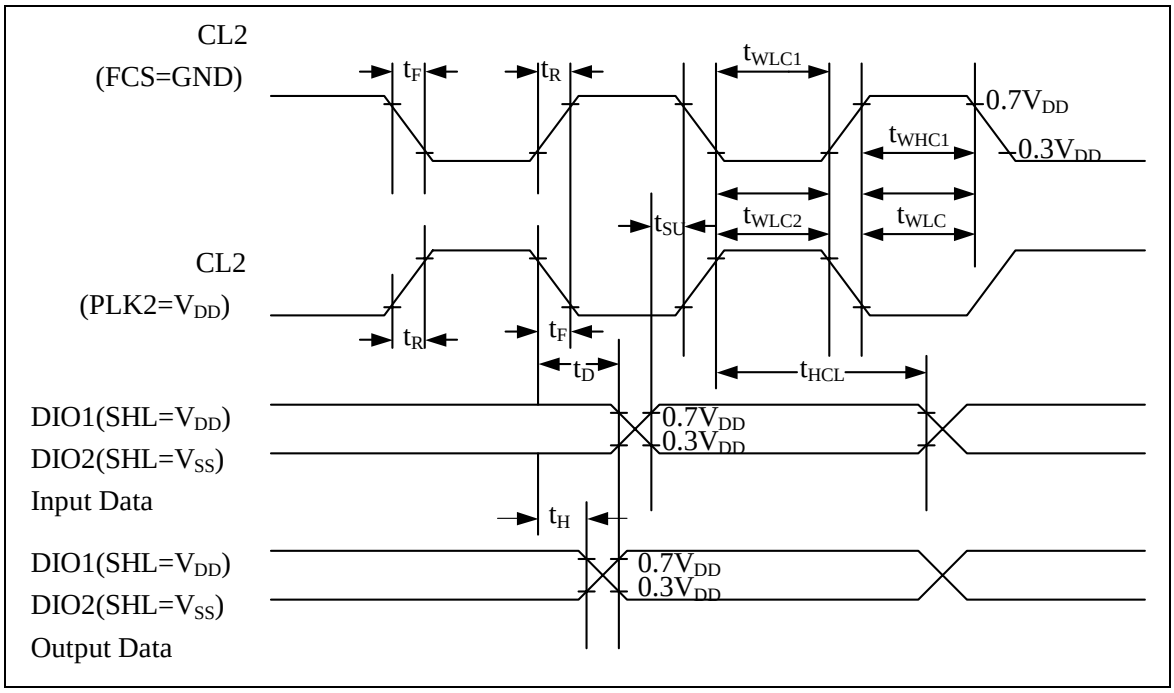
AC Characteristics (Vcc=2.7V to 5.5V,GND =0V,Ta=-30 to +75℃)*2

1.IN the Slave Mode(M/S=GND)



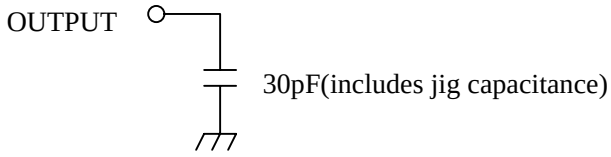
Item	Symbol	Min	Typ	Max	Unit
Data Setup Time	T_{DS}	20	-	-	
Data Hold Time	t_{DH}	40	-	-	
Data Delay Time	t_{DD}	5	-	-	
FRM Delay Time	t_{DFRM}	-2	-	2	μs
M Delay Time	t_{DM}	-2	-	2	
CL2 Low Level Width	t_{WCL2L}	35	-	-	
CL2 High Level Width	t_{WCL2H}	35	-	-	
CLK1 Low Level Width	t_{WL1}	700	-	-	
CLK2 Low Level Width	t_{WL2}	700	-	-	
CLK1 High Level Width	t_{WH1}	2100	-	-	
CLK2 High Level Width	t_{WH2}	2100	-	-	ns
CLK1-CLK2 Phase Difference	t_{D12}	700	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	700	-	-	
CLK1,CLK2 Rise/Fall Time	t_R/t_F	-	-	150	

Slave mode (MS=V_{SS})



Item	Symbol	Min	Typ	Max	Unit	Note
CL2 Low Level Width	t_{WLC2L}	450	-	-	ns	PCLK2=V_{SS}
CL2 High Level Width	t_{WLCL2H}	150	-	-		PCLK2=V_{SS}
CL2 Low Level Width	t_{WHCL2L}	150	-	-		PCLK2=V_{DD}
CL2 High Level Width	t_{WHCL2H}	450	-	-		PCLK2=V_{DD}
Data Setup Time	t_{DS}	100	-	-		
Data Hold Time	t_{DH}	100	-	-		
Data Delay Time	t_{DD}	-	-	200		*1
Output Data Hold Time	t_{DHW}	10	-	-		
CL2 Rise/Fall Time	t_R/t_F	-	-	30		

NOTE: 1. The following load circuit is connected for specification.



2.Specified at +75℃ for die products

FUNCTIONAL DESCRIPTION

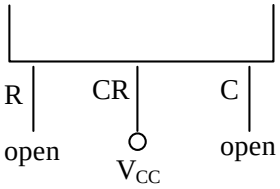
1.CR Oscillator

The CR oscillator generates display timing signals and operating for the HD61202U. It is required when the HD61203U is used with the HD61203U. An oscillation resister Rf and an oscillation capacitor Cf are attached as shown in Figure 1.When using an external clock ,input the clock into terminal CR and donnot connect any lines to terminals R and C.

The oscillator is not requied when the HD61203U is used with the HD61830.Then , connect terminal CR to the high level and donnot connect any lines to terminals R and C (Figure 2).

1) **Oscillator Connection with HD61202U**

2) Oscillator connection with HD61830



2.Timing Generation circuit

The timing generator circuit generates display timing and operating clock for the HD61203U.This circuit is required when the HD61203U is used with the HD61202U .Connect terminal M/S to high level (master mode). It is not necessary when the display timing signal is supplied from other circuits , for example , from HD61830. In this case connect the terminals FS,DS1 , and DS2 to high level and M/S to low level (slave mode).

3.Bidirectional Shift Register

A 64-bit bidirectional shift register. The data is shifted from DL to DR when SHL is at high level and from DR to DL when SHL is at low level .In this case , CL2 is used as shift clock . The lowest order bit on the DR side corresponds to X64.

4.Liquid Crystal Display Driver Circuit

The combination of the data from the shift register with the M signal allows one of the four liquid crystal display driver levels V1 , V2, V5, and V6 to be transferred to the output terminals (Table 1).

Table 1 Output Levels

Data Fm the Shift Register	M	Output Level
1	1	V2
0	1	V6
1	0	V1
0	0	V5

CHAPTER 3

Driver IC Function Description

KS0108 Driver IC
64 SEG graphic driver for dot matrix LCD

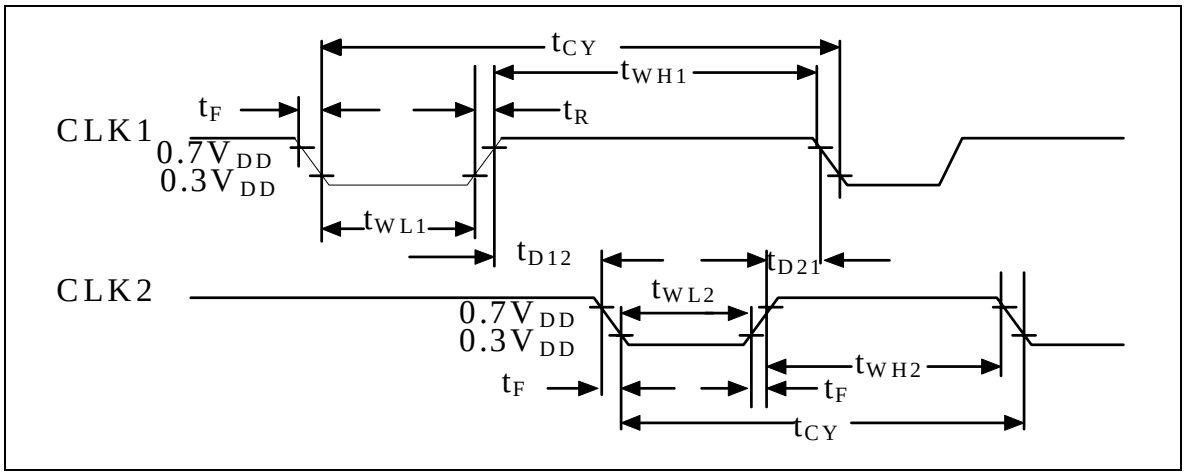
Introduction

The KS0108B is an LCD driver LSI with 64 channel outputs for dot matrix liquid crystal graphic display systems. This device consists of the display RAM, 64 bit data latch 64 bit drivers and decoder logics. It has the internal display RAM for storing the display data transferred from a 8 bit micro controller and generates the dot matrix liquid crystal driving signals corresponding to stored data. The KS0108B composed of the liquid crystal display system in combination with the KS0107B(64 common driver).

AC Characteristics (V_{DD}=4.5~5.5V ,V_{SS}=0V, Ta=-30℃~+85℃)

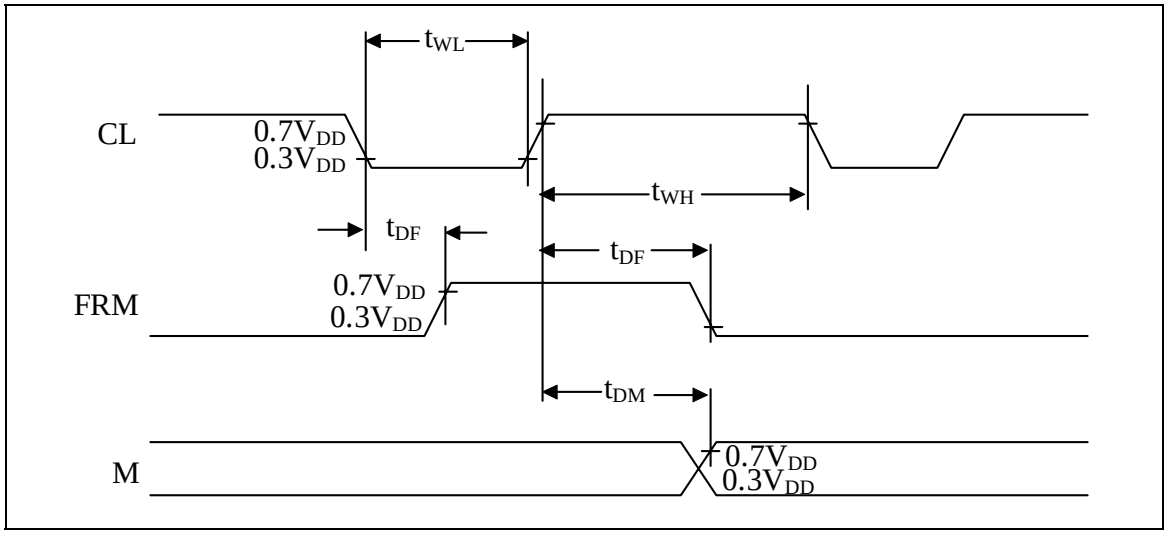
(1) Clock Timing

Characteristic	Symbol	Min	Typ	Max	Unit
CLK1, CLK2 Cycle Time	t_{CY}	2.5	-	20	μs
CLK1 ‘ LOW ’ Level Width	t_{WL1}	625	-	-	ns
CLK2 ‘ LOW ’ Level Width	t_{WL2}	625	-	-	
CLK1 ‘ HIGH ’ Level Width	t_{WH1}	1875	-	-	
CLK2 ‘ HIGH ’ Level Width	t_{WH2}	1875	-	-	
CLK1-CLK2 Phase Difference	t_{D12}	625	-	-	
CLK2-CLK1 Phase Difference	t_{D21}	625	-	-	
CLK1, CLK2 Rise Time	t_R	-	-	150	
CLK1, CLK2 Fall Time	t_F	-	-	150	



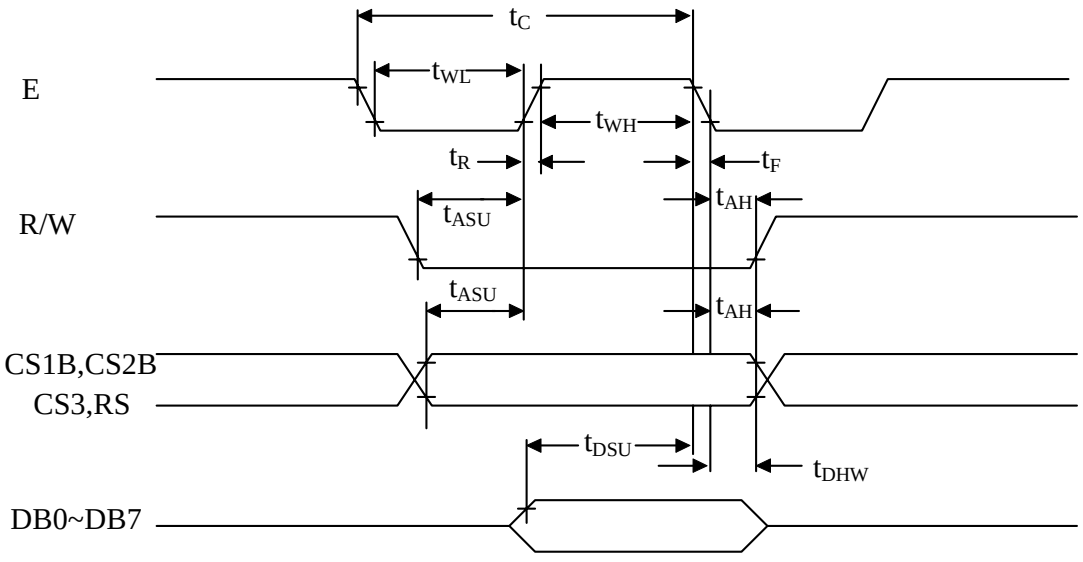
（2）.Display Control Timing

Characteristic	Symbol	Min	Typ	Max	Unit
FRM Delay Time	t_{DF}	-2	-	2	
M Delay Time	t_{DM}	-2	-	2	us
CL ‘LOW’ Level Width	t_{WL}	35	-	-	
CL ‘HIGH’ Level Width	t_{WH}	35	-	-	

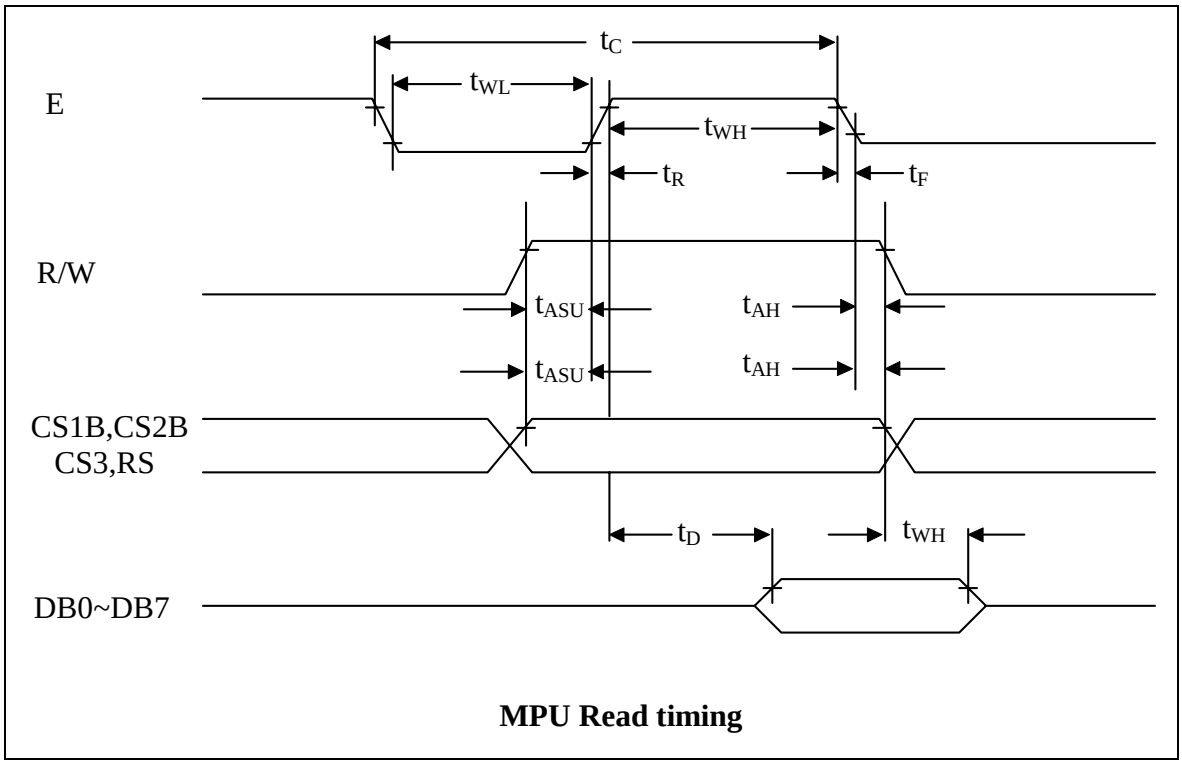


（3）. MPU Interface

Characteristic	Symbol	Min	Typ	Max	Unit
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	
E Low Level Width	t_{WL}	450	-	-	
E Rise Time	t_R	-	-	25	
E Fall Time	t_F	-	-	25	
Address Set-Up Time	t_{ASU}	140	-	-	
Address Hold Time	t_{AH}	10	-	-	
Data Set-Up Time	t_{SU}	200	-	-	
Data Delay Time	t_D	-	-	320	
Data Hold Time (Write)	t_{DHW}	10	-	-	
Data Hold Time (Read)	t_{DHR}	20	-	-	



MPU Write timing



MPU Read timing

OPERATING PRINCIPLES & METHODS

1. I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS!B-CS3.

2. Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.
When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

3. Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H , RS=L, status data (busy check) can read out.
To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

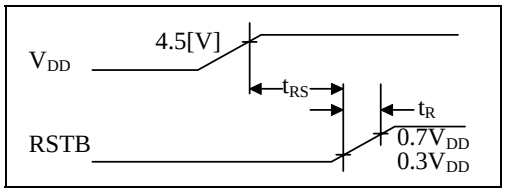
4. Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can by accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction. The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns

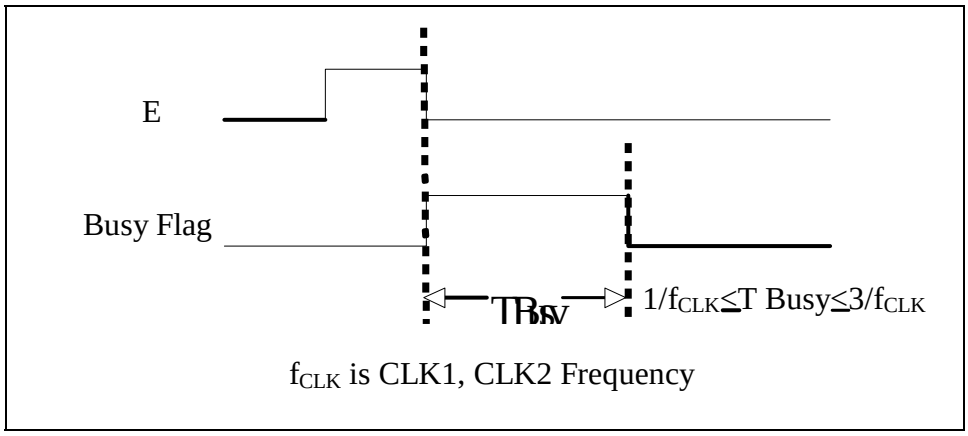


5. Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating .

When busy flag is low, KS0108B can accept the data or instruction.

DB7indicates busy flag of the KS0108B.



6. Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip-flop is reset (logical low), selective voltage or non selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data. The display on/off flip-flop can changes status by instruction. The display data at all segment disappear while RSTB is low.
The status of the flip-flop is output to DB5 by status read instruction.
The display on/off flip-flop synchronized by CL signal.

7. X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

8. Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by read or write operations of display data.

9. Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display , write datra1. The other way , off state, writes 0.
Display data RAM address and segment output can be controlled by ADC signal.
ADC=H => Y-address 0: S1~Y address 63: S64
ADC=L => Y-address 0: S64~Yaddress 63: S1
ADC terminal connect the V_{DD} or V_{SS}.

10. Display Start Line Register

The display start line register indicates of display data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z address counter.
It is used for scrolling of the liquid crystal display screen.

Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The following table shows various instructions.

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read Display Date	1	1	Read data								Reads data (DB[7:0]) from display data RAM to the data bus.
Write Display Date	1	0	Write data								Writes data (DB[7:0]) into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically
Status Read	0	1	Busy	0	ON/ OFF	Re-set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

1. Display On/Off

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

2. Set Address (Y Address)

Y address (AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

3. Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

4. Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

5. Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.
  When RESET is 0, initializing has finished and the system is in the usual operation condition.

6. Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

7. Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0