GLT416016

1M X 16 CMOS DYNAMIC RAM WITH EXTENDED DATA OUTPUT

May 2000 (Rev.3.0)

Features :

- 1,048,576 words by 16 bits organization.
- Fast access time and cycle time.
- Dual $\overline{CAS}$ Input.
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 1024 refresh cycles per 16ms.
- Available in 400 mil SOJ and TSOP(II) Packages.
- Single 5.0V±10% Power Supply.
- All inputs and Outputs are TTL compatible.
- Extended Data-Out(EDO) Page Mode operation.

Description :

The GLT416016 is a 1,048,576 x 16 bit high-performance CMOS dynamic random access memory. The GLT416016 offers Fast Page mode with Extended Data Output, and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT416016 has symmetric address and accepts 1024-cycle refresh in 16ms interval.

All inputs are TTL compatible. EDO Page Mode operation allows random access up to 1024 x 16 bits within a page, with cycle times as short as 18ns.

The GLT416016 is best suited for graphics, and DSP applications requiring high performance memories.

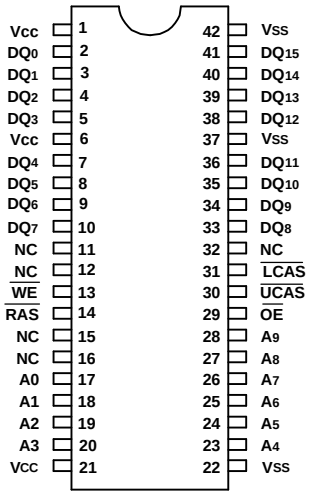
HIGH PERFORMANCE	45	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	22 ns	25 ns	30 ns
Min. Extended Data Out Page Mode Cycle Time, (t_{PC})	18 ns	20 ns	25 ns
Min. Read/Write Cycle Time, (t_{RC})	80 ns	85 ns	104 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	12 ns	14 ns	15ns

G-Link Technology Corporation
2701Northwestern Parkway
Santa Clara, CA 95051, U.S.A.

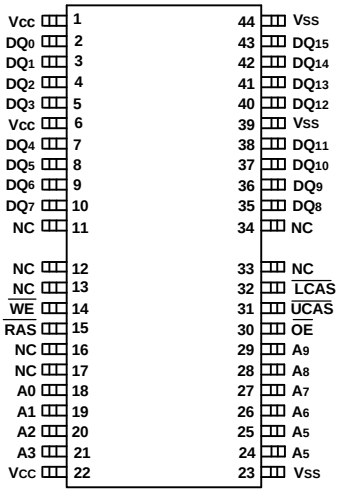
G-Link Technology Corporation,Taiwan
6F, No. 24-2, Industry E. RD. IV, Science Based
Industrial Park, Hsin Chu, Taiwan.

Pin Configuration

GLT416016
SOJ Top View



TSOP(Type II)
Top View



Pin Descriptions:

Name	Function
A_0 - A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_{15}	Data Inputs / Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient) .....-0°C to +70°C

Storage Temperature(plastic).....-55°C to +150°C

Voltage Relative to V_{SS}.....-1.0V to + 7.0V

Short Circuit Output Current.....50mA

Power Dissipation.....1.0W

*Note:Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=5V±10%, V_{SS}=0V

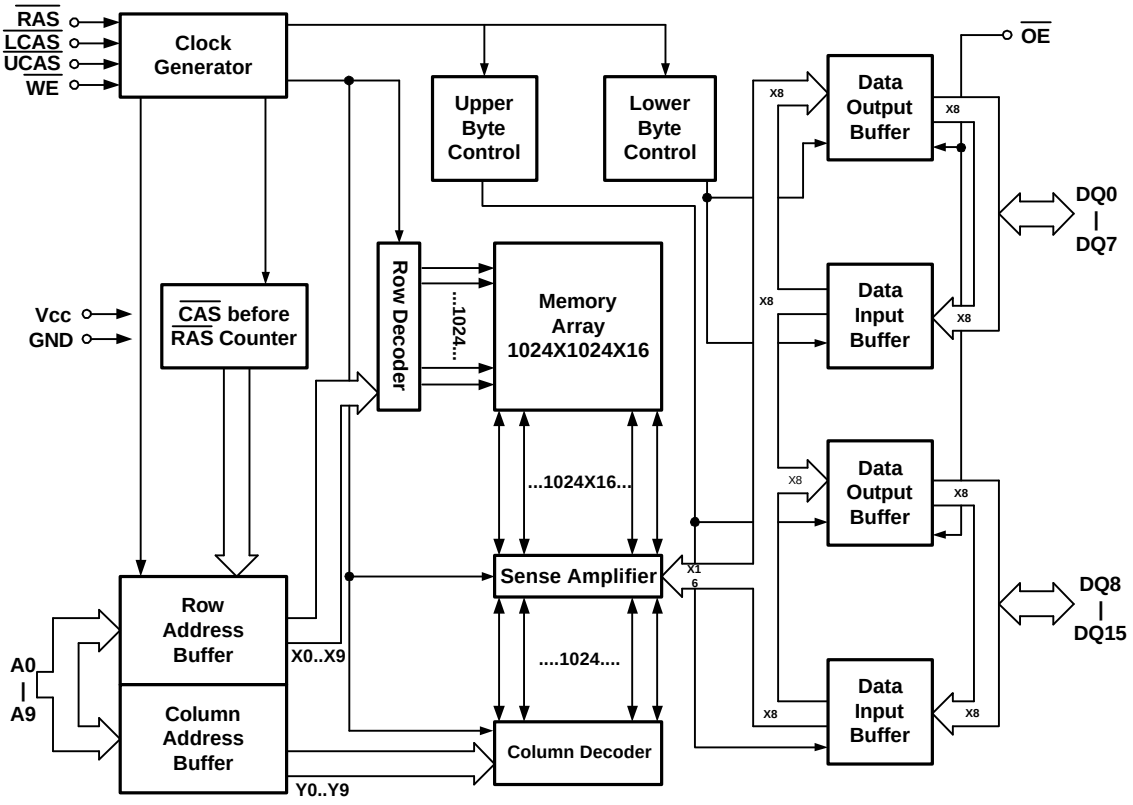
Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- $\overline{CAS}$ means $\overline{UCAS}$ and $\overline{LCAS}$.
- All voltages are referenced to GND.
- After power up, wait more than 100µs and then, execute eight $\overline{CAS}$ -before-$\overline{RAS}$ or $\overline{RAS}$ -only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT416016

Function		RAS	CASL	CASH	WE	OE	ADDRESS	DQs	Notes
Standby		H	H→X	H→X	X	X		High-Z	
Read: Word		L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte		L	L	H	H	L	ROW/COL	Lower Byte,Data-Out Upper Byte,High-Z	
Read: Upper Byte		L	H	L	H	L	ROW/COL	Lower Byte,High-Z Upper Byte,Data-Out	
Write: Word(Early Write)		L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)		L	L	H	L	X	ROW/COL	Lower Byte,Data-In Upper Byte,High-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW/COL	Lower Byte,High-Z Upper Byte,Data-In	
Read Write		L	L	L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW/COL	Data-Out	1
	2nd Cycle	L	H→L	H→L	H	L	COL	Data-Out	1
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW/COL	Data-In	2
	2nd Cycle	L	H→L	H→L	L	X	COL	Data-In	2
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW/COL	Data-Out,Data-In	1,2
	2nd Cycle	L	H→L	H→L	H→L	L→H	COL	Data-Out,Data-In	1,2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	1
	Write	L→H→L	L	L	L	X	ROW/COL	Data-In	2,3
$\overline{\text{RAS}}$ -Only Refresh		L	H	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	L	X	X		High-Z	4

Notes:

1. These READ cycles may also be BYTE READ cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
2. These WRITE cycles may also be BYTE READ cycles (either $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ active).
3. EARLY WRITE only.
4. At least one of the two CAS signals must be active ($\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$).

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test=0V)		-10		+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ 5.5V Output is disabled (Hiz)		-10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 45ns t_{RAC} = 50ns t_{RAC} = 60ns			210 200 180	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} other inputs ≥V_{SS}				2	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	$\overline{RAS}$ cycling, $\overline{UCAS}$, $\overline{LCAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 45ns t_{RAC} = 50ns t_{RAC} = 60ns			210 200 180	mA	2
I_{CC4}	Operating Current, EDO Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ address cycling:t_{PC}=t_{PC}(min.)	t_{RAC} = 45ns t_{RAC} = 50ns t_{RAC} = 60ns			210 200 180	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ address cycling: t_{RC}=t_{RC} (min.)	t_{RAC} = 45ns t_{RAC} = 50ns t_{RAC} = 60ns			210 200 180	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥V_{CC}-0.2V, $\overline{UCAS}$ ≥V_{CC}-0.2V, $\overline{LCAS}$ ≥V_{CC}-0.2V, All other inputs V_{SS}				1	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		V_{CC}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5.0mA		2.4			V	

Notes:

1.I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC}(max.) is measured with the output open.

2.I_{CC} is dependent upon the number of address transitions specified I_{CC}(max.) is measured with a maximum of one transition per address cycle in random Read/Write and EDO Fast Page Mode.

3.Specified V_{IL}(min.) is steady state operation. During transitions V_{IL}(min.) may undershoot to -1.0V for a period not to exceed 20ns. All AC parameters are measured with V_{IL}(min.)≥V_{SS} and V_{IH}(max.)≤V_{CC}.

AC Characteristics

T_A = 0°C to 70°C , V_{CC} = 5 V ± 10%, VIH/VIL = 2.4/0.8 V, V_{OH}/V_{OL} = 2.0/0.8V

An initial pause of 100 µs and 8 $\overline{CAS}$ -before- $\overline{RAS}$ or $\overline{RAS}$ -only refresh cycles are required after power-up.

		45		50		60			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**	**Notes**
Read or Write Cycle Time	t_{RC}	80		85		104		ns	
Read Modify Write Cycle Time	t_{RWC}	103		106		133		ns	
$\overline{RAS}$ Protegra Time	t_{RP}	30		30		40		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	45	100K	50	100k	60	100k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		45		50		60	ns	1,2,3
Access Time from $\overline{CAS}$	t_{CAC}		12		14		15	ns	1,5,10
Access Time from Column Address	t_{AA}		22		25		30	ns	1,5,6
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	0		0		0		ns	
$\overline{CAS}$ to Output High-Z	t_{CEZ}	3	8	3	8	3	10	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	13		14		14		ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	t_{ROH}	9		9		10		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40		45		45		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	7	10K	8	10k	12	10k	ns	
$\overline{RAS}$ to CAS Delay Time	t_{RCD}	18	33	19	37	19	45	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	13	23	14	25	14	30	ns	7
$\overline{CAS}$ to RAS Precharge Time	t_{CRP}	5		5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	8		9		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		0		ns	
Column Address Hold Time	t_{CAH}	6		7		10		ns	
Column Address to RAS Lead Time	t_{RAL}	23		25		30		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	39		44		55		ns	
Read Command Set-Up Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		0		ns	8,9
Write Command Hold Time	t_{WCH}	6		6		10		ns	
Write Command Pulse Width	t_{WP}	6		6		10		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	12		13		13		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	12		13		13		ns	

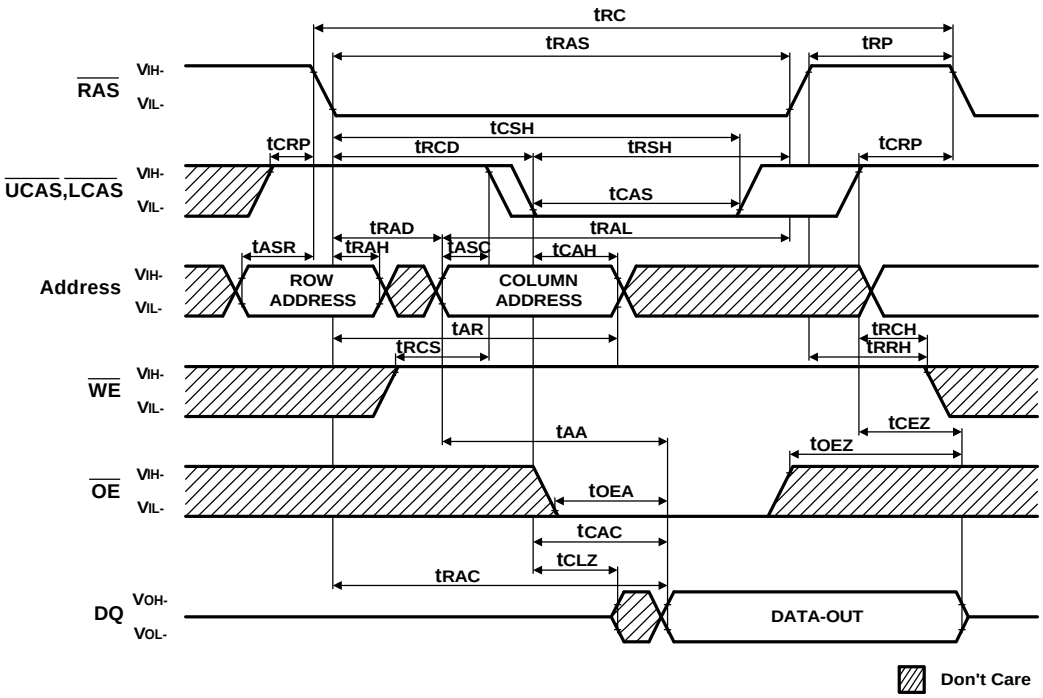
AC Characteristics

Parameter	Symbol	45		50		60		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Data Set-Up Time	t_{DS}	0		0		0		ns	
Data Hold Time	t_{DH}	8		8		10		ns	
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	41		46		55		ns	
$\overline{RAS}$ to $\overline{WE}$ E Delay Time	t_{RWD}	59		64		79		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	24		25		32		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	34		37		47		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	0		0		0		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		24		30		32	ns	
EDO Page Mode Cycle Time	t_{PC}	18		20		25		ns	
EDO Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	52		59		63		ns	
$\overline{CAS}$ Precharge Time (EDO Page Mode)	t_{CP}	7		8		15		ns	
$\overline{RAS}$ Pulse Width (EDO Page Mode Only)	t_{RASP}	45	100K	50	100k	60	100k	ns	
Access Time from $\overline{OE}$	t_{OEA}		12		14		15	ns	
$\overline{OE}$ to Data Delay Time	t_{OED}	8		8		13		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	3	8	3	8	3	8	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	7		7		7		ns	
Data Output Hold after $\overline{CAS}$ low	t_{DOH}	5		5		5		ns	
$\overline{RAS}$ to Output High-Z	t_{REZ}	3	8	3	8	3	8	ns	
$\overline{WE}$ to Output High-Z	t_{WEZ}	3	10	3	12	3	12	ns	
$\overline{OE}$ to $\overline{CAS}$ Hold Time	t_{OCH}	8		8		8		ns	
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	8		8		8		ns	
$\overline{OE}$ Precharge Time	t_{OEP}	8		8		8		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$ -before-$\overline{RAS}$ Cycle	t_{CSR}	10		10		10		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ -before-$\overline{RAS}$ Cycle	t_{CHR}	10		10		10		ns	
Transition Time	t_T	2	50	2	50	2	50	ns	
Refresh Period	t_{REF}		16		16		16	ms	

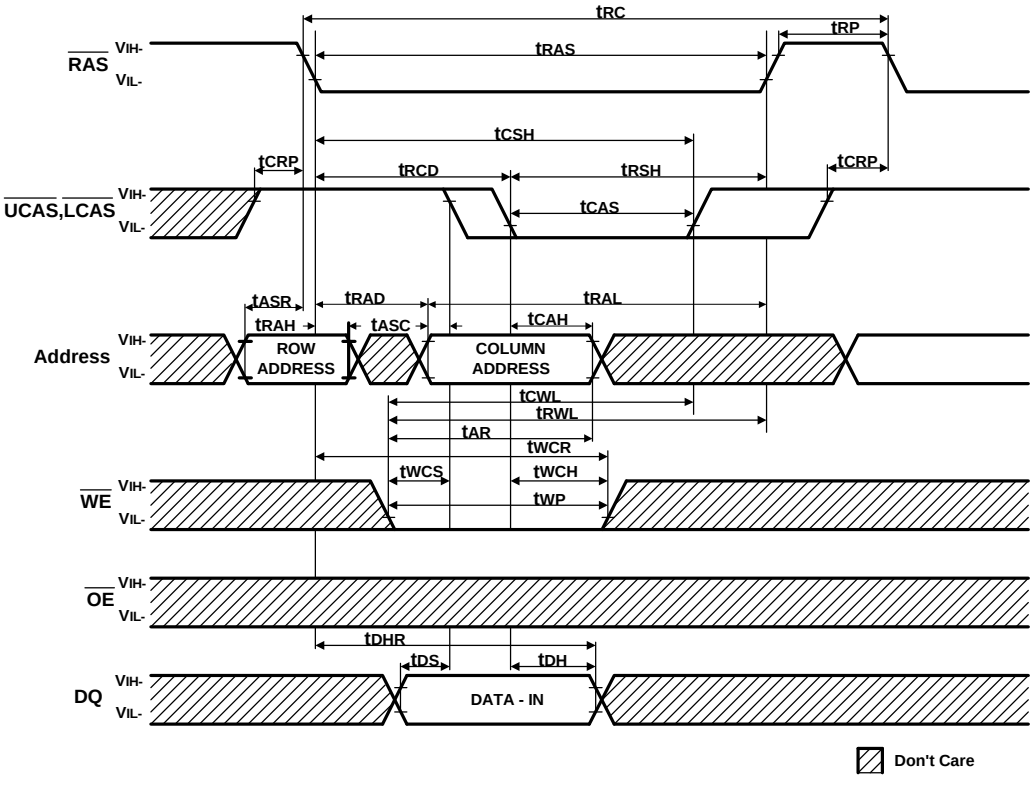
Notes:

1. Measure with a load equivalent to one TTL inputs and 50 pF.
2. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), access time will be t_{AA} dominant.
3. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RCD} (max.), access time will be controlled by t_{CAC}.
4. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle.
5. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CPA}.
6. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
7. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ of $\overline{WE}$.
11. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 1.5 ns.

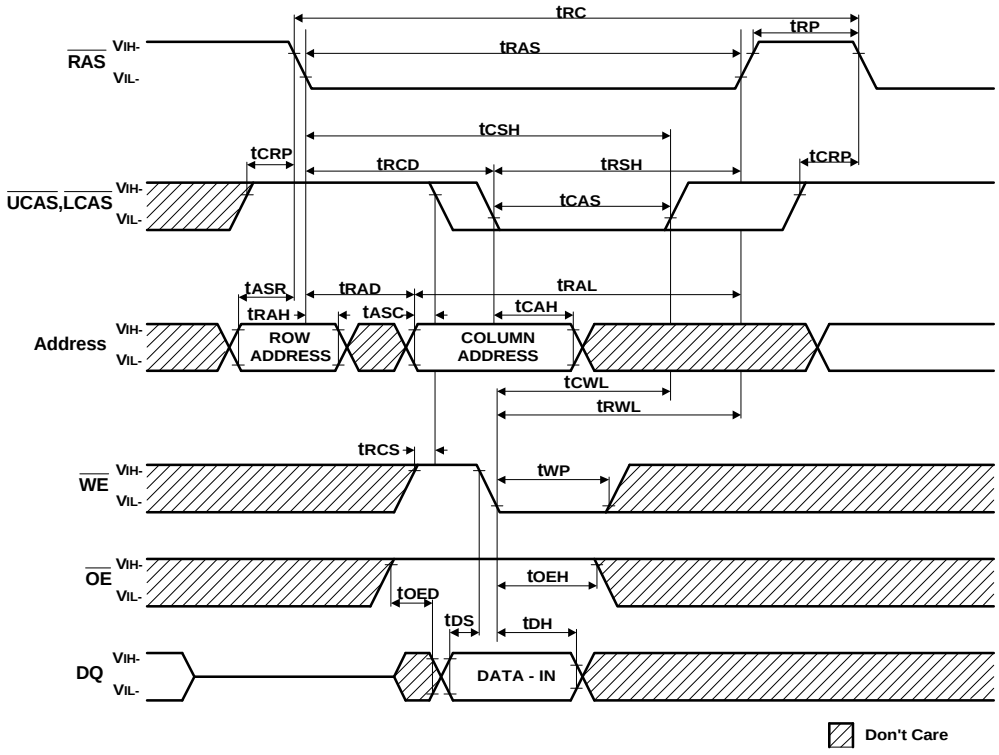
Read CYCLE Note : D_{IN} = OPEN



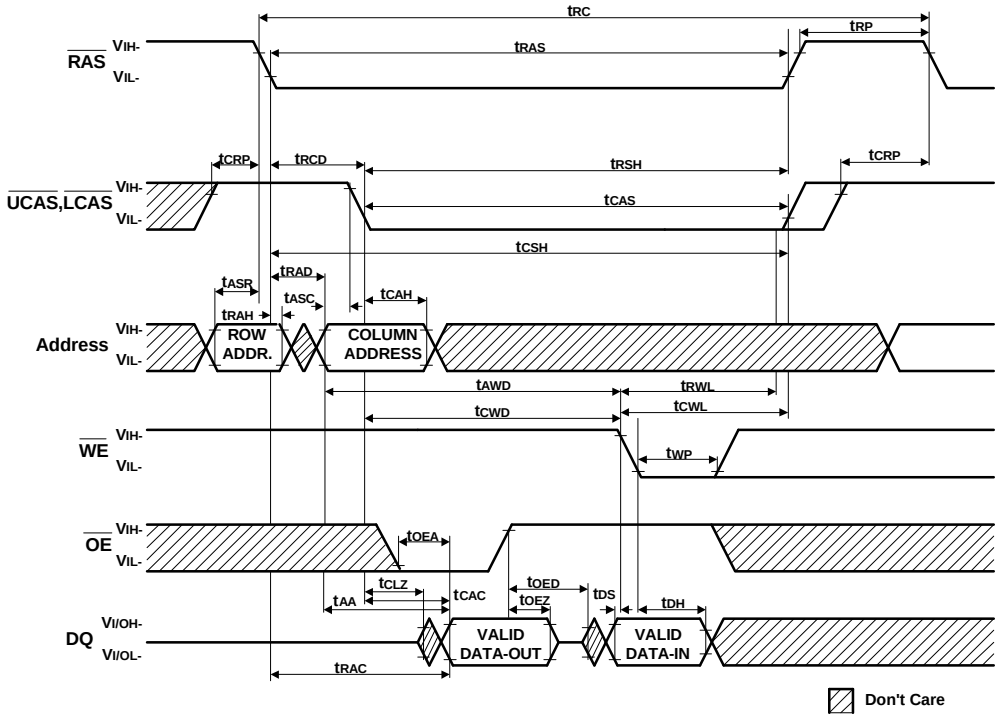
Early Write Cycle NOTE : D_{OUT} = OPEN



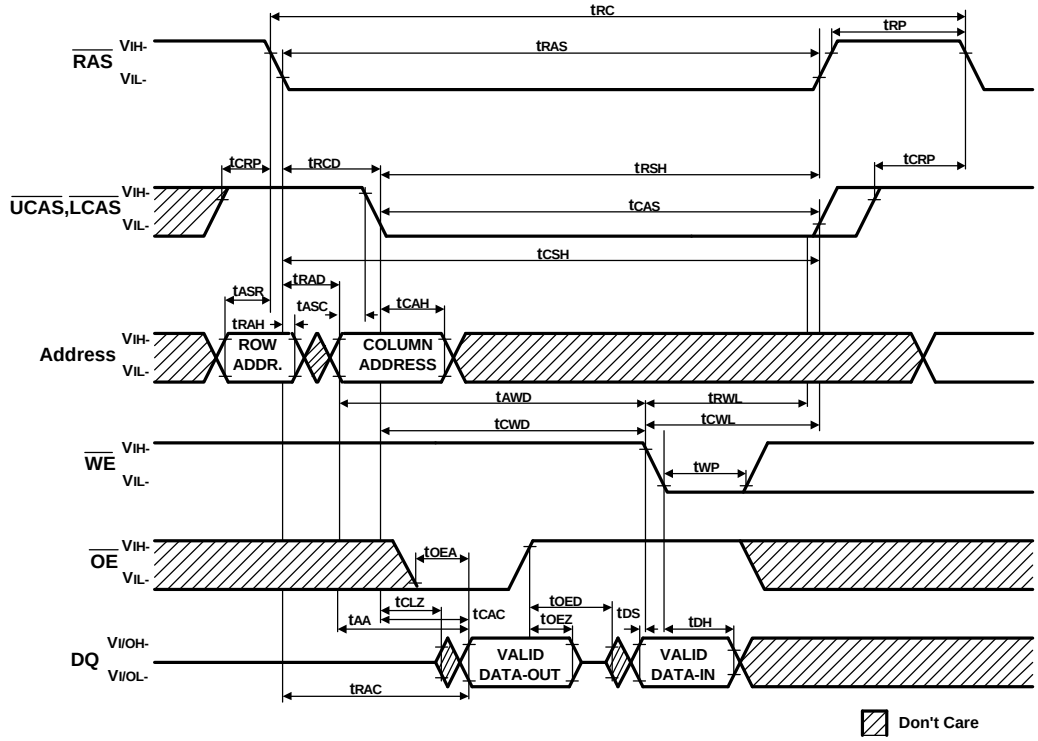
$\overline{OE}$ Controlled Write Cycle NOTE : D_{OUT} = OPEN



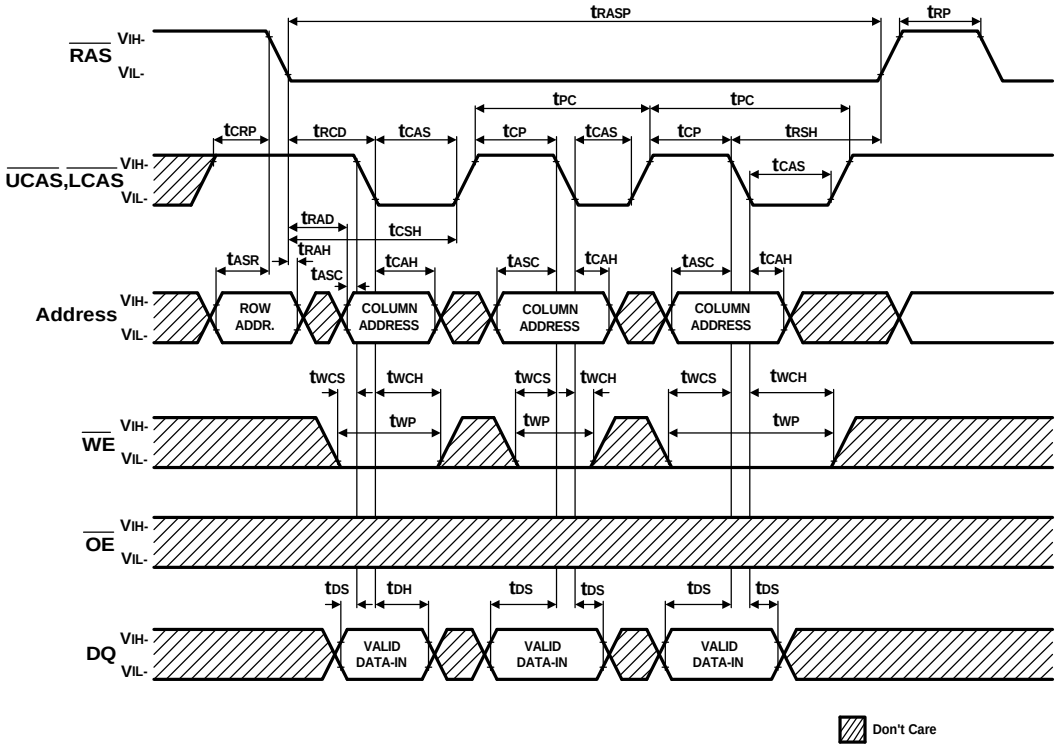
Read - Modify - Write Cycle



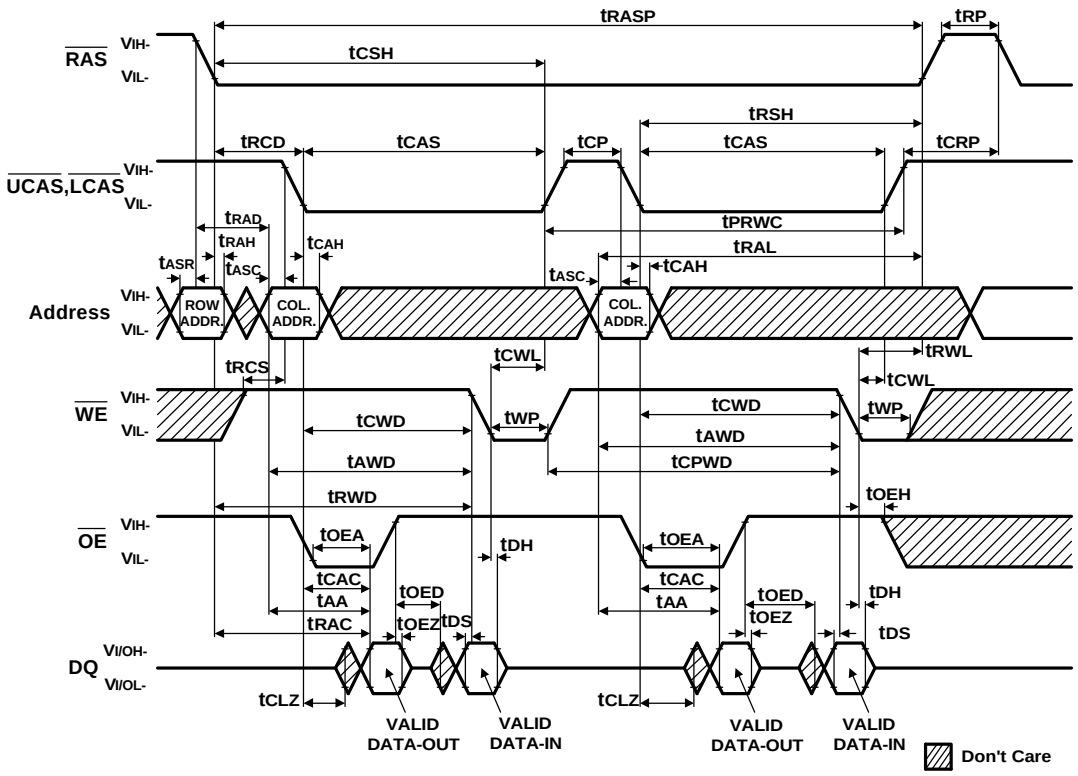
EDO Page Mode Read Cycle



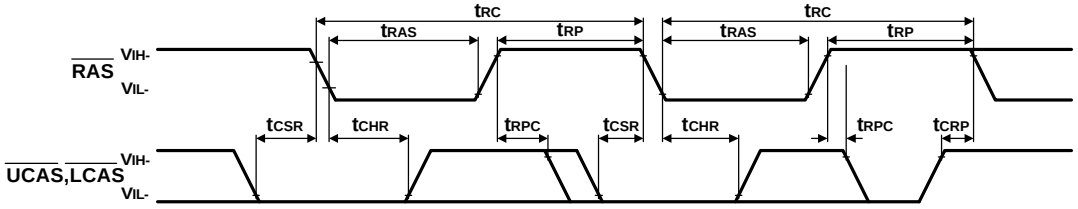
EDO Page Mode Early Write Cycle NOTE : D_{OUT} = OPEN



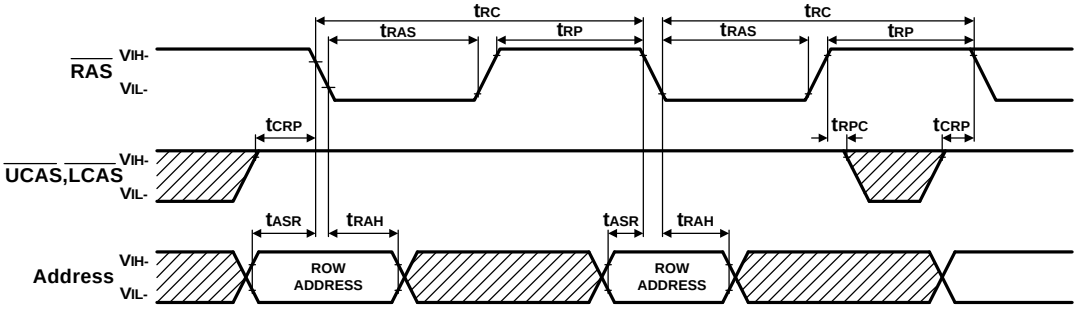
EDO Page Mode Read - Modify - Write Cycle



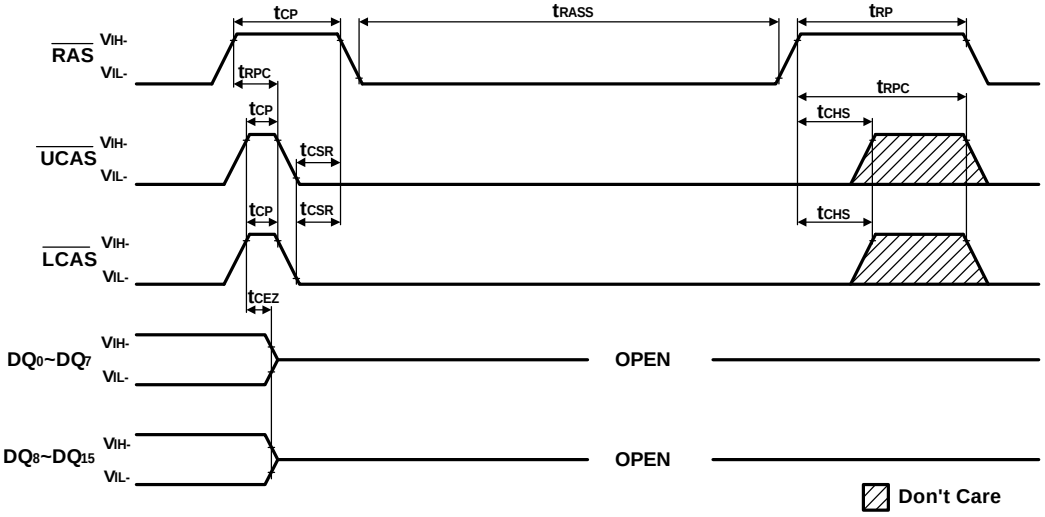
CAS - Before - RAS Refresh Cycle



RAS-Only Refresh Cycle

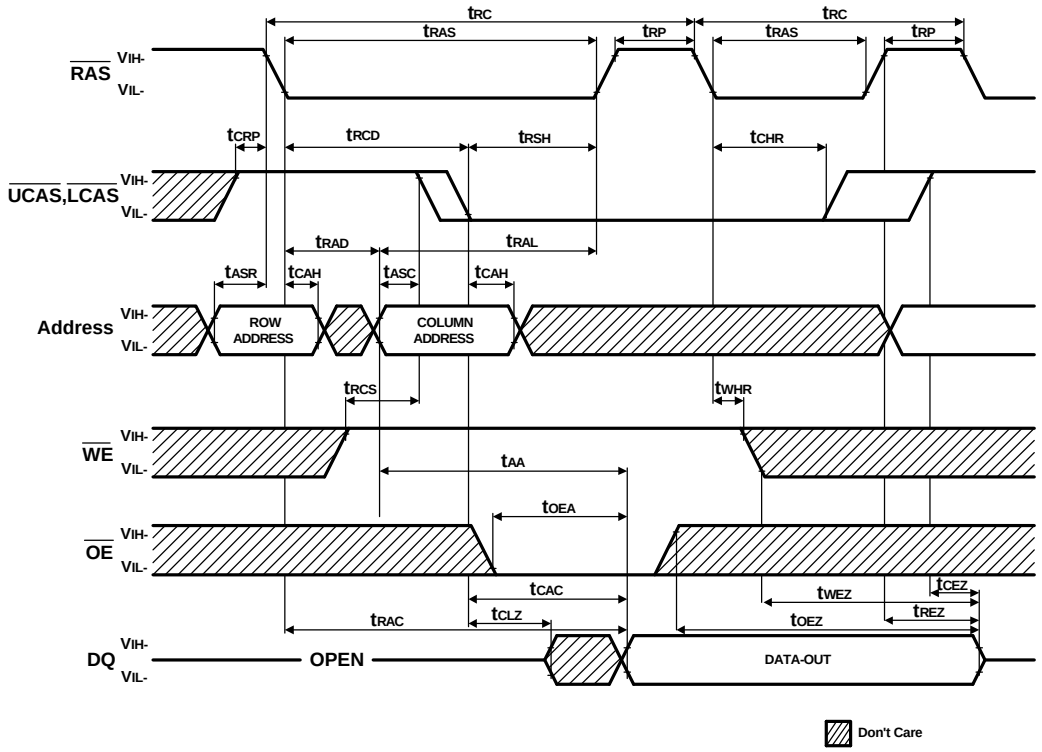


$\overline{CAS}$ - Before - $\overline{RAS}$ Self Refresh Cycle

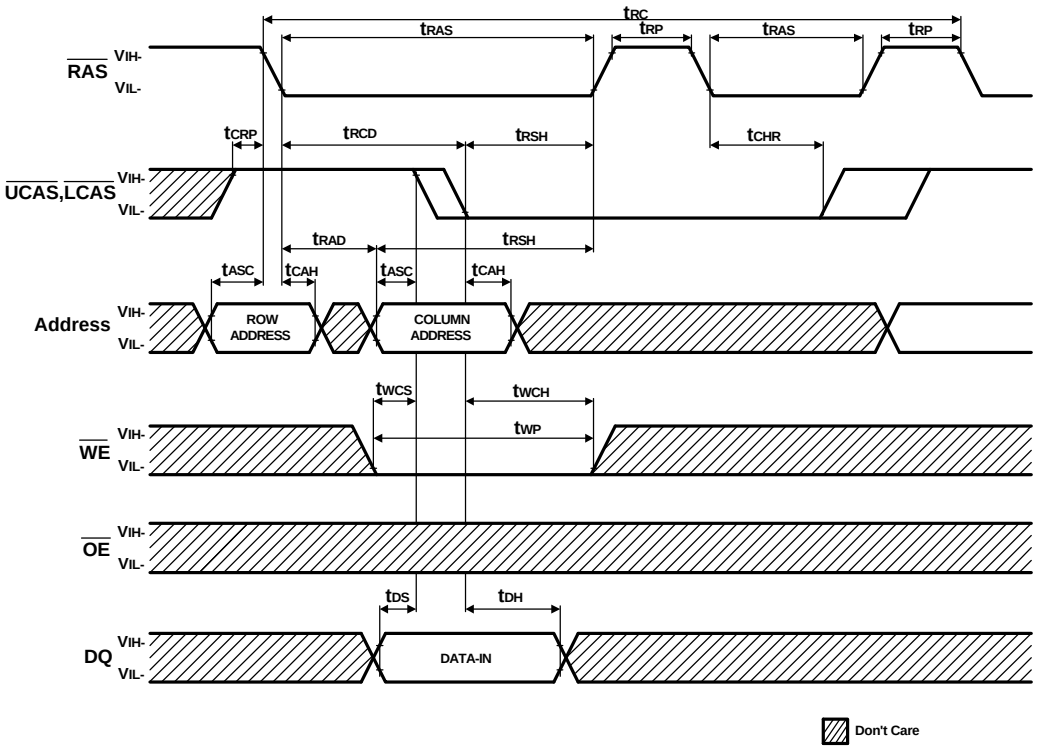


NOTE : $\overline{WE}$, $\overline{OE}$,Address = Don't care.

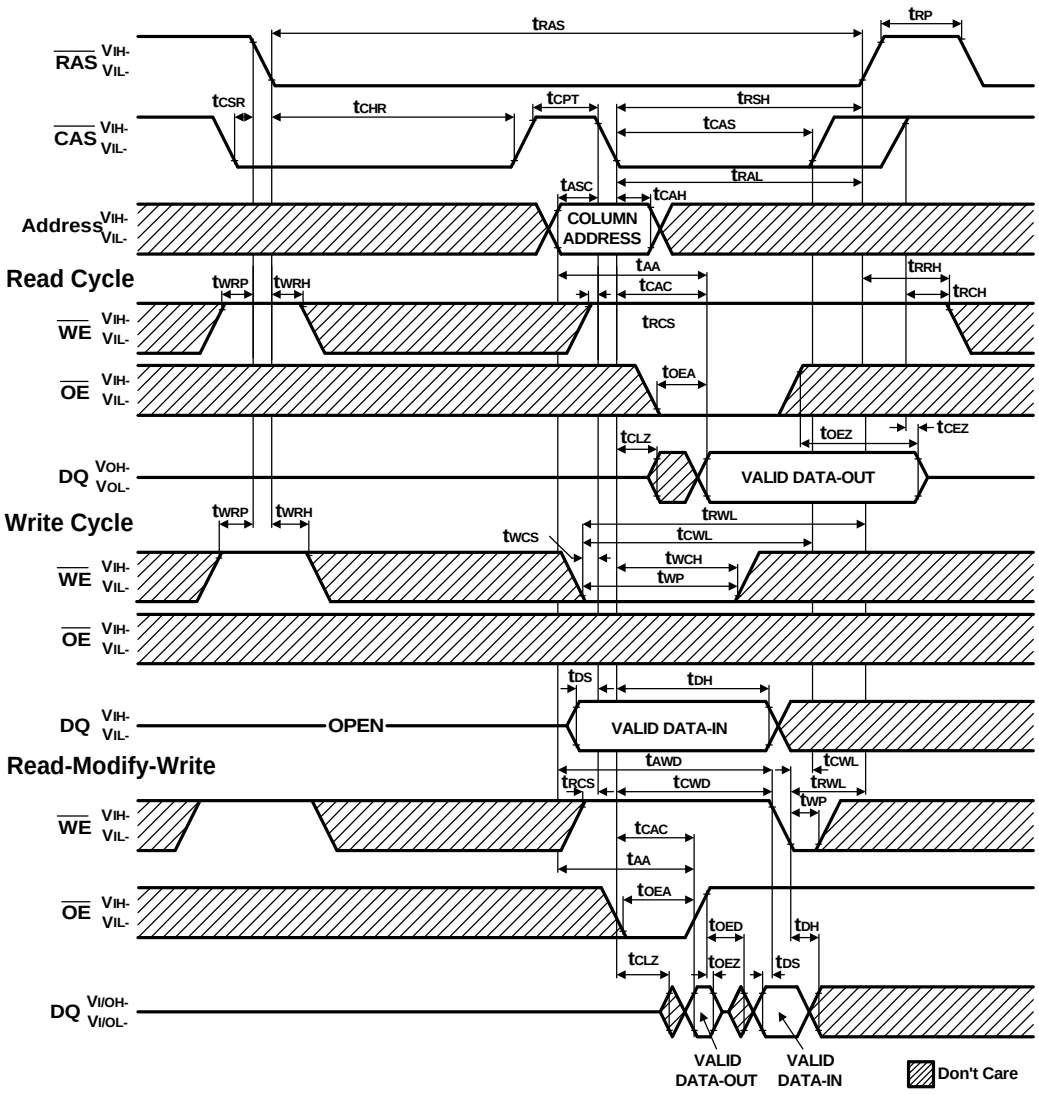
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write) NOTE : D_{OUT} = OPEN



$\overline{CAS}$ -Before- $\overline{RAS}$ Refresh Counter Test Cycle



Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*PACKAGE*
GLT416016-45J4	**45ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT416016-50J4	**50ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT416016-60J4	**60ns**	**Normal**	**EDO**	**42L 400mil SOJ**
GLT416016-45TC	**45ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**
GLT416016-50TC	**50ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**
GLT416016-60TC	**60ns**	**Normal**	**EDO**	**44/50L 400mil TSOPII**

Parts Numbers (Top Mark) Definition :

GLT 4 160 _ 16 - 45 J4

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M
-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
160 : 16M(EDO)
161 : 16M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : Mix Voltage

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

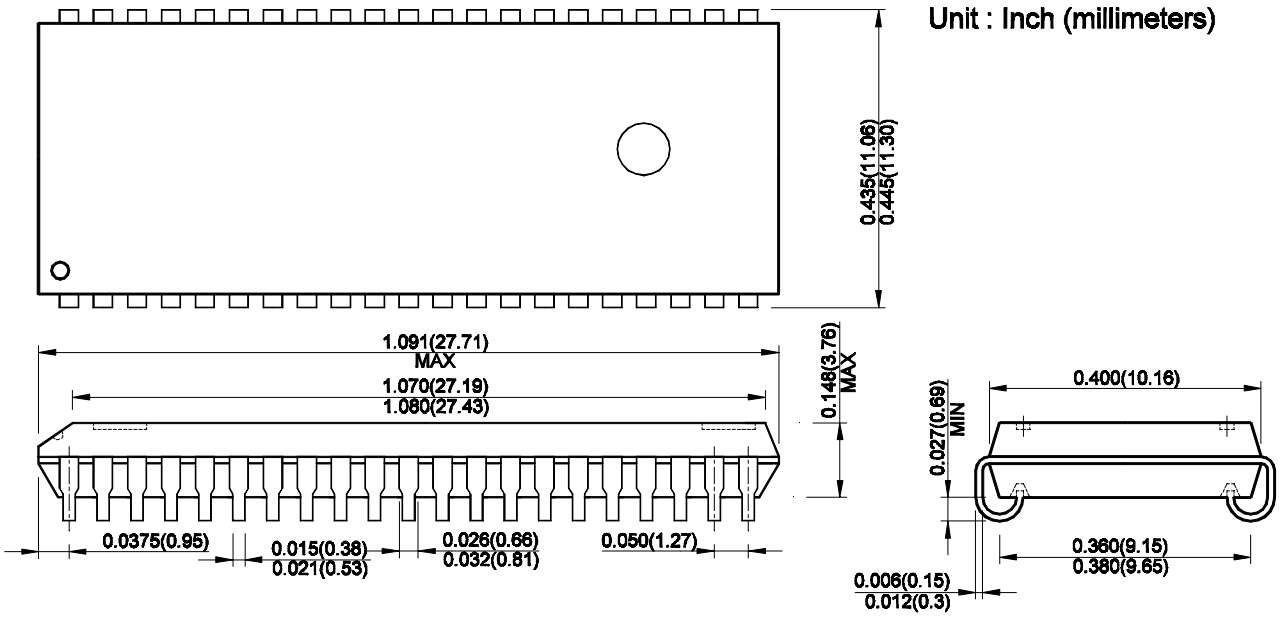
SPEED
-SRAM
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
25 : 25ns
30 : 30ns
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

Note : C→CDROM , H→HDD.
Example :
1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

40/42L 400MIL SOJ



44/50L TSOPII 400MIL