GATEFIELD™

GF260F Embedded ProASIC Product Family

Data Sheet Supplement

Highest Performance, Highest Density, Most Flexible Embedded Memory Programmable CMOS ASICs

The GF260F™ ProASIC™ product family is the highest performance, highest gate count with flexible embedded memory programmable ASIC released in the GateField™ portfolio. The GF260F family offers reprogrammable ASIC solutions to applications in the consumer, computer and communications markets.

The GF260F ProASIC product family is built upon the strength of its logic gate "only" relative, the GF250F™ ProASIC family, and enhances the well proven features and benefits by including blocks of embedded SRAM memory which are available to the programmable logic functions. These memory blocks include hardwired decoder, I/O circuits, parity generation and detection circuits, FIFO flow generation logic, and timing and control circuits as required to minimize external logic gate count and complexity while maximizing flexibility and utility.

GF250F Data Sheet Applicable

The GF250F ProASIC product family data sheet is fully applicable to the GF260F Embedded ProASIC product family. This data sheet supplement focuses on describing the enhancements and features that are specific to the GF260F Embedded ProASIC product.

Features and Benefits

- Up to 307,000 "gate array" equivalent gates provide increased system integration
- 15-20% speed increase over the GF200F product improves system performance
- Distributed and embedded memory compilation for SRAMs and FIFOs ensures optimal memory usage
- Non-volatile flash technology retains programming during power cycles
- The fine-grained architecture provides synthesis source compatibility with gate arrays
- Package options, including CPGA, MQUAD, and eSBGA, meet a wide range of system requirements
- Full compatibility with industry standard design methodology and tools improves design productivity
- Sign-off on industry-leading third party verification tools simplifies design process
- PCI compliant target and master cores enable easy interfacing to industry standard PCI buses
- Compilable JTAG support facilitates boundary-scan insertion
- Programmable security bit helps prevent customer-owned intellectual property (IP) reverse engineering

Table 1. GF260F Embedded ProASIC Product Family

Part Type	Logic Gates	Typical Logic Gates[1]	Embedded Ram Bits	Maximum Gates[2]	FlipFlops	Device I/O Pins
GF260F100	43K	20K	14K	99K	5.4K	248
GF260F180	92K	42K	23K	184K	10.8K	360
GF260F310	123K	57K	46K	307K	16.2K	424

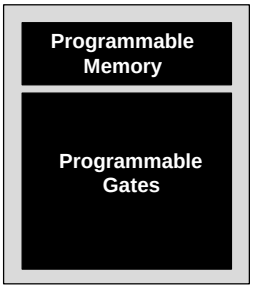
[1] Logic gates utilized in a typical design, count is exclusive of memory, actual utilization may vary.

[2] Gate count calculation for sizing designs migrating to gate arrays (100% of GF260F embedded memory used.)

Embedded Memory Floorplan

The GF260F Embedded ProASIC family shares the same architecture distributed memory compilation benefits that the GF250F product possesses but adds embedded memory for large, fast dedicated memories. As shown in figure 1, the embedded memory is located across the top of the device. Depending upon the family member, 6 to 20 blocks of memory are available to support a variety of possible memory configurations. Each block may be programmed as an independent memory or may be combined, using dedicated memory routing resources, to form larger, more complex memories. It is important to note that there are eight device I/Os on either side of memory that have slightly reduced functionality. Each set of eight I/Os can still be independently programmed as input, output, or bi-directional. However, they must share common programming for input threshold, pull-up, output drive strength and slew rate.

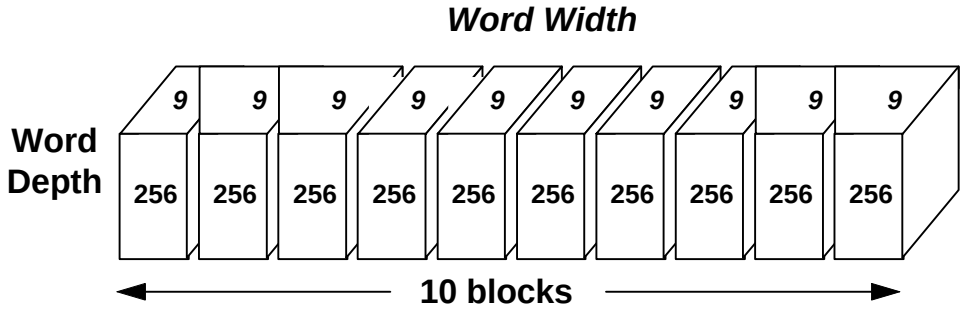
Figure 1. The GF260F Device Floorplan



Embedded Memory Configurations

The GF260F Embedded ProASIC family offers great flexibility in programming options. Up to 10 individual and unique memories may be programmed on the GF260F180 device. Each memory can be configured as synchronous or asynchronous, FIFO or SRAM, and single port or multi-port. In addition, many more characteristics are programmable, including FIFO flags, parity control, depth and width. These memories are designed to operate in excess of 66MHz in most configurations. Each of the 10 blocks contains a 9-bit wide x 256 word deep memory. The memory blocks shown in figure 2 may be paralleled to form wider memories or stacked to form deeper memories. The MEMORYmaster™ compiler facilitates the paralleling of 2, 4, and 8 blocks for wider words. This provides optimal bit widths of 9 (1 block), 18, 36, and 72. In practice, the compiler will allow any bit width up to 72. It is important to note that if an intermediate bit width is chosen, such as 16 bits, the remaining two bits are no longer accessible for other memories. The compiler enables optimal memory stacking in 256 word increments. Once again, however, any word depth may be compiled from 1 to 2,560 words.

Figure 2. GF260F180 Memory Block Architecture



Whereas FPGA/CPLD vendors typically provide single port memories that can be partitioned into a dual port memory at the loss of half the memory, each GF260F block is designed and optimized as a two-port memory (1r1w). This provides 23,040 total memory bits for dual port and single port memory usage in the GF60F180 device. In addition, GateField's unique architecture allows memory paralleling to form memories of up to 11 memory ports (10r1w).

Figure 3 shows an example of optimal memory usage. Three memories have been compiled with various widths and depths using all 10 blocks and consuming all 23,040 bits of available memory. Figure 4 shows an example of doubling up memory to create extra read ports. In this example, all 10 blocks of the GF260F180 are fully used, but only yield an effective 6,912 bits of multiple port memories.

Figure 3. Optimal Memory Usage Example for the GF260F180

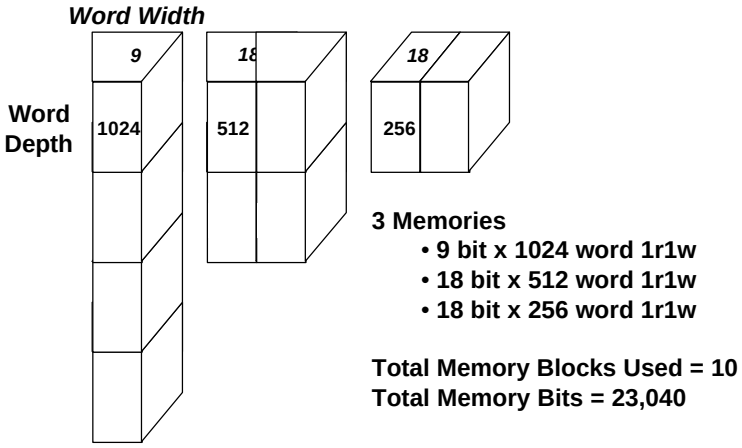
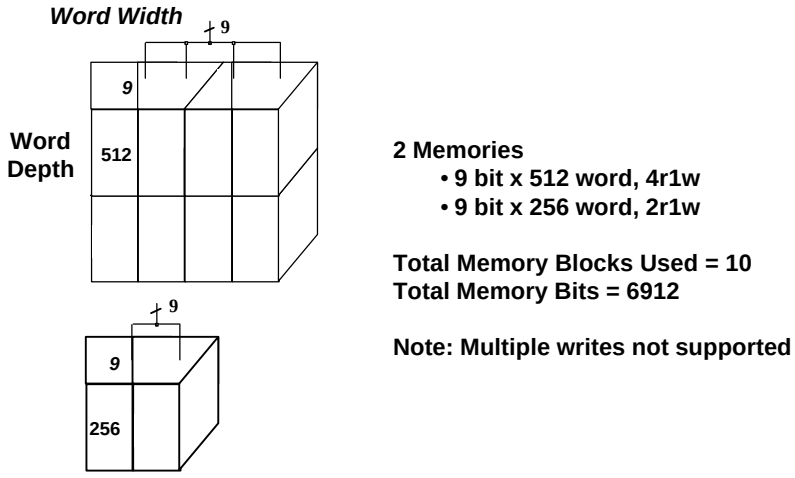


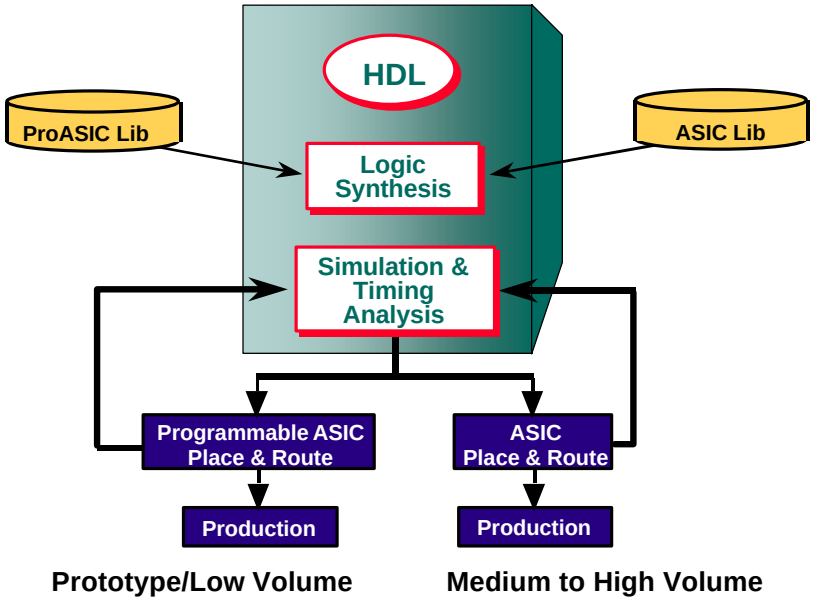
Figure 4. GF260F180 Example Showing Multiport Memory Usage



ASIC Design Environment

The ProASIC product design environment provides significant advantages to the design engineer and program manager. It utilizes the same robust VHDL and Verilog HDL descriptions that are targeted for gate arrays and standard cells. This frees the designer from the limitations and special idiosyncrasies imposed upon HDL by FPGA vendors. Furthermore, GateField does not require special FPGA tools for synthesis and the so-called "architectural mapping." Standard ASIC tools such as Design Compiler, VSS, Verilog XL, QuickSim II, VCS, Motive, Leonardo, etc. are supported. This streamlines the design environment and enables the design team to focus on a single suite of design tools, whether the design is targeted for gate arrays or programmable ASICs. The ProASIC design flow also ensures a seamless transition to your ASIC vendor of choice should production volumes warrant a migration to a gate array or a standard cell product. As shown in figure 5, with identical HDL, identical design tools and flow, migration to ASICs for high volume production is greatly simplified. Conversely, migration from ASICs to GateField's ProASIC technology is also unburdened by traditional FPGA design requirements. Supported EDA environments include Mentor Graphics (Falcon Framework 8.5), Synopsys (Design Compiler 3.5a and later), Quad Design Technologies (Motive 5.0 and later), Viewlogic Systems (Powerview 5.1) and Exemplar (Leonardo 4.0.3).

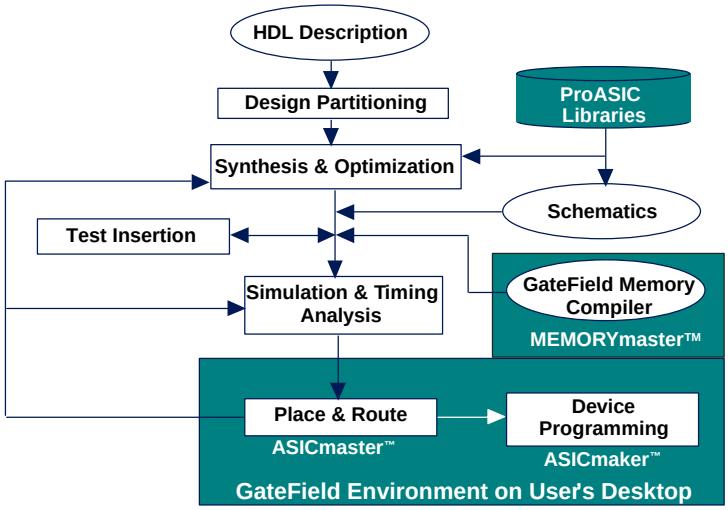
Figure 5. Common Design Environment Simplifies Migrations



Once the design has been synthesized and the appropriate embedded memory configurations have been defined through GateField's MEMORYmaster compiler, it is ready for simulation and timing analysis. GateField's ProASIC libraries and MEMORYmaster generated simulation and timing models provide the database required by the well-accepted and proven ASIC design environment.

As soon as the design meets the functional and pre-layout timing specifications, it is ready for place and route. To facilitate this activity, GateField has created a desktop software package, ASICmaster™, which is ideally suited for the busy engineer. As an integral part of the ProASIC design flow (figure 6), ASICmaster runs on Sun and HP workstations, as well as on Windows NT platforms. It accepts standard ASIC formatted netlists, performs place and route of the design into the selected device and provides back annotated delay information for simulation. This is all accomplished through the software's easy to use interface. Within minutes, the average design engineer will be up and running.

Figure 6. The ProASIC Design Flow



The ASICmaster software also contains very powerful interactive layout capabilities for the experienced user. Preferred placement, routing changes and custom clock tree configurations are all possible. Once the design is finalized, the layout is downloaded into GateField's ASICmaker™ device programmer, shown in figure 7, for ProASIC part programming. The ASICmaker device programmer supports interchangeable modules for each package type available and an In-System-Programming module to facilitate reprogramming ProASIC devices already resident in a board or system. The ASICmaster and ASICmaker tools ensure fast and efficient programmable ASIC implementations for the novice or expert user.

Figure 7. GateField's ASICmaker Device Programmer

Specifications

Electrical specifications for the GF260F Embedded ProASIC devices are provided in the GF250F ProASIC product family data sheet.

Macrocells, as well as programmable I/O specifications, are consistent with the GF250F family and, therefore, transferable.

This chapter focuses on the embedded memory part of the GF260F Embedded ProASIC family. It describes in detail the SRAM and FIFO interface signals and includes timing diagrams that show the relationships of various signals as they pertain to the compiled embedded memories.

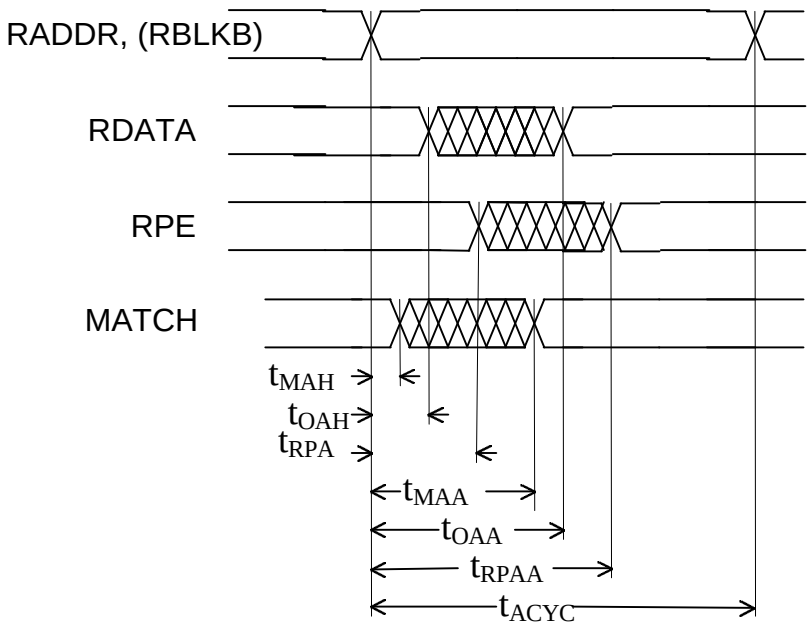
MEMBLOCK SRAM Interface Signals

SRAM Signal	Hookup	Bits	In/Out	Description
CLK	Route	1	IN	Read/Write synchronization clock, used in SYNC mode, only.
RADDR<0:7>	Route	8	IN	Read address.
RBLKB	Route/ Config.	1	IN	Negative true read block select. Selects data out strobe timing in synchronous mode.
RDB	Route/ Config.	1	IN	Negative true read pulse.
WADDR<0:7>	Route	8	IN	Write address.
WBLKB	Route/ Config.	1	IN	Negative true write block select.
WDATA<0:8>	Route	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true.
WRB	Route	1	IN	Negative true write pulse.
MATCH	Route	1	OUT	Flag that indicates matching read and write addresses and block selects, during asynchronous mode.
RDATA<0:8>	Route	9	OUT	Output data bits <0:8>
RPE	Route	1	OUT	Read parity error.
WPE	Route	1	OUT	Write parity error.
FIFO	Config.	1	IN	Selects FIFO mode when high and SRAM mode when low.
PARGEN	Config.	1	IN	Generates data input parity when high, none when low.
PARODD	Config.	1	IN	Selects odd parity generation/detect when high, even when low.
SYNC	Config.	1	IN	Selects synchronous mode when high and asynchronous mode when low.

Enclosed Timing Diagrams — SRAM Mode:

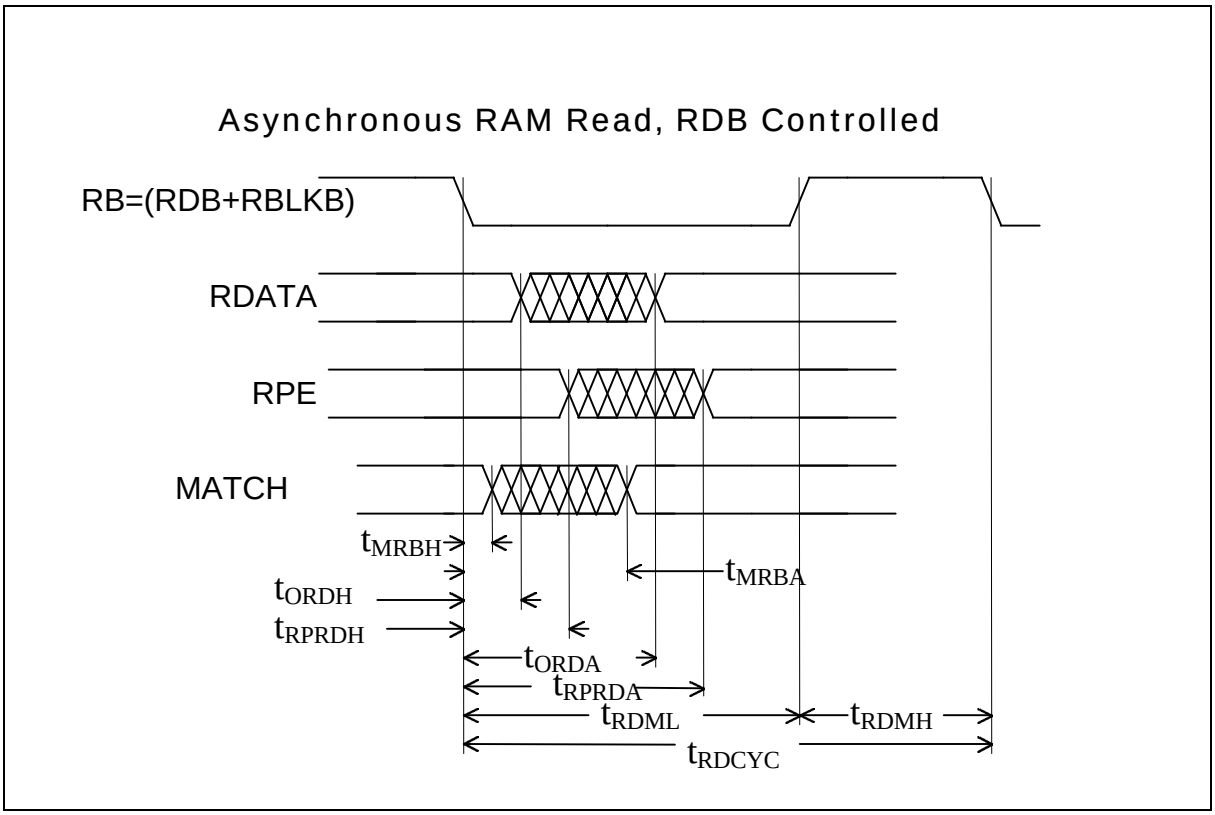
- Asynchronous RAM Read, Address Controlled
- Asynchronous RAM Read, RDB Controlled
- Asynchronous RAM Write
- Asynchronous RAM Write while Reading the Same Location
- Synchronous RAM Read, Access Timed Output Strobe
- Synchronous RAM Read, Pipeline Mode Outputs
- Synchronous RAM Write

Asynchronous RAM Read, Address Controlled, RDB=0



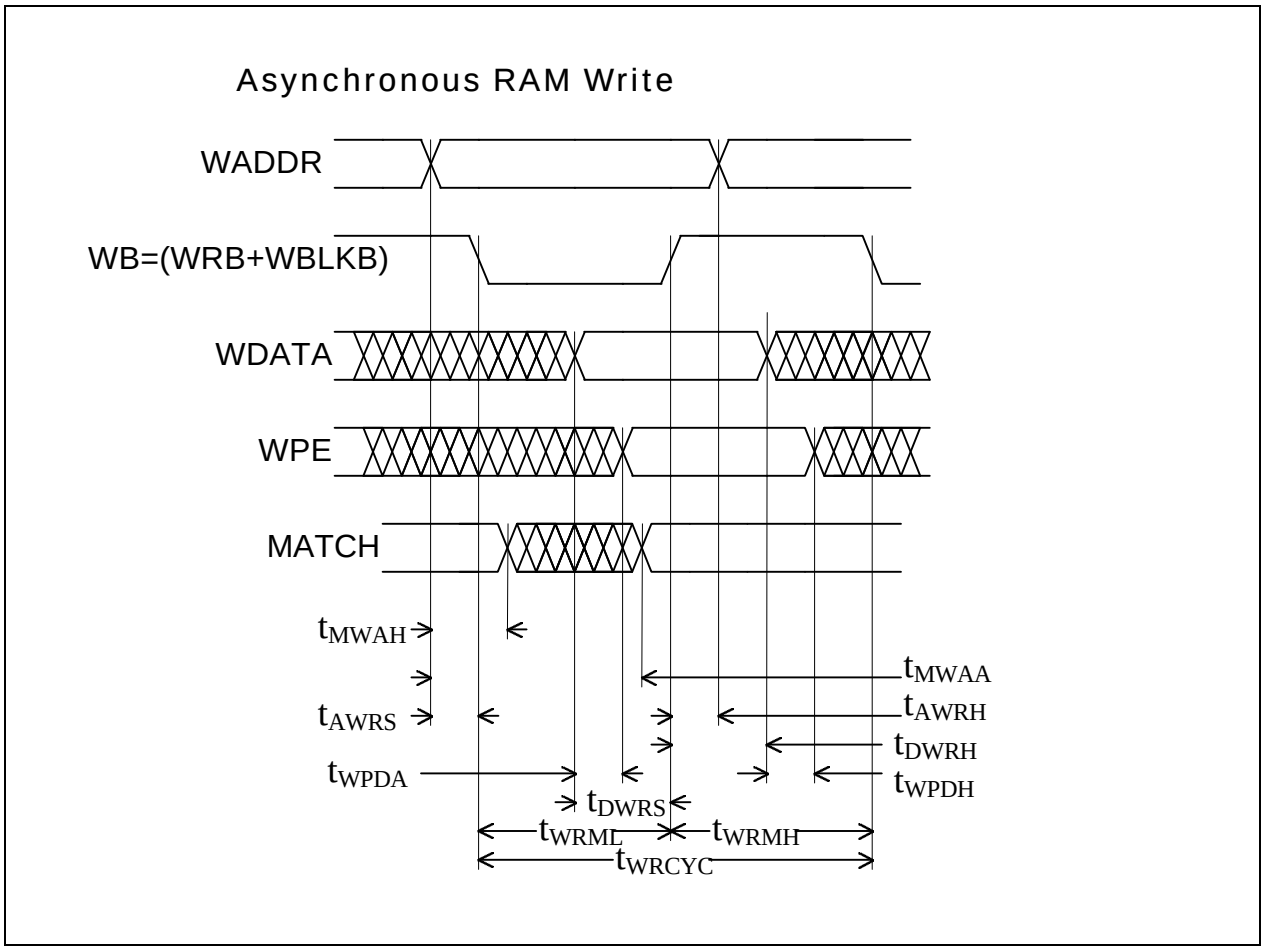
T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
ACYC	Read cycle time	15.0		ns	
MAA	New MATCH access from RADDR stable	10.0		ns	Write address is stable.
MAH	Old MATCH hold from RADDR stable		3.0	ns	Write address is stable.
OAA	New RDATA access from RADDR stable	16.0		ns	
OAH	Old RDATA hold from RADDR stable		6.0	ns	
RPAA	New RPE access from RADDR stable	20.0		ns	
RPAH	Old RPE hold from RADDR stable		6.0	ns	



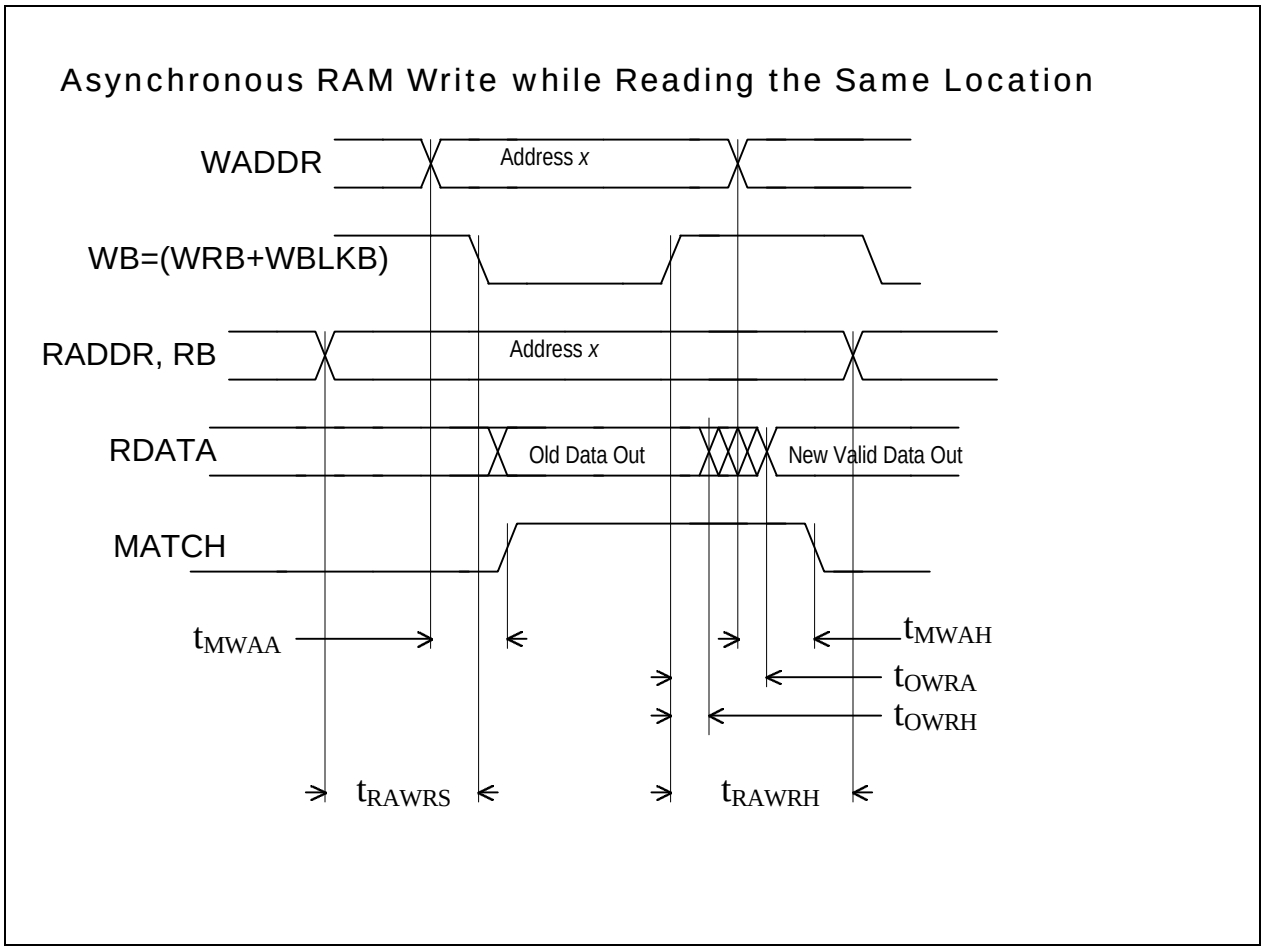
T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
MRBA	New MATCH access from RBLKB stable, either edge.	10.0		ns	Write address is stable.
MRBH	Old MATCH hold from RBLKB stable, either edge.		3.0	ns	Write address is stable.
ORDA	New RDATA access from RB ↓	15.0		ns	
ORDH	Old RDATA valid from RB ↓		6.0	ns	
RDCYC	Read cycle time	15.0		ns	
RDMH	RB high phase	6.0		ns	Inactive setup to new cycle
RDML	RB low phase	6.0		ns	Active
RPRDA	New RPE access from RB ↓	19.0		ns	
RPRDH	Old RPE valid from RB ↓		6.0	ns	



T_J= 0 C to 110 C; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
AWRH	WADDR hold from WB ↑	2.0		ns	
AWRS	WADDR setup to WB ↓	1.0		ns	
DWRH	WDATA hold from WB ↑	3.0		ns	
DWRS	WDATA setup to WB ↑	1.0		ns	PARGEN is inactive.
DWRS	WDATA setup to WB ↑	5.0		ns	PARGEN is active.
MWAA	New MATCH access from WADDR, WBLKB stable	10.0		ns	READ address is stable.
MWAH	Old MATCH valid hold from WADDR, WBLKB stable		3.0	ns	READ address is stable.
WPDA	WPE access from WDATA	6.0		ns	WPE is invalid while PARGEN is active.
WPDH	WPE hold from WDATA		2.0	ns	
WRCYC	Cycle time	15.0		ns	
WRMH	WB high phase	6.0		ns	Inactive
WRML	WB low phase	6.0		ns	Active

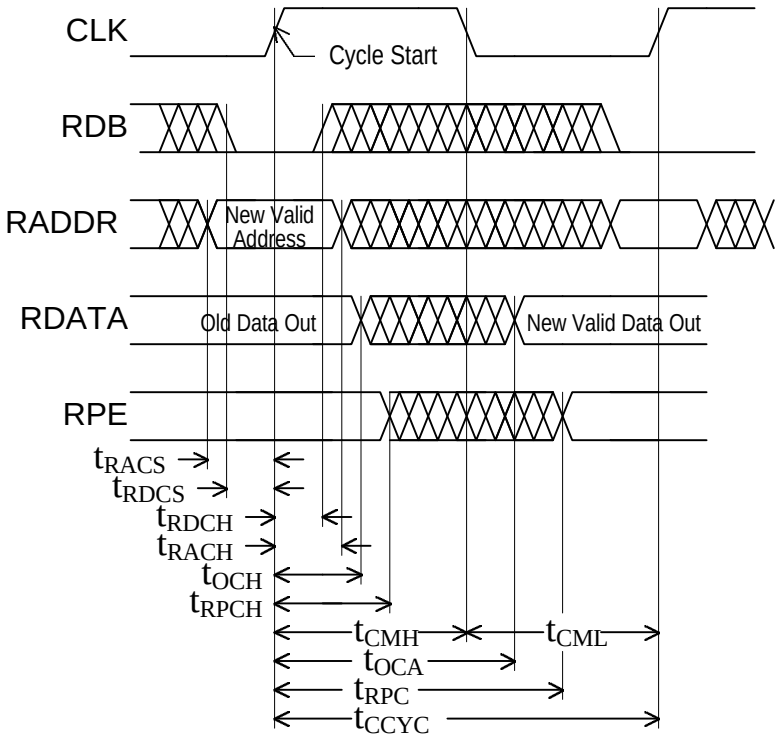


T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
MWAA	New MATCH access from WADDR, WBLKB stable	10.0		ns	READ address is stable.
MWAH	Old MATCH valid hold from WADDR, WBLKB stable		3.0	ns	READ address is stable.
OWRA	RDATA access from WB ↑	6.0		ns	READ address is stable.
OWRH	Old RDATA hold from WB ↑		1.0	ns	READ address is stable.
RAWRH	RADDR & RB hold from WB ↑	10.0		ns	
RAWRS	RADDR & RB setup to WB ↓	10.0		ns	

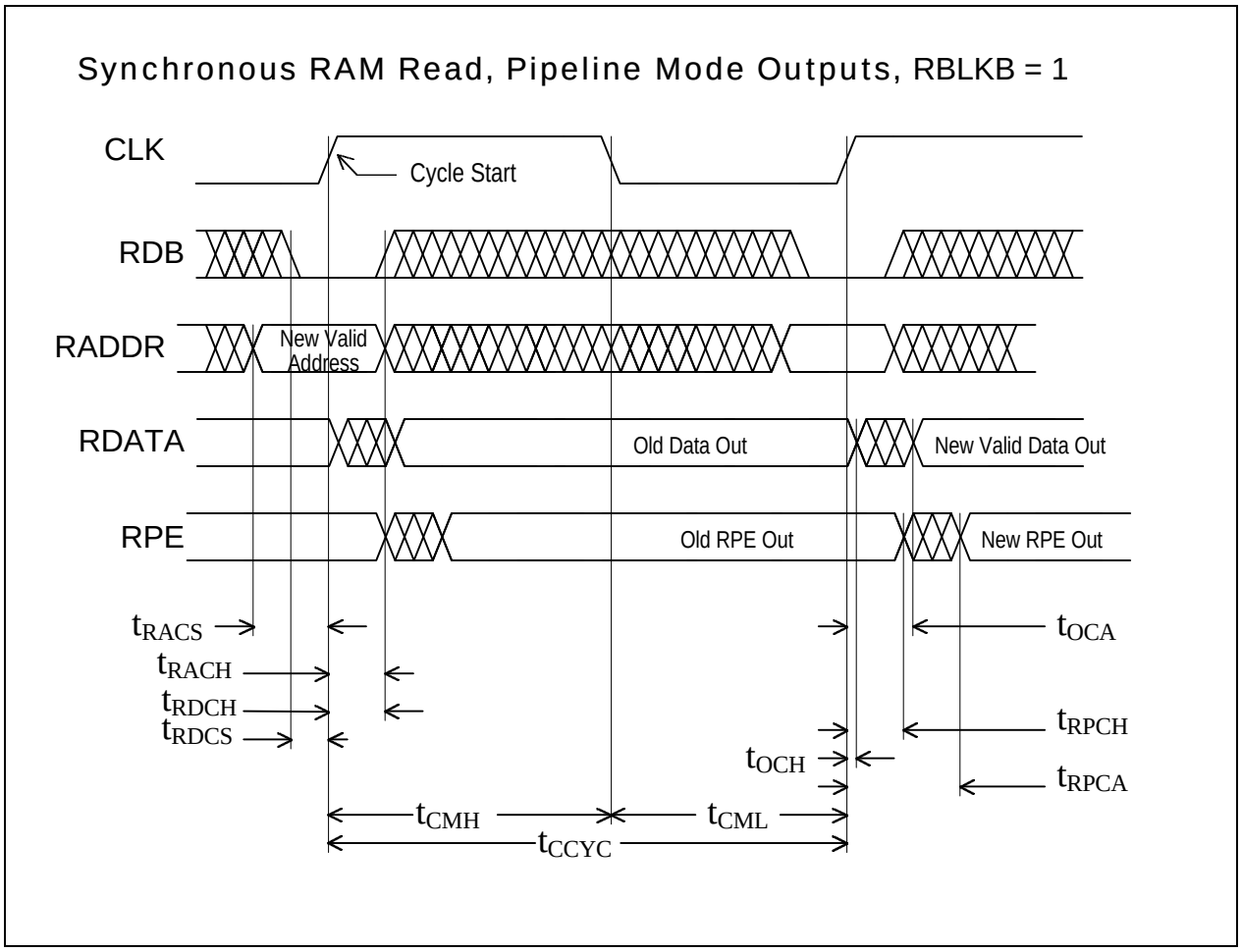
NOTE: Other simultaneous read and write accesses to the same location may produce unexpected or invalid RDATA.

Synchronous RAM Read, Access Timed Output Strobe, RBLKB = 0



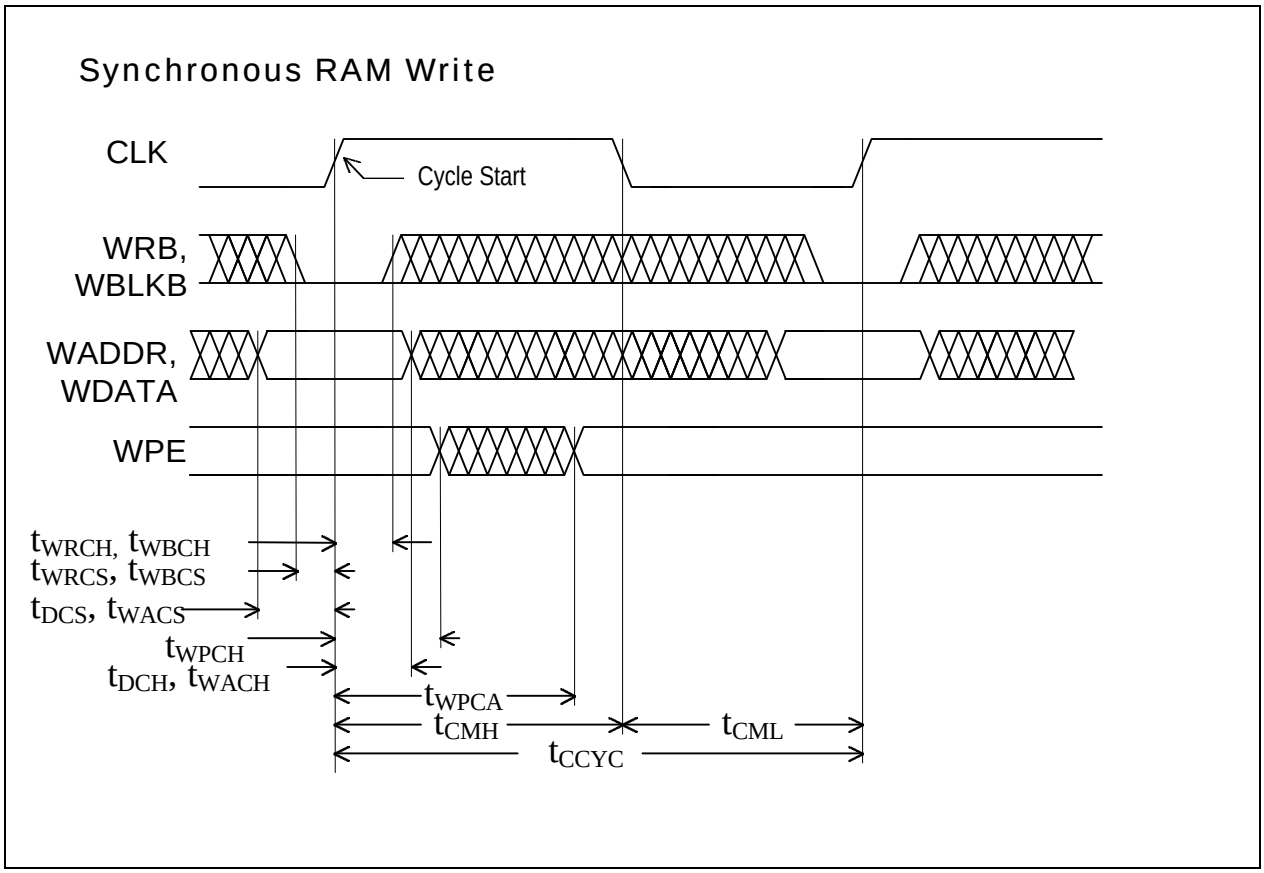
T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
OCA	New RDATA access from CLK ↑	15.0		ns	
OCH	Old RDATA valid from CLK ↑		6.0	ns	
RACH	RADDR hold from CLK ↑	1.0		ns	
RACS	RADDR setup to CLK ↑	2.0		ns	
RDCH	RDB hold from CLK ↑	1.0		ns	
RDCS	RDB setup to CLK ↑	2.0		ns	
RPCA	New RPE access from CLK ↑	19.0		ns	
RPCH	Old RPE valid from CLK ↑		6.0	ns	



T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
OCA	New RDATA access from CLK ↑	4.0		ns	
OCH	Old RDATA valid from CLK ↑		1.5	ns	
RACH	RADDR hold from CLK ↑	1.0		ns	
RACS	RADDR setup to CLK ↑	2.0		ns	
RDCH	RDB hold from CLK ↑	1.0		ns	
RDCS	RDB setup to CLK ↑	2.0		ns	
RPCA	New RPE access from CLK ↑	8.0		ns	
RPCH	Old RPE valid from CLK ↑		2.0	ns	



T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
DCH	WDATA hold from CLK ↑	1.0		ns	
DCS	WDATA setup to CLK ↑	2.0		ns	
WACH	WADDR hold from CLK ↑	1.0		ns	
WACS	WADDR setup to CLK ↑	2.0		ns	
WPCA	New WPE access from CLK ↑	6.0		ns	WPE is invalid while
WPCH	Old WPE valid from CLK ↑		1.0	ns	PARGEN is active.
WRCH, WBCH	WRB & WBLKB hold from CLK ↑	1.0		ns	
WRCS, WBCS	WRB & WBLKB setup to CLK ↑	2.0		ns	

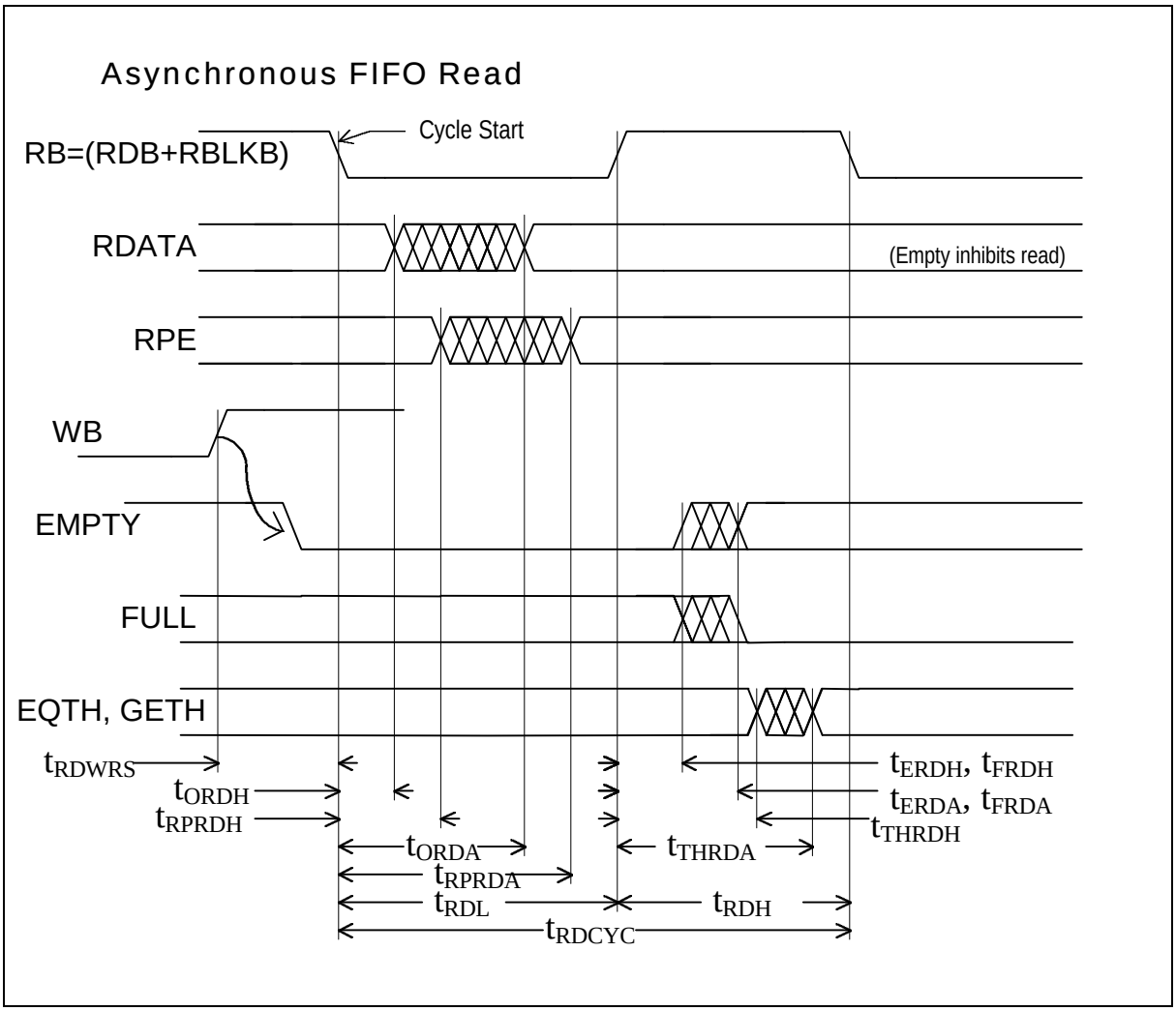
NOTE: On simultaneous read and write accesses to the same location WDATA is output to RDATA

MEMBLOCK FIFO Interface Signals

FIFO Signal	Hookup	Bits	In/Out	Description
CLK	Route	1	IN	Read/Write synchronization clock, used in SYNC mode; it must be ì0î in ASYNC mode.
LEVEL <0:7>	Route/ Config.	8	IN	Direct configuration implements static flag logic.
RBLKB	Route/ Config.	1	IN	Negative true read block select. Selects data out strobe timing in synchronous mode.
RDB	Route/ Config.	1	IN	Negative true read pulse.
RESETB	Route	1	IN	Negative true reset for FIFO pointers.
WBLKB	Route/ Config.	1	IN	Negative true write block select.
WDATA<0:8>	Route	9	IN	Input data bits <0:8>, <8> will be generated if PARGEN is true.
WRB	Route	1	IN	Negative true write pulse.
FULL, EMPTY	Route	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read.
EQTH, GEQTH	Route	2	OUT	EQTH is true when the FIFO holds (LEVEL) words. GEQTH is true when the FIFO holds (LEVEL) words or more. These flags are only available in the full 256x9 FIFO mode (LGDEP=111)
RDATA<0:8>	Route	9	OUT	Output data bits <0:8>
RPE	Route	1	OUT	Read parity error.
WPE	Route	1	OUT	Write parity error.
FIFO	Config.	1	IN	Selects FIFO mode when high and SRAM mode when low.
LGDEP <0:2>	Config.	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARGEN	Config.	1	IN	Generates data input parity when high, none when low.
PARODD	Config.	1	IN	Selects odd parity generation/detect when high, even when low.
SYNC	Config.	1	IN	Selects synchronous mode when high and asynchronous mode when low.

Enclosed Timing Diagrams — FIFO Mode:

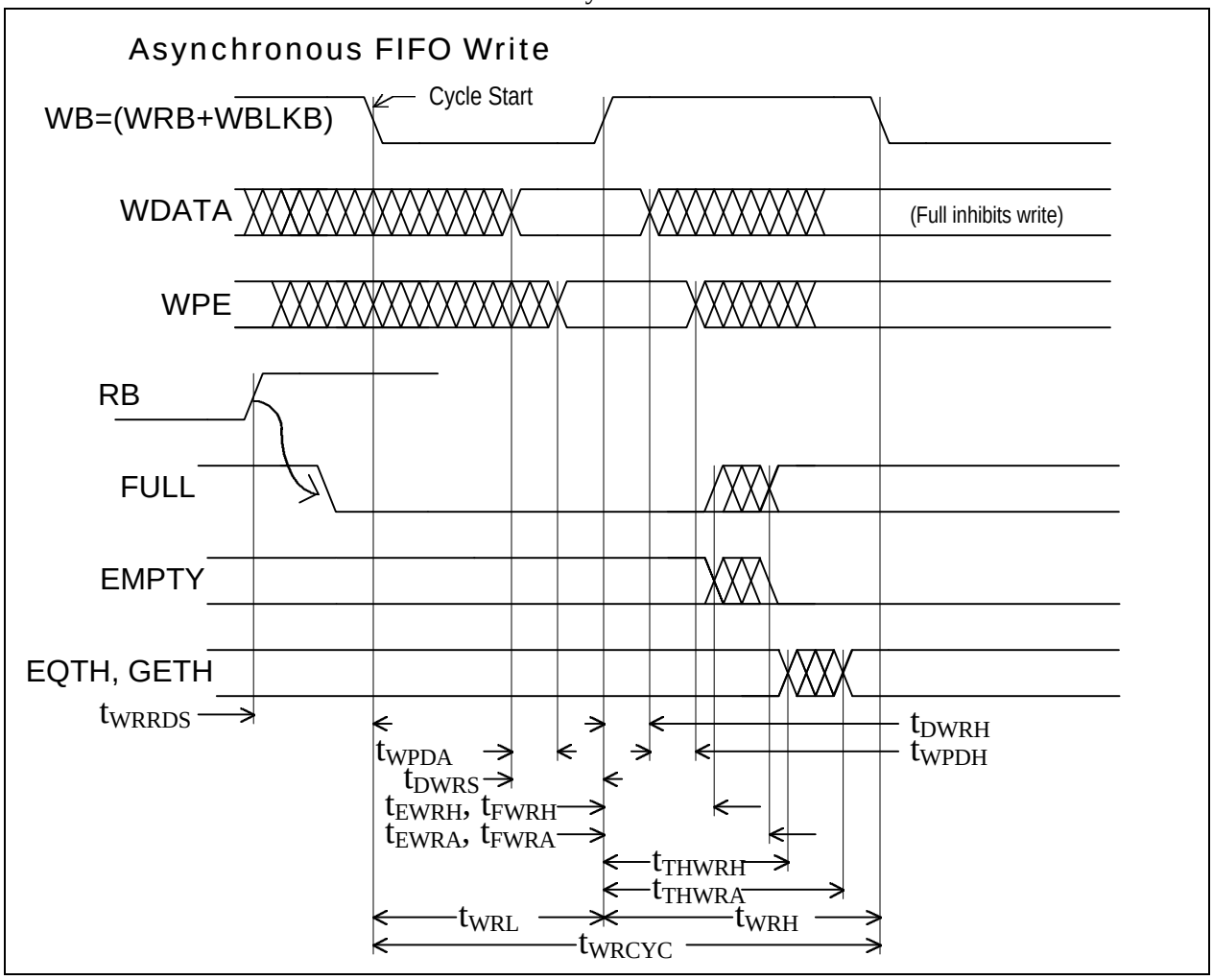
- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe
- Synchronous FIFO Read, Pipeline Mode Outputs
- Synchronous FIFO Write
- FIFO Reset



T_J= 0 C to 110 C; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
ERDA	New EMPTY access from RB ↑	6.0*		ns	* At fast cycles, ERDA & FRDA = MAX((15.0ns-RDL), 6.0ns)
FRDA	FULL↓ access from RB ↑	6.0*		ns	
ORDA	New RDATA access from RB ↓	15.0		ns	
ORDH	Old RDATA valid from RB ↓		6.0	ns	
RDCYC	Read cycle time	15.0		ns	
RDWRS	WB ↑, clearing EMPTY, setup to RB ↓	6.0**		ns	Enabling the read operation.
			2.0	ns	Inhibiting the read operation.
RDH	RB high phase	6.0		ns	Inactive
RDL	RB low phase	6.0		ns	Active
RPRDA	New RPE access from RB ↓	19.0		ns	
RPRDH	Old RPE valid from RB ↓		8.0	ns	
THRDA	EQTH or GETH access from RB↑	9.0		ns	

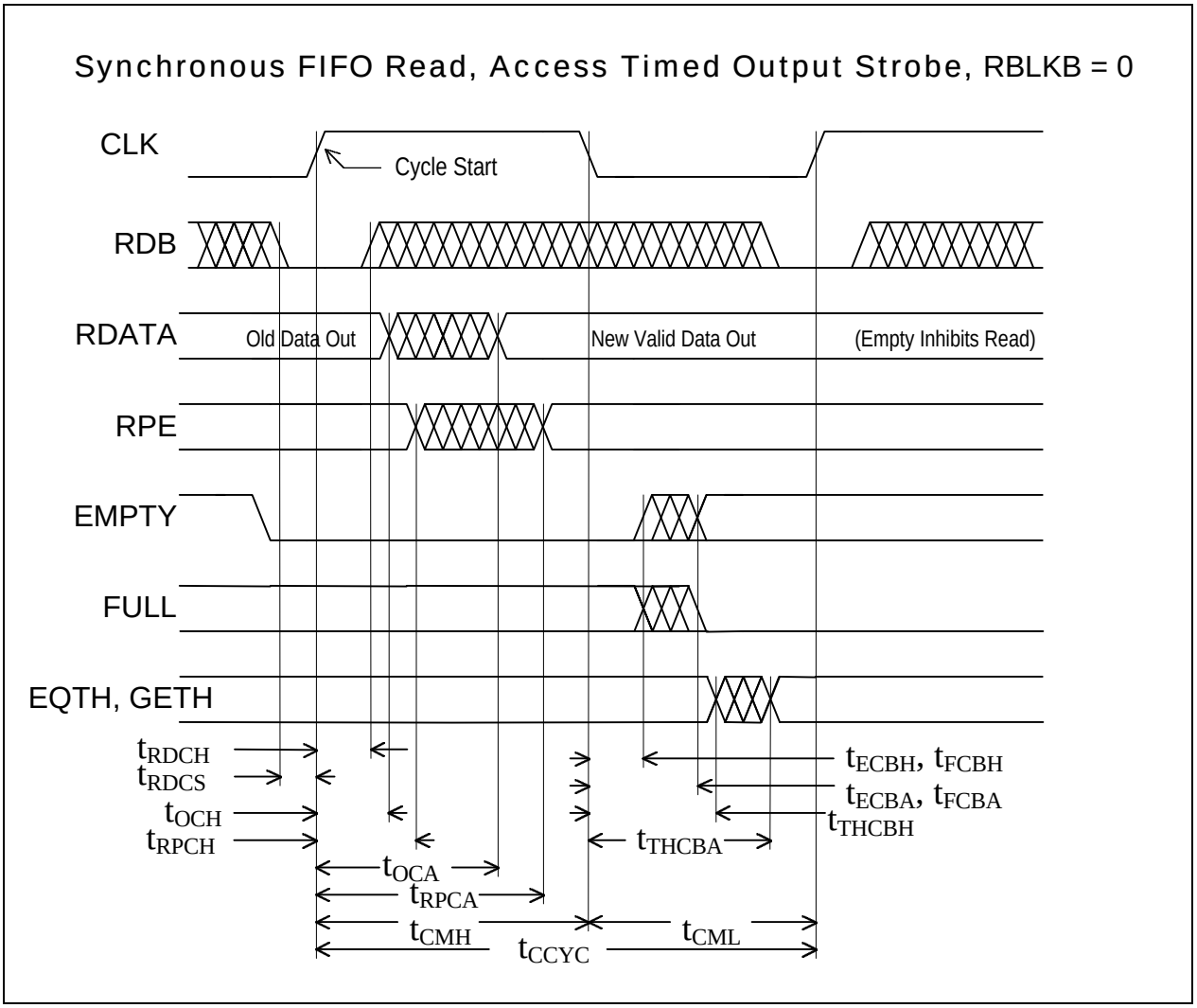
NOTE: ** At fast cycles, RDWRS (for enabling read) =MAX((15.0ns-WRL), 6.0ns)



T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

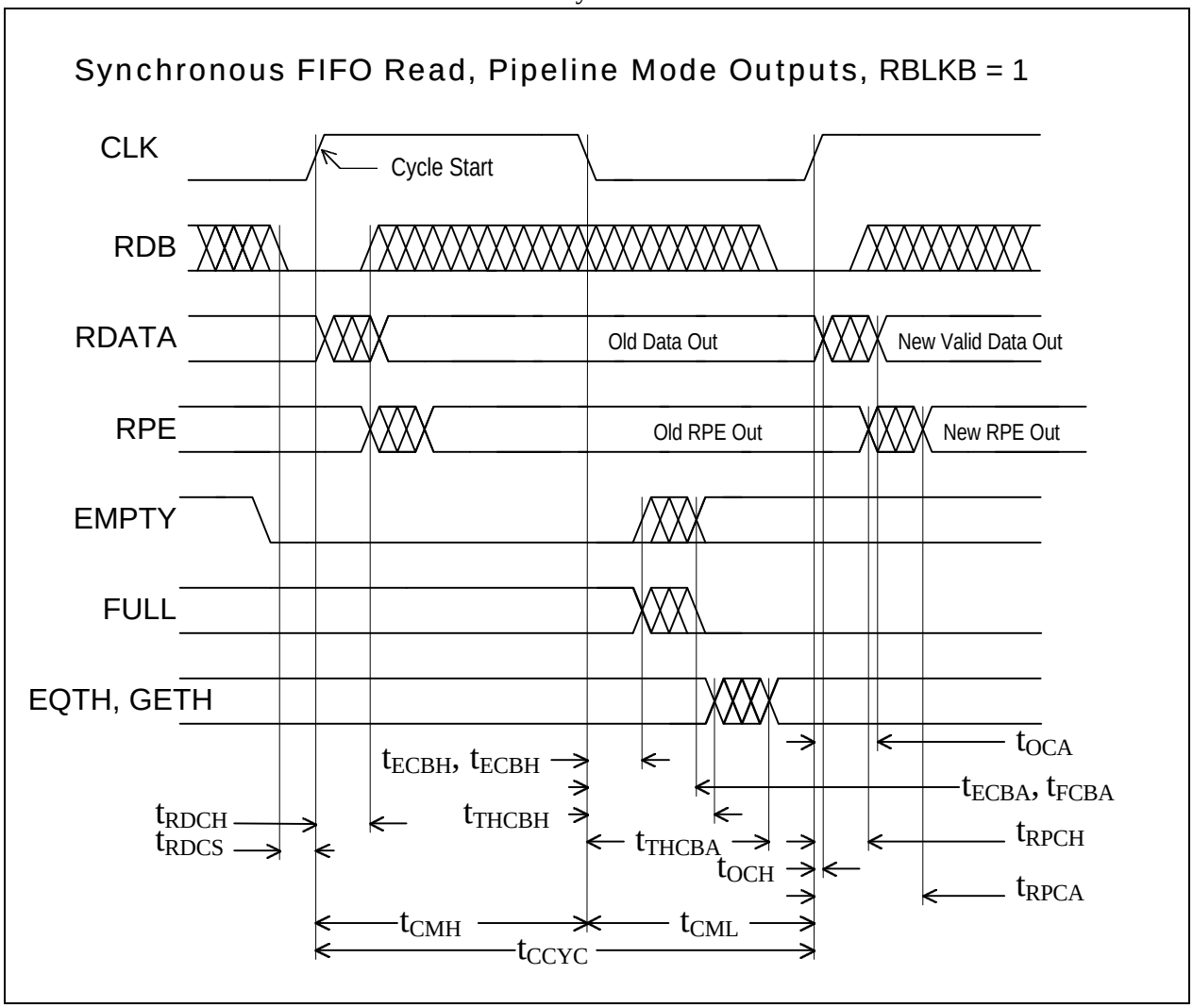
Symbol t_{xxx}	Description	Min	Max	Unit	Comment
DWRH	WDATA hold from WB ↑	3.0		ns	
DWRS	WDATA setup to WB ↑	1.0		ns	PARGEN is inactive.
DWRS	WDATA setup to WB ↑	5.0		ns	PARGEN is active.
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
EWRA	EMPTY ↓ access from WB ↑	6.0*		ns	* At fast cycles, EWRA, FWRA =MAX((15.0ns-WRL), 6.0ns)
FWRA	New FULL access from WB ↑	6.0*		ns	
THWRA	EQTH or GETH access from WB ↑	9.0		ns	
WPDA	WPE access from WDATA	6.0**		ns	WPE is invalid while PARGEN is active.
WPDH	WPE hold from WDATA		2.0	ns	
WRCYC	Cycle time	15.0		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	6.0		ns	Enabling the write operation.
			2.0		Inhibiting the write operation.
WRH	WB high phase	6.0		ns	Inactive
WRL	WB low phase	6.0		ns	Active

Note: **At fast cycles, WWRDS (for enabling write) = MAX ((15.0ns-RDL), 6.0ns



T_J= 0 C to 110 C; VDD = 4.75V to 5.25V

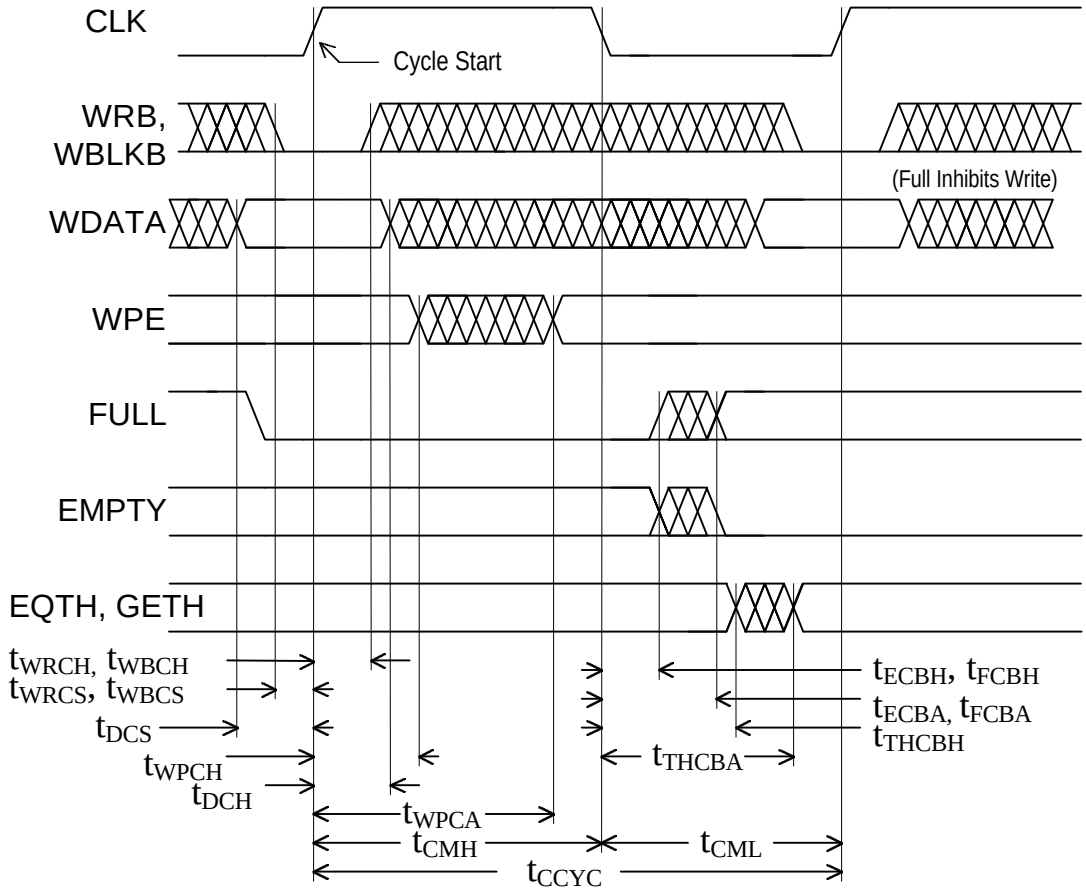
Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
ECBA	New EMPTY access from CLK ↓	6.0*		ns	* At fast cycles, ECBA & FCBA
FCBA	FULL ↓ access from CLK ↓	6.0*		ns	= MAX((15.0ns-CMH), 6.0ns)
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		2.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
OCA	New RDATA access from CLK ↑	15.0		ns	
OCH	Old RDATA valid from CLK ↑		6.0	ns	
RDCH	RDB hold from CLK ↑	1.0		ns	
RDCS	RDB setup to CLK ↑	2.0		ns	
RPCA	New RPE access from CLK ↑	19.0		ns	
RPCH	Old RPE valid from CLK ↑		6.0	ns	
THCBA	EQTH or GETH access from CLK ↓	9.0		ns	



T_J= 0 C to 110 C; VDD = 4.75V to 5.25V

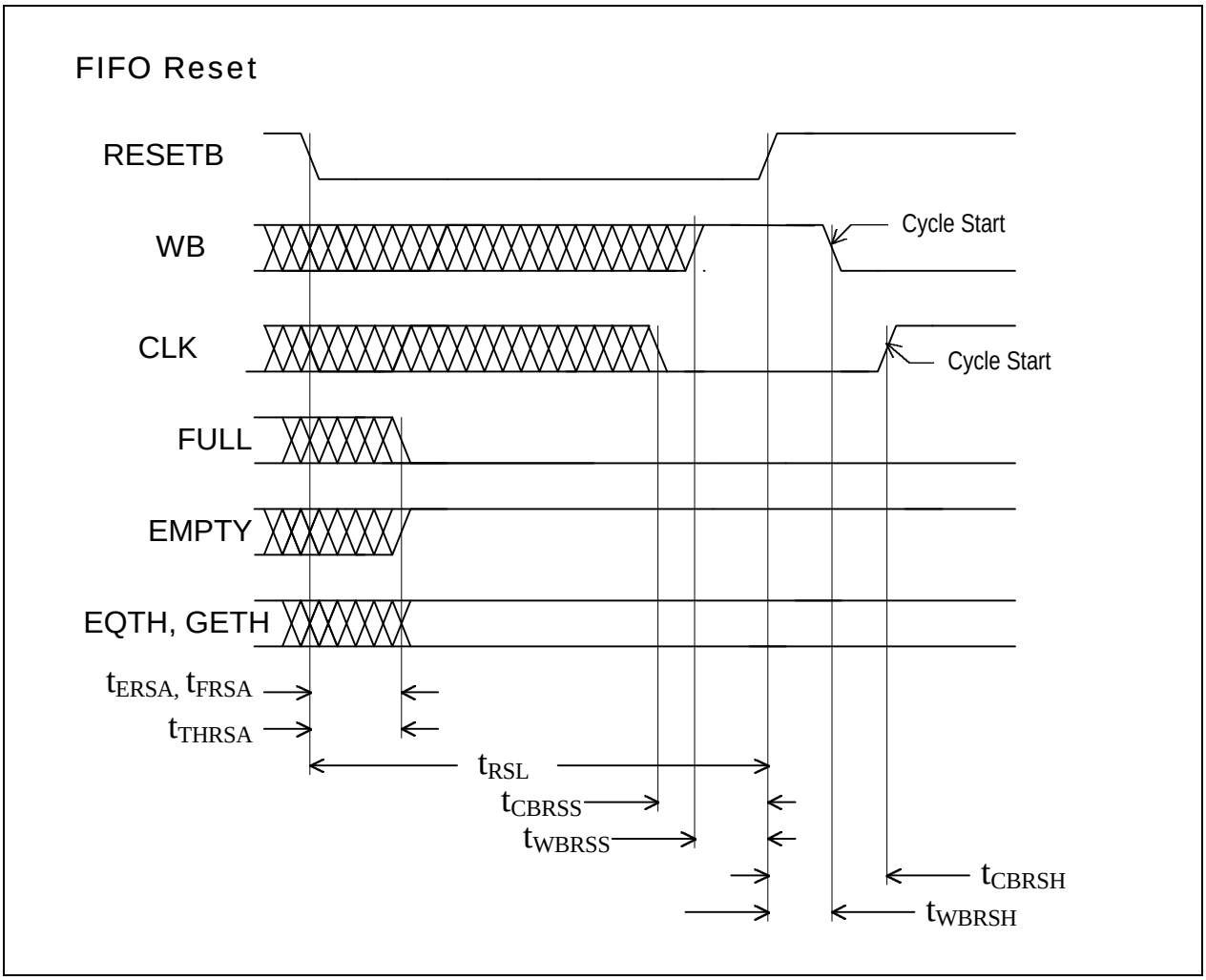
Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
ECBA	New EMPTY access from CLK ↓	6.0*		ns	* At fast cycles, ECBA & FCBA = MAX((15.0ns-CMH), 6.0ns)
FCBA	FULL ↓ access from CLK ↓	6.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		2.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
OCA	New RDATA access from CLK ↑	4.0		ns	
OCH	Old RDATA valid from CLK ↑		1.5	ns	
RDCH	RDB hold from CLK ↑	1.0		ns	
RDCS	RDB setup to CLK ↑	2.0		ns	
RPCA	New RPE access from CLK ↑	8.0		ns	
RPCH	Old RPE valid from CLK ↑		2.0	ns	
THCBA	EQTH or GETH access from CLK ↓	9.0		ns	

Synchronous FIFO Write



T_J= 0 C to 110 C ; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CCYC	Cycle time	15.0		ns	
CMH	Clock high phase	6.0		ns	
CML	Clock low phase	6.0		ns	
DCH	WDATA hold from CLK ↑	1.0		ns	
DCS	WDATA setup to CLK ↑	2.0		ns	
FCBA	New FULL access from CLK ↓	6.0*		ns	* At fast cycles, ECBA & FCBA = MAX((15.0ns-CMH), 6.0ns)
ECBA	EMPTY↓ access from CLK ↓	6.0*		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from CLK ↓		2.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete.
THCBA	EQTH or GETH access from CLK ↓	9.0		ns	
WPCA	New WPE access from CLK ↑	6.0		ns	WPE is invalid while PARGEN is active.
WPCH	Old WPE valid from CLK ↑		1.0	ns	
WRCH, WBCH	WRB & WBLKB hold from CLK ↑	1.0		ns	
WRCS, WBCS	WRB & WBLKB setup to CLK ↑	2.0		ns	



T_J= 0°C to 110°C; VDD = 4.75V to 5.25V

Symbol t_{xxx}	Description	Min	Max	Unit	Comment
CBRSH	CLK inactive hold from RESETB ↑	3.0		ns	Synchronous mode only.
CBRSS	CLK inactive setup to RESETB ↑	3.0		ns	Synchronous mode only.
ERSA	New EMPTY ↑ access from RESETB ↓	6.0		ns	
FRSA	FULL ↓ access from RESETB ↓	6.0		ns	
RSL	RESETB low phase	15.0		ns	
THRSA	EQTH or GETH access from RESETB ↓	9.0		ns	
WBRSH	WB inactive hold from RESETB ↑	3.0		ns	Asynchronous mode only.
WBRSS	WB inactive setup to RESETB ↑	3.0		ns	Asynchronous mode only.

Packaging Data

This section provides packaging information for the ProASIC GF260F products. Table 1 shows the maximum signal pins available by package type.

Table 1. Maximum Signal Pins Available

	MQUAD		eSBGA		CPGA	
Device	**Pins**	**I/Os**	**Pins**	**I/Os**	**Pins**	**I/Os**
GF260F100	208	144	352	248	391	247
GF260F180	N/A	N/A	560	360	391	319
GF260F310	N/A	N/A	560	408	N/A	N/A

For mechanical drawings of each package, please refer to the GF250F ProASIC product family data sheet.

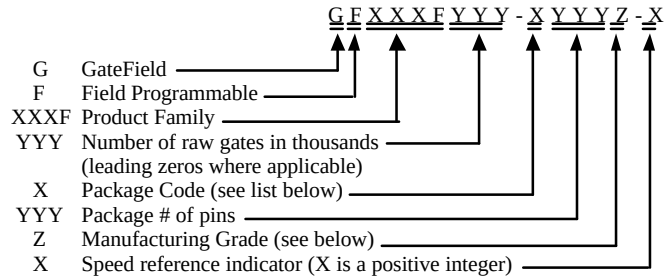
Pinout Information

The GF260F Embedded ProASIC product family has been designed to be pin-compatible with its "logic gate only" relative GF250F. However, the row of embedded memory blocks, which is located across the top of the GF260F device, affects the eight I/O pads on each of the "east" and "west" sides of a device. Each set of eight pads is gauged together as far as configuration goes. Input threshold and pull-up, and output drive strength and slew rate are configured in common for all eight pads. Each pad still has independent data in, data out, and output enable signals.

Please refer to the GF250F ProASIC Products Databook for detailed pinout information.

Ordering Information (Part Number Description)

PRODUCT CODING



Package Code List:

M	MQUAD	Metal Quad Flatpack
B	eSBGA	enhanced Super Ball Grid Array
C	CPGA	Ceramic Pin Grid Array

Manufacturing Grade:
C Commercial

Example:
GF260F180-C391C-4

GateField Sales Offices

	Location	Phone
Domestic		
GateField Corp.	California	510-249-5757
GateField Corp.	Massachusetts	617-848-8884
GateField Corp.	New Jersey	973-770-4700
GateField Corp.	Texas	972-562-3465
International		
GateField GmbH	Germany	089-962-4260
GateField Japan K.K.	Japan	045-471-1500

Manufacturing Reps

	Location	Phone
Domestic		
ESE	Alabama	205-830-1812
Aspen Technologies	California/Sacramento	916-985-3000
Bager Electronics	California/San Diego	619-632-8816
DynaRep	California/Los Angeles	805-777-1185
DynaRep	California/Orange County	714-573-1223
Marcom Sales	California/Silicon Valley	408-263-3660
Wescom Marketing	Colorado	303-422-8957
Dyne-a-Mark Corp.	Florida/Maitland	407-660-1661
Dyne-a-Mark Corp.	Florida/Ft. Lauderdale	954-485-3500
ESE	Georgia	770-242-7440
Wescom Marketing	Idaho	208-377-5585
Carlson Electr. Sales	Illinois	847-956-8240
Five Star Electronics	Indiana/Indianapolis	317-879-0940
Carlson Electr. Sales	Indiana/Carmel	317-575-4888
Carlson Electr. Sales	Iowa	319-377-6341
Nexus Tech. Sales	Maryland	301-663-4159
Compass Technology	Massachusetts	617-272-9990
Electromec Sales	Minnesota	612-894-8200
Metro Logic Corp.	New York/New Jersey	973-575-5585
Quality Components	New York/Manlius	315-682-8885
Quality Components	New York/Rochester	716-288-3420
Quantum Marketing	North Carolina/Raleigh	919-846-5728
Quantum Marketing	North Carolina/Charlotte	704-536-8558
Five Star Electronics	Ohio/Solon	216-349-1611
Five Star Electronics	Ohio/Dayton	937-299-1718
Five Star Electronics	Ohio/Hilliard	614-529-8031
Micro Sales Inc.	Oregon	503-645-2841
Quality Components	Pennsylvania/New Jersey	610-489-0155
Gardin Moore Sales	Texas/Austin	512-794-2900
Gardin Moore Sales	Texas/Plano	972-985-1193
Gardin Moore Sales	Texas/Stafford	281-240-6767
Wescom Marketing	Utah	801-269-0419
Micro Sales Inc.	Washington	425-451-0568
Carlson Elec. Sales	Wisconsin	414-476-2790
Canada		
Polar Components	Ontario/Kanata	613-592-8807
Polar Components	Ontario/Woodbridge	416-410-3377
Polar Components	Quebec	514-683-3141
International		
GEC Electronics	Australia	02-9638-1888
Hantro Products	Finland	358-8-551-4382
SICAN	Germany	0511-277-1464
Tritech Ltd.	Israel	09-902092
Esco Italiana S.p.A.	Italy	02-262-7011
Rohm Co. Ltd.	Japan	075-311-2121
Tomen Electronics	Japan	03-5462-9706
Sanghwa Micro Tech.	Korea	02-3-453-7117
PTC Systems PTE	Singapore	282-0255
Maojet Technology	Taiwan	06-2-25677643

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