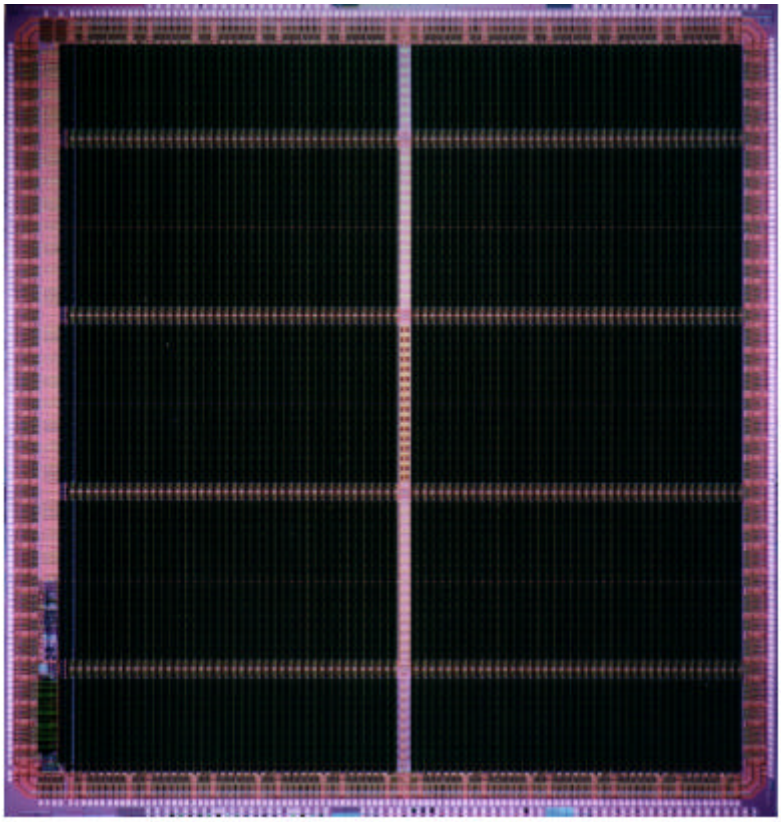
GATEFIELD
TM

GF250F ProASIC Product Family

Highest Performance, Highest Density, Programmable CMOS ASICs

The GF250F™ ProASIC™ product family is the highest performance and highest gate count programmable ASICs released in the GateField™ portfolio. The GF250F family offers reprogrammable ASIC solutions to applications in the consumer, computer and communications markets.

Figure 1. ProASIC 50,000 Gate Device



Features and Benefits

- 150,000 available gates provide increased system integration
- 15-20% speed increase over the GF200F product improves system performance
- Distributed memory compilation for register files and FIFOs ensures optimally placed memory
- Non-volatile flash technology retains programming during power cycles
- The fine-grained architecture provides synthesis source compatibility with gate arrays
- Package options, including CPGA, MQUAD, and eSBGA, meet a wide range of system requirements
- Full compatibility with industry standard design methodology and tools improves design productivity
- Sign-off on industry-leading third party verification tools simplifies design process
- PCI compliant target and master cores enable easy interfacing to industry standard PCI buses
- Compilable JTAG support facilitates boundary-scan insertion
- Programmable security bit helps prevent customer-owned intellectual property (IP) reverse engineering

Table 1. GF250F ProASIC Product Family

Part Type	Total Gates	Usable Gates	Compilable Ram Bits	flip-flops	Maximum # of I/O Pins
GF250F025	25,000	12,000	1.2K 1r/1w	3,000	176
GF250F050	50,000	22,000	2.5K 1r/1w	6,000	248
GF250F100	100,000	46,000	5.1K 1r/1w	12,000	360
GF250F150	150,000	70,000	7.5K 1r/1w	18,000	424

Contact your sales representative for product availability.

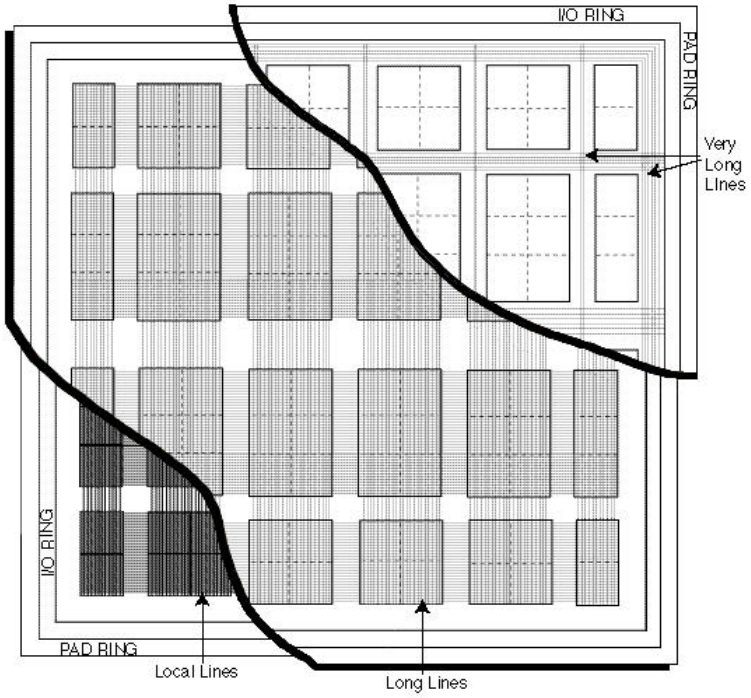
Process Technology

The GF250F ProASIC family achieves its non-volatility and re-programmability through its underlying process technology; an advanced flash-based, 0.5µm channel length CMOS technology. Standard CMOS design techniques are used to implement logic and control functions resulting in highly predictable performance and gate array compatibility. Flash memory bits are distributed throughout each device providing non-volatile, yet reconfigurable interconnect programming. GateField manufactures the GF250F in conjunction with its wafer fabrication partner, Rohm Semiconductor, in Kyoto, Japan. The GF250F process employs I-line lithography to produce state-of-the-art products optimized for performance, density and high-reliability.

The ProASIC GF250F Product Architecture

The GF250F ProASIC product utilizes a proprietary architecture that results in granularity comparable to gate arrays. Unlike SRAM-based FPGAs, the GF250F products do not utilize look-up tables nor architectural mapping during design. Synthesizing directly to gates streamlines the design flow, increases design productivity and eliminates dependencies upon vendor specific design tools. The GF250F device core consists of a sea of programmable tiles. Each tile is configured as a specific logic function (i.e. inverter, NAND gate, NOR gate, etc.) by programming interconnect switches. This is directly analogous to the metal mask and via programming of one or more "gates" in a gate array core. Gates and larger functions are connected together in the same manner utilizing the three levels of routing hierarchy shown in figure 2. Switches are programmed to connect signal lines to the appropriate macrocell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew clock distribution throughout the core. All core tiles are configurable as gates, flip-flops or distributed memory. Maximum core efficiency is possible for virtually any design.

Figure 2. The GF250F Device Core Architecture



Macrocell Library

The GF250F products' macrocell library provides functional granularity equivalent to gate arrays. The library includes simple gates, complex gates and storage elements such as flip-flops and latches. A sampling of the breadth of functionality is provided in table 2. Every effort has been made to create a "synthesis friendly" library. Many versions of every cell type exist which allows Synopsys' Design Compiler tool maximum flexibility in selecting the best cell for each situation during synthesis. This results in optimum performance and maximum silicon efficiency. In addition, two speed grades are available: (-4) standard grade and (-3) high-performance grade.

Table 2. Sample Macrocell Library Listing

Cell Name	Description	Delay (ns)[1]	
		-4	-3
INV	Inverter	2.15	1.66
NAND2	2-Input NAND	1.88	1.45
AND2	2-Input AND	1.02	0.79
NOR3	3-Input NOR	1.57	1.22
MUX2L	2-1 Multiplexor with Active Low Select	1.47	1.14
OA21	2-Input OR into a 2-Input AND	1.54	1.19
XOR2	2-Input Exclusive OR	1.71	1.32
LDL	Active Low Latch (HL/LH)	1.89/2.22	1.41/1.66
DFFL	Negative Edge-Triggered D-type Flip-flop (HL/LH)	1.89/2.22	1.41/1.66

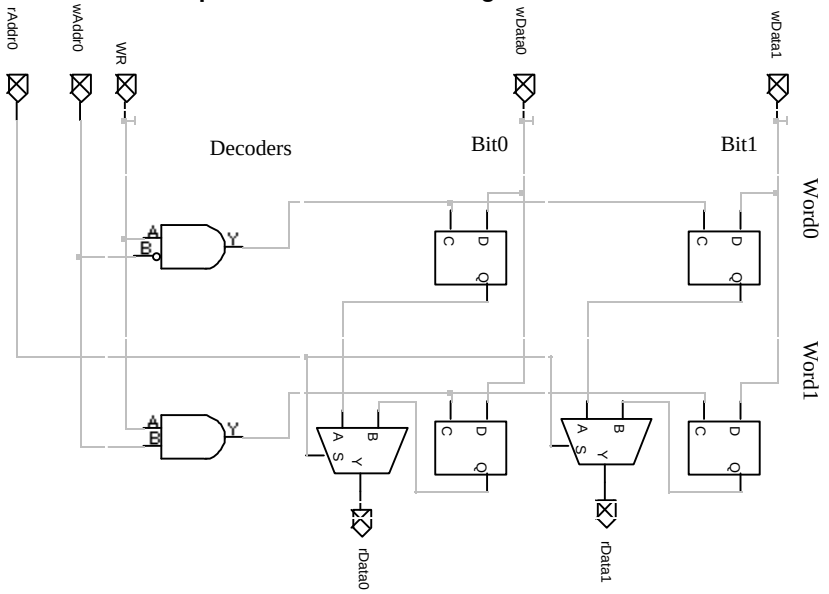
1. Assumes two standard loads.

Distributed Memory Compiler

The GF250F ProASIC family allows small register files and FIFOs to be compiled utilizing the functionality of core tiles. This enables memory to be placed whenever and wherever it is needed in relation to the surrounding logic. As a part of the ASICmaster™ software suite, the MEMORYmaster™ software accepts inputs from the designer as to number of words and bits, preferred origin and orientation, and the targeted device. MEMORYmaster produces a netlist complete with estimated timing for design simulation purposes and a hard-macro for layout ensuring dense, fast memories. After layout, actual delay data is back-annotated into the hard-macro design file for final simulation.

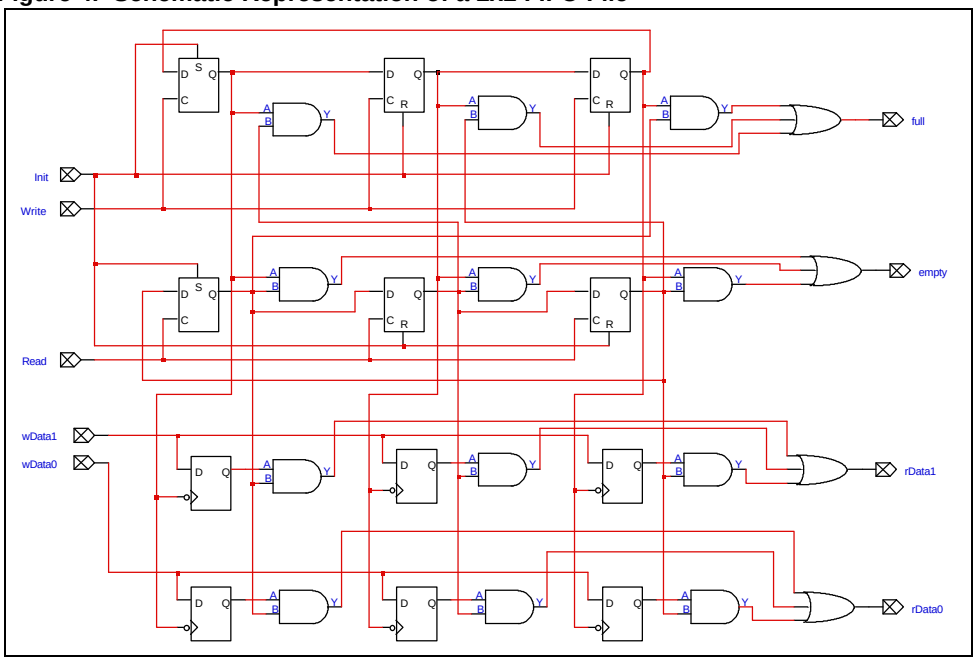
Register Files - Compiled register files have independent read and write ports. The read port is asynchronous ensuring the data is available as soon as possible after a read address change. The write operation may be compiled as level-sensitive or edge-sensitive. Figure 3 is a schematic representation of a 2x2 register file.

Figure 3. Schematic Representation of a 2x2 Register File



FIFO - Compiled FIFOs have independent read and write ports as well but no address inputs. The FIFO automatically keeps track of the address. Figure 4 shows the schematic of a 2x2 FIFO file.

Figure 4. Schematic Representation of a 2x2 FIFO File



Additional information on GateField's memory compiler technology may be found in the MEMORYmaster application note.

Clock Distribution

High performance, low skew clock distribution networks are extremely important in addressing today's high performance designs. The GF250F family is designed to provide optimum programmable clock performance. Each device contains four primary clock inputs. Each clock input has programmable access to every tile throughout the chip. These four inputs can be individually programmed as separate clocks operating within particular regions of the core or programmed for operation throughout the entire core. The skew between any two flip-flops on a clock net is less than 1ns.

The programming options of the four primary clock paths are extensive. The delay path from the clock input pad to any flip-flop in the chip is virtually identical. As shown in figure 5, each clock distribution path branches into 10 equal regions. Then, using the GF250F100 family member as an example, each region further branches into over 40 localized clock nets. Any branch not programmed for the primary clock may be used for other clock signals or any other signal that requires low skew.

Through programming, the designer may implement up to four global low skew clock nets, up to 40 regional clock nets, over 400 local clock nets, or various combinations of global, regional and local clock nets. Table 3 provides performance specifications for different clocking implementations.

Figure 5. GF250F100 Clock Distribution

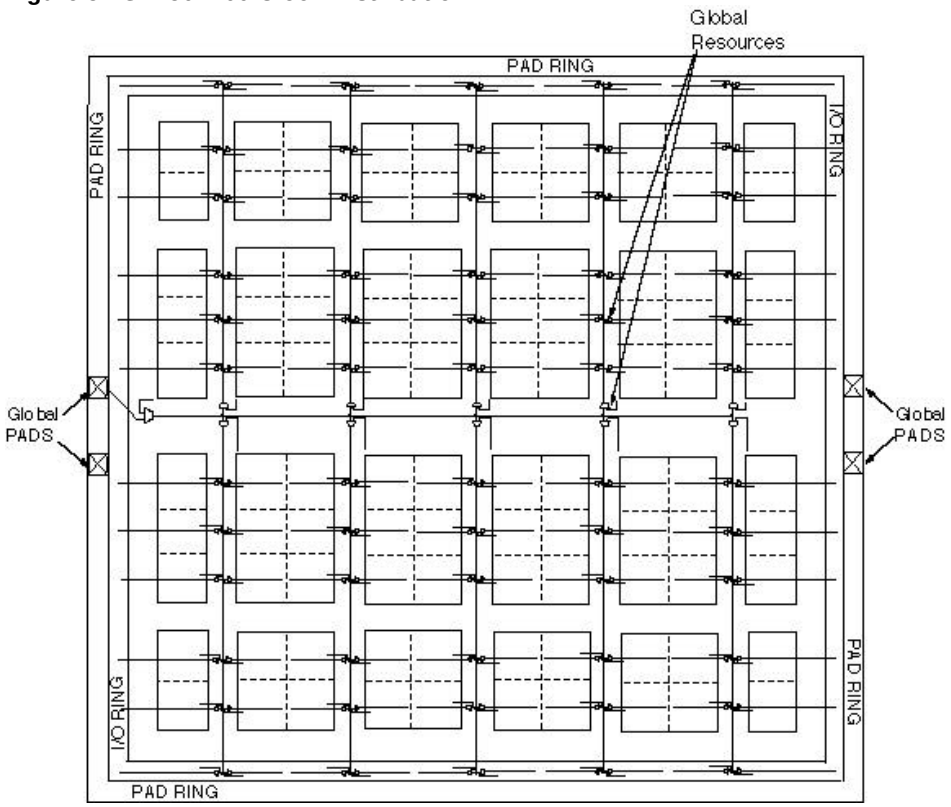


Table 3. Sample Clock Distribution Specification

Device	Worst Case Skew(ns)	Typ. Operating Frequency[1] (MHz)	Max. Clk Loads	Nom Prop Delay (ns)
GF250F025	1	67	3,000	2.6
GF250F050	1	67	6,000	2.9
GF250F100	1	67	12,000	3.5
GF250F150	1	67	18,000	4.0

[1] Actual frequency is dependent upon design (i.e. levels of logic)

Programmable I/Os

The GF250F family I/Os may be programmed as input, output and bi-directional. I/Os programmed as input buffers offer the following flexibility:

- TTL voltage levels
- CMOS voltage levels
- Pull-up resistor

I/Os programmed as output buffers offer the following flexibility:

- Selectable drive strengths
- Selectable slew rates
- Three-state
- Internal driver

I/Os programmed as bi-directional buffers offer the following flexibility:

- TTL voltage levels
- CMOS voltage levels
- Pull-up resistor
- Selectable drive strengths
- Selectable slew rates
- Three-state

All I/Os include ESD protection and are designed to prevent latchup.

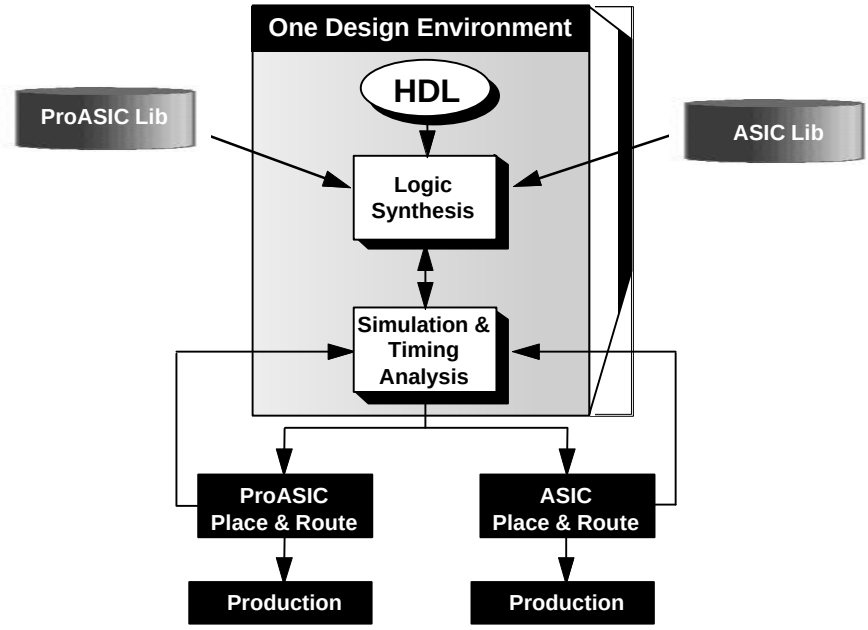
PCI I/Os

The Peripheral Component Interconnect (PCI) programmable I/O simplifies interfacing to industry-standard, revision 2.1, 33 MHz PCI buses. Any I/O may be programmed for PCI interfacing. In addition, hard-cores are available for simulation and layout to ensure that PCI timing requirements are met. Synthesizable core descriptions allow design portability and migration to standard ASICs. For more information on PCI I/O support, refer to the GateField PCI application note.

ASIC Design Environment

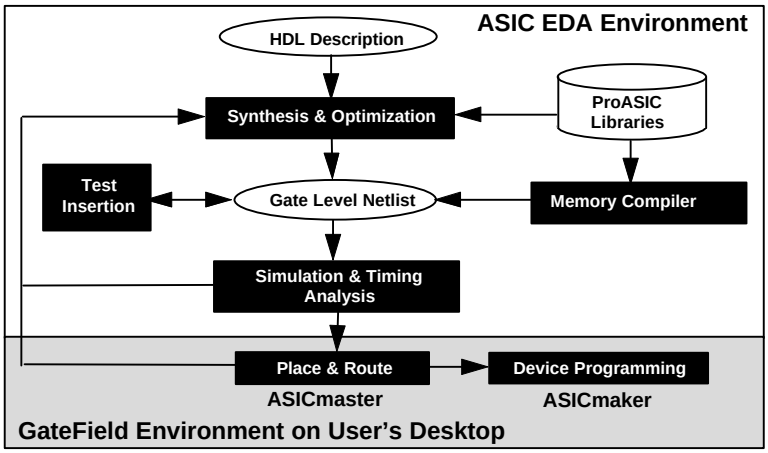
The GF250F ProASIC product design environment provides significant advantages to the design engineer and program manager. It utilizes the same robust VHDL and Verilog HDL descriptions that are targeted for gate arrays and standard cells. This frees the designer from the limitations and special idiosyncrasies imposed upon HDL by FPGA vendors. Furthermore, GateField does not require special FPGA tools for synthesis and the so-called "architectural mapping." Standard ASIC tools such as Design Compiler, VSS, Verilog XL, QuickSim II, VCS, Motive, Leonardo, etc. are supported. This streamlines the design environment and enables the design team to focus on a single suite of design tools, whether the design is targeted for gate arrays or programmable ASICs. The ProASIC design flow also ensures a seamless transition to your ASIC vendor of choice should production volumes warrant a migration to a gate array or a standard cell product. As shown in figure 6, with identical HDL, identical design tools and flow, migration to ASICs for high volume production is greatly simplified. Conversely, migration from ASICs to GateField's ProASIC technology is also unburdened by traditional FPGA design requirements. Supported EDA environments include Mentor Graphics (Falcon Framework 8.5), Synopsys (Design Compiler 3.5a and later), Quad Design Technologies (Motive 5.0 and later), Viewlogic Systems (Powerview 5.1) and Exemplar (Leonardo 4.0.3).

Figure 6. Common Design Environment Simplifies Migrations



Once the design has been synthesized, simulated and timing analysis performed, it is ready for place and route. To facilitate this activity, GateField has created a desktop software package, ASICmaster™, which is ideally suited for the busy engineer. As an integral part of the ProASIC design flow (figure 7), ASICmaster runs on Sun and HP workstations. It accepts standard ASIC formatted netlists, performs place and route of the design into the selected device and provides back annotated delay information for simulation. This is all accomplished through the software's easy to use interface. Within minutes, the average design engineer will be up and running.

Figure 7. The ProASIC Design Flow



The ASICmaster software also contains very powerful interactive layout capabilities for the experienced user. Preferred placement, routing changes and custom clock tree configurations are all possible. Once the design is finalized, the layout is down-loaded into GateField's ASICmaker™ device programmer, shown in figure 8, for ProASIC part programming. The ASICmaker device programmer supports interchangeable modules for each package type available and an In-System-Programming module to facilitate reprogramming ProASIC devices already resident in a board or system. The ASICmaster and ASICmaker tools ensure fast and efficient programmable ASIC implementations for the novice or expert user.

Figure 8. GateFieldís ASICmaker Device Programmer

Package Thermal Characteristics

The GF250F ProASIC family is available in a number of package types. Packages are selected based on high pin count, reliability factors and superior thermal characteristics.

The ability of a package to conduct heat away from the silicon, through the package to the surrounding air is expressed in terms of thermal resistance. This junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta JA (Θ_{JA}). The lower the thermal resistance, the easier it is for the package to dissipate heat.

The maximum allowed power (P) for a package is a function of the maximum junction temperature (T_J), the maximum ambient operating temperature (T_A), and the junction-to-ambient thermal resistance (Θ_{JA}). Maximum junction temperature is the maximum temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{JA}}$$

Θ_{JA} is a function of the rate of air flow in contact with the package, in linear feet per minute

(lfpm). When the estimated power consumption exceeds the maximum allowed power, other means of cooling must be used, such as increasing the air flow rate.

The junction-to-case thermal resistance is Theta JC (Θ_{JC}) and is the lowest possible thermal resistance of the device. Θ_{JC} is defined as:

$$\Theta_{JC} = \frac{T_J - T_C}{P}$$

where

T_C = temperature measured at the top dead center of the package
P = is power

The following tables list Θ_{JC} and Θ_{JA} for the packages used by the GF250F products under several different operating conditions.

Table 4. Thermal Characteristics of CPGA Package

Package	Θ_{JC}	Θ_{JA} Still Air	Θ_{JA} 200 lfpm Air Flow	Θ_{JA} 400 lfpm Air Flow
CPGA391	1.7	20.2	12.7	9.8

Table 5. Thermal Characteristics of MQUAD Package

Package	Θ_{JC}	Θ_{JA} Still Air	Θ_{JA} 200 lfpm Air Flow	Θ_{JA} 400 lfpm Air Flow
MQUAD208	0.5	13	10.6	9.7

Table 6. Thermal Characteristics of eSBGA Package

Package	Θ_{JC}	Θ_{JA} Still Air	Θ_{JA} 200 lfpm Air Flow	Θ_{JA} 400 lfpm Air Flow
eSBGA352	0.34-0.72	9.9-11.3	9.6*	8.7*
eSBGA560	0.20-0.30	8.5-9.1	7.3*	6.5*

(*) Forced convection at 3.0 watts.

Calculating Power Dissipation

GF250F device power is calculated in the same manner as CMOS gate arrays and includes both a static and an active component. The active component is a function of both the number of tiles utilized and the speed. To calculate the power dissipation, use the formula:

$$P = V_{DD} \cdot I_{DD}$$

where

$$I_{DD} = I_{STATIC} + I_{OUTPUT} + I_{LOGIC}$$

and

I_{STATIC} is the static current.
I_{OUTPUT} is the current due to the outputs switching.
I_{LOGIC} is the current due to the internal logic signals switching.

The static power (I_{STATIC}) is the amount of current drawn when no inputs are switching. This is equal to the Quiescent Supply Current I_{DDQ} specified under DC Characteristics.

Active power includes both the current due to outputs switching and the current due to internal logic signals switching.

$$I_{OUTPUT} = \sum_{i=1}^{n} (C_i \cdot V_i \cdot f_i + I_{DCi})$$

where

C_i is the capacitance on the *i* th output pad.
V_i is the voltage swing on the *i* th output pad.

f_i is the switching frequency on the *i* th output pad.
n is the number of outputs.
I_{DCi} is the average DC load on each pad, if any.

In most cases I_{OUTPUT} can be approximated by this formula, measured in mA:

$$I_{OUTPUT} = n \cdot C_{typ} \cdot V \cdot f_{avg}$$

where

n is the number of active outputs.
C_{typ} is the typical capacitance load on an output.
V is the average voltage swing.
f_{avg} is the average switching frequency of the outputs. Typically this is less than 25% of the clock frequency.

I_{LOGIC} is represented by this formula, measured in mA:

$$I_{LOGIC} = 0.35 \cdot I_E \cdot G \cdot f \cdot F$$

where

I_E is the effective µA per gate per MHz of the GateField parts. For the GF250F products the value is 10.
G is the number of gates used in the design, in thousands.
f is the operating frequency in MHz.
F is the fraction of devices active on each clock edge. F varies for different designs, but 0.15 is a conservative and commonly used value.

For a GF250F050 design that has 22,000 used gates, 50 active outputs, an average load of 20 pF, and a 30 MHz clock, creating an average switching frequency of 6 MHz, the power calculation appears below.

I_{STATIC} = 1.0 mA
I_{OUTPUT} = $50 \cdot 20 \cdot 10^{-12} \cdot 5 \cdot 6 \cdot 10^6$ mA
= 30 mA
I_{LOGIC} = $0.35 \cdot 10 \cdot 22 \cdot 30 \cdot 0.15$ mA
= 346 mA
Therefore
I_{DD} = (1 + 30 + 346) mA
= 377 mA
P = 5V · 377 mA
= 1.9 W

Delay Derating

The timing characteristics for GF250F ProASIC devices are similar to those of traditional gate arrays. Delays are a function of the macrocells used in the design and the output loading/fanout of each cell. While actual delays are a function of the final placement and routing, typical values for delays can be used to make good approximations of the delays prior to implementation. Each macrocell description includes typical values for intrinsic and load dependent delays.

Device performance varies as a factor of the process, temperature and voltage. The tables and figures below show how the nominal timing values given in the macrocell library change as a function of these three variables.

Table 7. Process Derating Factor

Worst Case	Typical	Best Case
1.2	1.0	0.7

Table 8. Combined Temperature and Voltage Derating Factor

Commercial*		Industrial*	
Best Case	**Worst Case**	**Best Case**	**Worst Case**
0.85	1.42	0.66	1.49

*Remarks:

Commercial	5V ± 5%	T_j = 0 ~ 110°C
Industrial	5V ± 10	T_j = -40 ~ 110°C

Calculating Critical Path Delays

Figure 9 shows the temperature derating factor KT for a given junction temperature. Figure 10 shows the voltage derating factor for a given supply voltage.

Figure 9. Temperature Derating

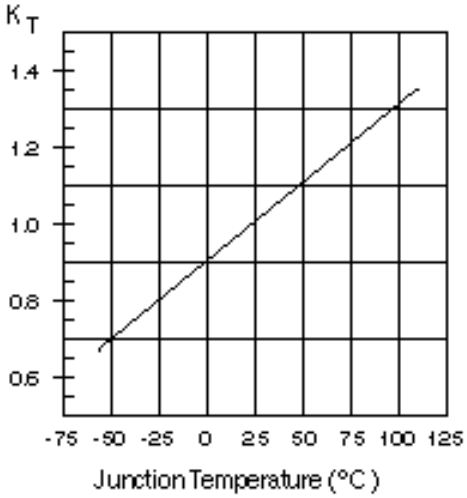
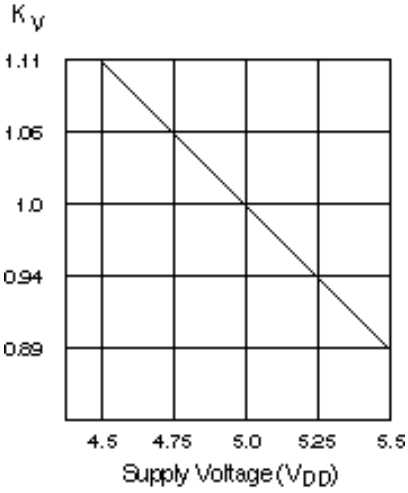


Figure 10. Voltage Derating



To estimate the delay for a particular cell, the following equation is used:

Delay = Intrinsic + (Drive · Load) + Wire Delay

Note: To obtain the most accurate timing data, use the figures generated by the ASICmaster after completing place and route.

where

$$\text{Load} = \sum_{i=1}^{\text{fanout}} \text{Input loading}$$

To estimate wire delay for a particular net, the following equation is used:

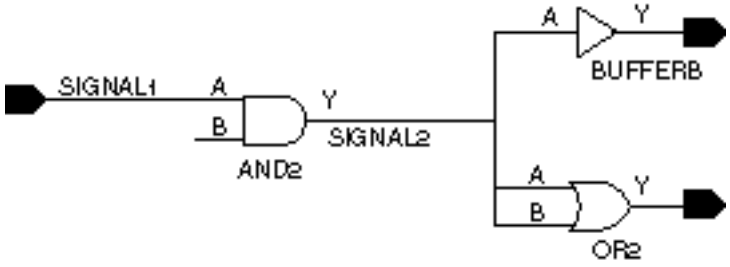
Delay = $0.56 + 0.29 \cdot f_o$ for $f_o < 15$

= $1.47 + 0.22 \cdot f_o$ for $15 \bullet f_o \bullet 100$

where f_o is fan out.
These are 80% values, that is, 80% of nets will be faster than this prediction.

Here is an example estimated delay calculation. For the sample circuit below, the estimated delay from SIGNAL1 to SIGNAL2, when SIGNAL2 is rising, and for typical case wire loading, can be calculated using the following formula.

Figure 11. Example Circuit for Estimated Delay Calculation



A to Y tPLH = D1 + (D2 · (L1 + L2 + L3)) + L4

D1 = 0.83 = Intrinsic Delay A to Y (tPLH) for AND2.
D2 = 0.05 = Drive Delay A to Y (tPLH) for AND2.
L1 = 1.1 = Input Loading of pin A for BUFFERB.
L2 = 3.0 = Input Loading of pin A for OR2.
L3 = 2.6 = Input Loading of pin B for OR2.
L4 = 1.43 = Wire Delay from Wire Delay table for a fanout of 3, typical case, (L4 = 0.56 + 0.29 · 3).

$Delay_{AY}$ tPLH = 0.83 + [0.05 ˙ (1.1 + 3.0 + 2.6)] + 1.43 = 2.59 ns

Specifications

Electrical specifications for the GF250F devices are provided in this section. Table 9 lists the absolute maximum ratings for the technology. Table 10 lists the recommended operating conditions for the GF250F products.

Table 9. Absolute Maximum Rating (Referenced to V_{SS})

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	-0.3 to +7	V
Input Voltage	V_{IN}	-0.3 to VDD+0.3	V
DC Input Current	I_{IN}	±10	mA
Storage Temperature (Ceramic)	T_{STG}	-65 to +150	°C
Storage Temperature (Plastic)	T_{STG}	-40 to +125	°C

[1] PCI I/Os comply with the Peripheral Component Interface Specification version 2.1.

Table 10. Recommended Operating Conditions

Parameter	Symbol	Limits[1]	Unit
Operating Ambient Temperature	T_A	0 to +70	°C
Junction Temperature	T_J	-40 to 110	°C
DC Supply Voltage (over junction temperature range)	V_{DD}	-4.75 to 5.25	V

[1] Adherence to the limits in this table is required for normal device operation. Sustained operation of a device at conditions exceeding these values may result in permanent device damage or impaired device reliability.

Table 11 lists the DC characteristics for the GF250F products input and output buffers.

Table 11. DC Characteristics for 5V Buffers

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Voltage Input Low - TTL - CMOS				 0.8 $0.3*V_{DD}$	V
V_{IH}	Voltage Input High - TTL - CMOS		 2 $0.7*V_{DD}$			V
V_T	Switching Threshold	TTL CMOS		1.5 2.5		V
I_{IN}	Input Current - CMOS & TTL - with pull-up	 $V_{IN}=V_{DD}$ or V_{SS} $V_{IN}=V_{SS}$	 -10 -30	 ±0.1 -100	 10 -300	µA
V_{OH}	Voltage Output High - I/O Cell IOB6 - I/O Cell IOB12	I_{OH}=-1mA I_{OH}=-6mA I_{OH}=-12mA	V_{DD}-0.1 2.4 2.4			V
V_{OL}	Voltage Output Low - I/O Cell IOB6 - I/O Cell IOB12	I_{OL}=1mA I_{OL}=6mA I_{OL}=12mA		 0.2 0.2	0.1 0.4 0.4	V
I_{OZ}	Three-state Leakage Current	$V_O=V_{DD}$ or V_{SS}	-10	±0.1	10	µA
I_{OS}	Output Short Circuit Current	V_{DD}=Max, $V_O=V_{DD}$ V_{DD}=Max, $V_O=V_{SS}$		80 -80	200 -200	mA
I_{DDQ}	Quiescent Supply Current	$V_{IN}=V_{DD}$ or V_{SS}		1.0	10	mA
C_{IN}	Input Capacitance	Any Input Buffer		4.0		pF
C_{OUT}	Output Capacitance	Any Input Buffer		4.0		pF

Packaging Data

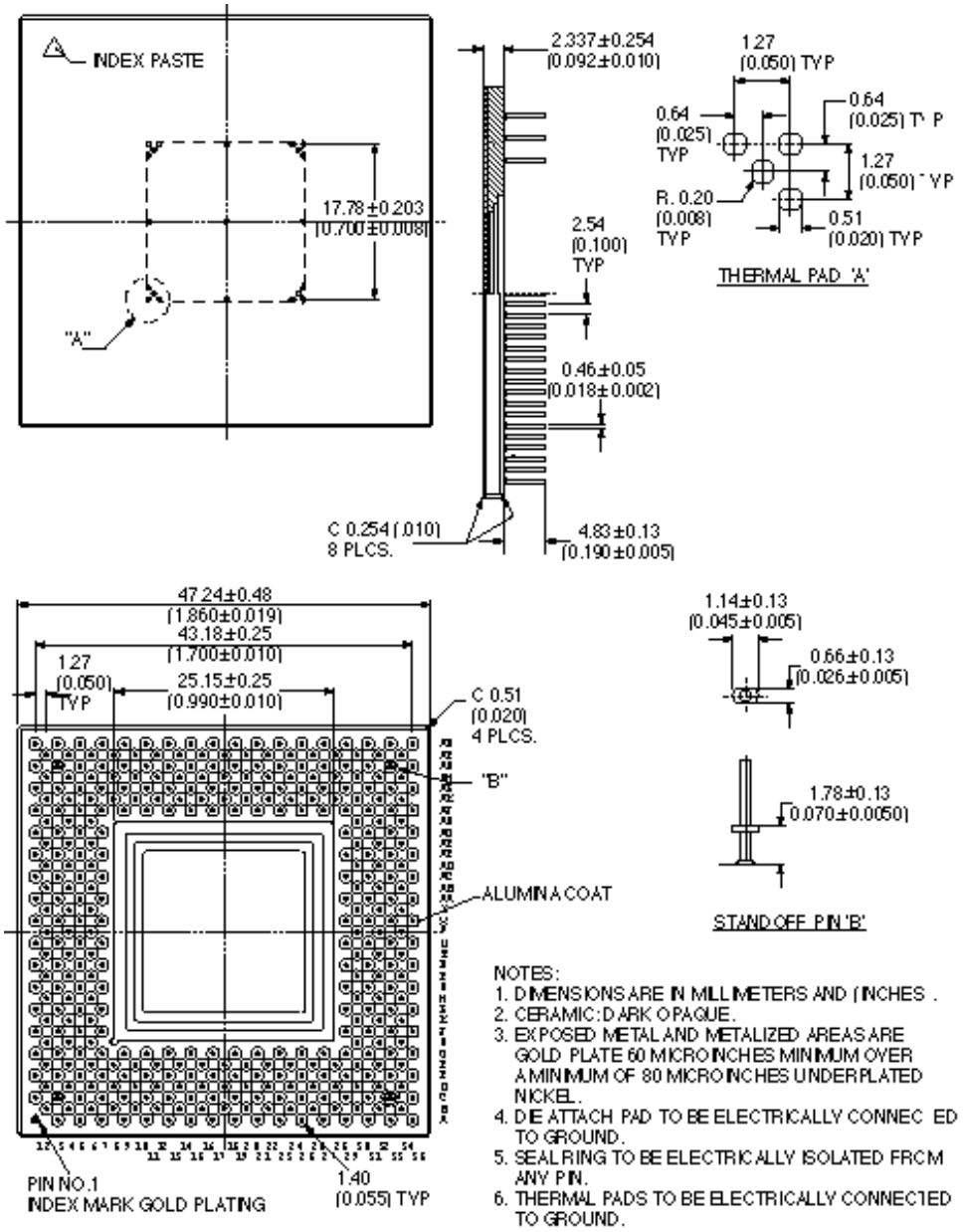
This section provides packaging information for the ProASIC GF250F products. Table 12 shows the maximum signal pins available by package tpye.

Table 12. Maximum Signal Pins Available

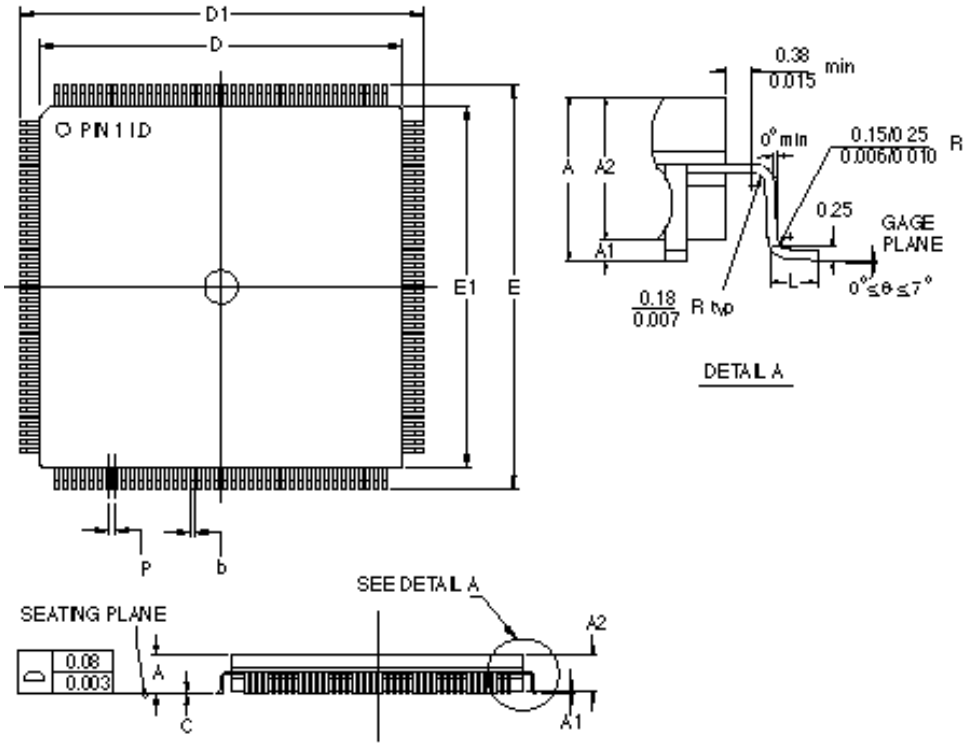
Device	MQUAD Pins	MQUAD I/Os	eSBGA Pins	eSBGA I/Os	CPGA Pins	CPGA I/Os
GF250F025	208	144	352	176	N/A	N/A
GF250F050	208	144	352	248	391	248
GF250F100	N/A	N/A	560	360	391	391
GF250F150	N/A	N/A	560	408	N/A	N/A

Following are the mechanical drawings of each package.

391-Pin CPGA Package Mechanical Drawings



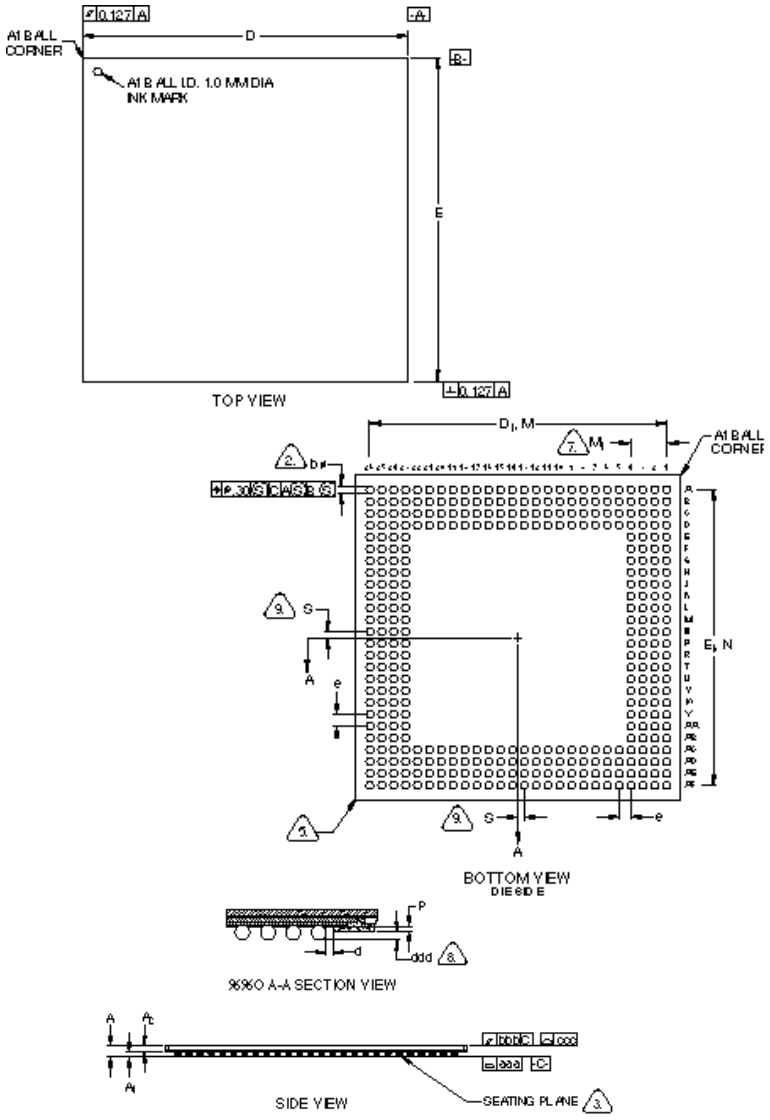
208-Pin MQUAD Package Mechanical Drawings



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.42	3.85	4.07	0.135	0.152	0.160
A1	0.25	0.45	0.64	0.010	0.018	0.025
A2	3.17	3.40	3.43	0.125	0.134	0.135
D	30.40	30.60	30.80	1.197	1.205	1.213
D1	27.59	27.64	27.79	1.086	1.088	1.094
E	30.40	30.60	30.80	1.197	1.205	1.213
E1	27.59	27.64	27.79	1.086	1.088	1.094
L	0.50	0.60	0.75	0.020	0.024	0.030
P	0.50 BSC			0.0197 BSC		
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.15	0.175	0.20	0.004	0.007	0.008

NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS

352-Pin eSBGA Package Mechanical Drawings



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. PIN A1 I.D. MARKED BY INK.
5. SHAPE AT CORNER.

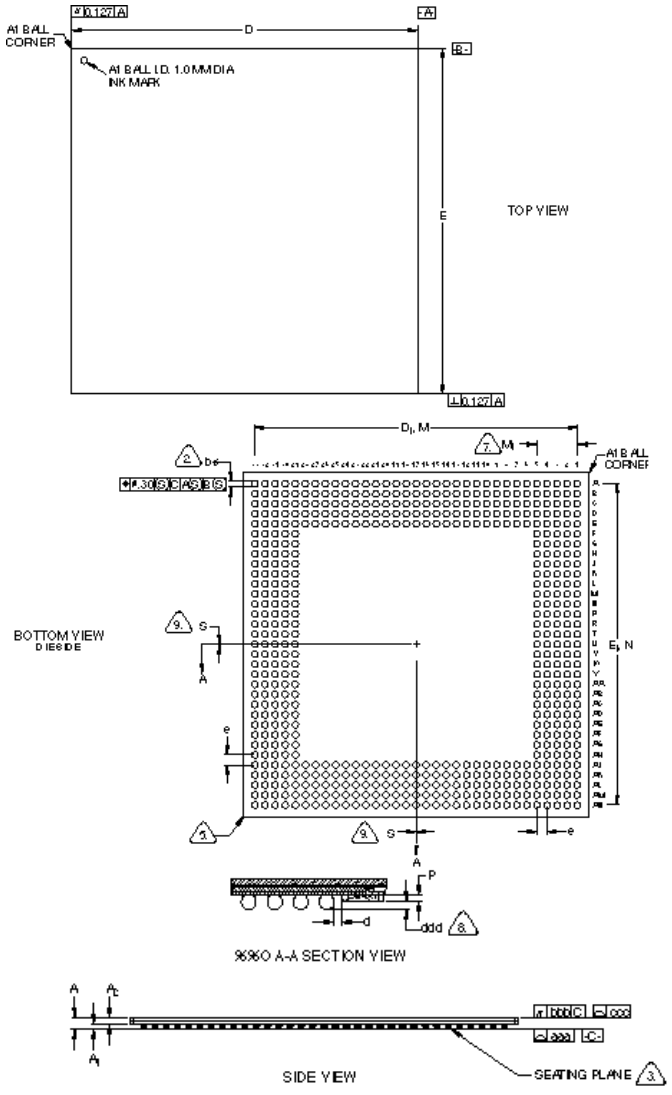
SINGLE FORM

6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. NUMBER OF ROWS IN FROM EDGE TO CENTER.
8. HEIGHT FROM BALL SEATING PLANE TO PLANE OF ENCAPSULANT.
9. "S" IS MEASURED WITH RESPECT TO -A- AND -B- AND DEFINES THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW THE VALUE "S"=e/2.
10. THE DIMENSION FROM THE OUTER EDGE OF THE RESIN DAM TO THE EDGE OF THE INNERMOST ROW OF SOLDER BALL PADS IS TO BE A MINIMUM OF 0.50mm.

SYMBOL	eSBGA 352		
	MIN	NOM	MAX
A	1.41	1.54	1.67
A_1	0.56	0.63	0.70
A_2	0.85	0.91	0.97
C	31.65	31.75	31.85
D	34.90	35.00	35.10
D_1	31.65	31.75	31.85
E	34.90	35.00	35.10
E_1	31.65	31.75	31.85
M,N	26 x 26		
M_1 (7)	2-4		
b	0.60	0.75	0.90
d	0.6		
e	1.27		
aaa			0.15
bbb			0.15
ccc			0.10
ddd (8)	0.15	0.33	0.40
P	0.20	0.30	0.50
S	—	—	0.135

Note: The 352-Pin eSBGA packages are compliant with JEDEC MO-151/MO-192 package outline.

560-Pin eSBGA Package Mechanical Drawings



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C- .
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. PIN A1 I.D. MARKED BY INK.
5. SHAPE AT CORNER.

SINGLE FORM

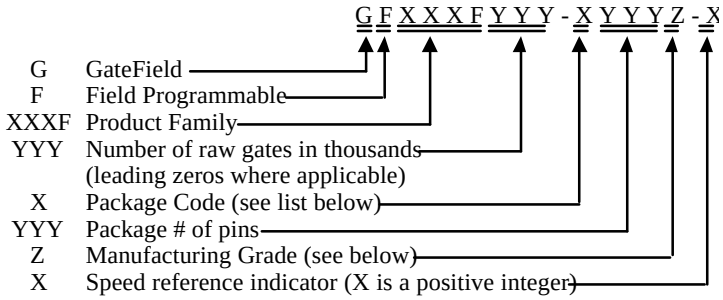
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. NUMBER OF ROWS IN FROM EDGE TO CENTER .
8. HEIGHT FROM BALL SEATING PLANE TO PLANE OF ENCAPSULANT.
9. "S" IS MEASURED WITH RESPECT TO -A- AND -B- AND DEFINES THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "S" = .000.
10. THE DIMENSION FROM THE OUTER EDGE OF THE RESIN DAM TO THE EDGE OF THE INNERMOST ROW OF SOLDER BALL PADS IS TO BE A MINIMUM OF 0.50mm.

SYMBOL	eSBGA 560		
	MIN	NOM	MAX
A	1.41	1.54	1.67
A_1	0.56	0.63	0.70
A_2	0.85	0.91	0.97
C	40.54	40.64	40.74
D	42.40	42.50	42.60
D_1	40.54	40.64	40.74
E	42.40	42.50	42.60
E_1	40.54	40.64	40.74
M,N	33 x 33		
M_1 (7)	3-5		
b	0.60	0.75	0.90
d	0.6		
e	1.27		
aaa			0.15
bbb			0.15
ccc			0.20
ddd (8)	015	0.33	0.50
P	0.20	0.30	0.45
S	—	—	0.100

Note: The 560-Pin eSBGA packages are compliant with JEDEC MO-151/MO-192 package outline

Ordering Information (Part Number Description)

PRODUCT CODING



Package Code List:

M	MQUAD	Metal Quad Flatpack
B	eSBGA	enhanced Super Ball Grid Array
C	CPGA	Ceramic Pin Grid Array

Manufacturing Grade:

C	Commercial

Example:
GF150F050-M208C-4

GateField Sales Offices

	Location	Phone
Domestic		
Zycad Corp.	California	510-249-5757
Zycad Corp.	Massechuetts	508-303-3627
Zycad Corp.	New Jersey	201-989-2900
Zycad Corp.	Texas	972-789-8124
International		
Zycad Ltd.	England	01344-51515
Zycad sarl	France	01-46-105016
Zycad GmbH	Germany	089-9624260
Zycad Japan KK	Japan	045-471-1500
Intellect, Inc.	Korea	02-568-0221
Zycad Corp.	Taiwan	03-572-8850

Manufacturing Reps

	Location	Phone
Domestic		
ESE	Alabama	205-830-1812
Bager Electronics	Arizona	602-968-7406
RSVP Associates	California/San Jose	408-467-1200
Aspen Technologies	California/Folsom	916-985-3000
Platinum Associates	California/Irvine	714-851-2477
Platinum Associates	California/San Diego	619-824-0077
Platinum Associates	Calif./Westlake Village	818-879-5900
NGR Lindco	Connecticut	203-266-0728
Dyne-a-Mark Corp.	Florida/Maitland	407-660-1661
Dyne-a-Mark Corp.	Florida/Ft. Lauderdale	954-485-3500
ESE	Georgia	770-242-7440
Carlson Electr. Sales	Illinois	847-956-8240
Five Star Electronics	Indiana/Indianapolis	317-879-0940
Carlson Electr. Sales	Indiana/Carmel	317-575-4888
Carlson Electr. Sales	Iowa	319-377-6341
Nexus Tech. Sales	Maryland/Baltimore	410-488-3025
Nexus Tech. Sales	Maryland/Frederick	301-663-4159
Compass Technology	Massachusetts	617-272-9990
Electromec Sales	Minnesota	612-894-8200
Metro Logic Corp.	New Jersey/Fairfield	201-575-5585
Metro Logic Corp.	New Jersey/Flaunders	201-252-0001
Metro Logic Corp.	New York/Westbury	516-333-8212
Metro Logic Corp.	New York/Kings Park	516-979-0921
ELCOM Sales	New York/Pittsford	716-385-1400
Quantum Marketing	North Carolina/Raleigh	919-846-5728
Quantum Marketing	North Carolina/Charlotte	704-536-8558
Quantum Marketing	N.Carolina/Hendersonville	704-698-0244
Five Star Electronics	Ohio/Solon	216-349-1611
Five Star Electronics	Ohio/Dayton	937-299-1718
Five Star Electronics	Ohio/Hilliard	614-529-8031
Micro Sales Inc.	Oregon	503-645-2841
Five Star Electronics	Pennsylvania/Pittsburg	413-488-7352
Nexus Tech. Sales	Pennsylvania/Horsham	215-675-9600
Gardin Moor Sales	Texas/Austin	512-794-2900
Gardin Moor Sales	Texas/Plano	972-985-1193
Gardin Moor Sales	Texas/Stafford	281-240-6767
Bager Electronics	Utah	801-582-0501
Nexus Tech. Sales	Virginia	804-589-4246
Micro Sales Inc.	Washington	425-451-0568
Carlson Elec. Sales	Wisconsin	414-476-2790
International		
Canada		
Longman Sales	Alberta	403-295-6324
Longman Sales	British Colombia	604-454-0045
Longman Sales	Ontario/Nepean	613-564-0100
Longman Sales	Ontario/Mississauga	905-670-8100
Longman Sales	Quebec	514-694-3911
Europe		
SICAN	Germany	0511-277-1464
Hantro Products	Finland	358-8-5514-406
Asia		
Rohm Co. Ltd.	Japan	075-311-2121
PTC Systems PTE	Singapore	065-282-0255

GATEFIELD
a Zycad division
47100 Bayside Parkway • Fremont, CA 94538-9942
(800) 818-5052 • (510) 249-5757 • FAX (510) 623-4484
gfinfo@gatefield.com • www.gatefield.com

© 1997 Zycad Corporation 5/97

Zycad Corporation is a registered trademark and GateField is a trademark of Zycad Corporation. The GateField logo, GF200F, GF250F, ProASIC, ASICmaster, ASICmaker, and MEMORYmaster are trademarks of GateField, a Zycad division. All other trademarks are owned by their respective holders.

Zycad Corporation reserves the right to make changes to any products and services herein at any time without notice. Zycad does not assume any responsibility or liability arising out of the application or use of any product or service described herein, except as expressly agreed to in writing by Zycad; nor does the purchase, lease, or use of a product or service from Zycad convey a license under any patent rights, copyrights, trademark rights, or any other of the intellectual property rights of Zycad or of third parties.