STANDARD MICROSYSTEMS CORPORATION

GT3200-DIE

USB 2.0 PHY IC Die

Data Brief

Product Features

- Designed on the TSMC 0.18µ Generic Logic Process (CL018G) with 1.8V core and 3.3V I/O
- USB-IF "Hi-Speed" certified to USB 2.0 electrical specification
- Interface compliant with the UTMI specification (60MHz 8-bit unidirectional interface and 30MHz 16-bit unidirectional interface)
- Supports 480Mbps High Speed (HS) and 12Mbps Full Speed (FS) serial data transmission rates
- Integrated 45Ω and 1.5kΩ termination resistors save 3 external components
- Internal short circuit protection of DP and DM lines
- On-chip oscillator operates with low cost 12MHz crystal
- Robust and low power digital clock and data recovery circuit
- SYNC and EOP generation on transmit packets and detection on receive packets
- NRZI encoding and decoding
- Bit stuffing and unstuffing with error detection
- Supports the USB suspend state, HS detection, HS Chirp, Reset and Resume
- Support for all test modes defined in the USB 2.0 specification
- Draws 72mA (185mW) maximum power dissipation in HS mode – ideal for bus powered functions
- Highly optimized circuit design and layout provide industry's smallest die size
- On-die decoupling capacitance and isolation for immunity to digital switching noise
- Supports junction operating range from -40°C to +125°C
- Die are shipped in wafer form on 8-inch diameter wafers
- Wafers are 100% probe tested prior to shipment

For detailed electrical characteristics and timing diagrams, please refer to the GT3200-JD datasheet at **www.smsc.com**

PRELIMINARY

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General Description

The GT3200-Die provides the Physical Layer (PHY) interface to a USB 2.0 Device Controller. The GT3200-Die is ideal for Multi-Chip Module (MCM) applications where the PHY and Device Controller are discrete IC solutions.

Product Description

The GT3200-Die is a USB 2.0 physical layer (PHY) integrated circuit. SMSC's proprietary technology results in low power dissipation, which is ideal for building a bus powered USB 2.0 peripheral. The PHY IC supports both an 8-bit and 16-bit unidirectional parallel interface, which complies with the USB Transceiver Macrocell Interface (UTMI) specification. It supports Hi-Speed 480Mbps data transfer rate, while remaining backward compatible with USB 1.1 legacy Full-Speed protocol at 12Mbps.

All required termination for the USB 2.0 Transceiver is internal. Internal 5.25V short circuit protection of DP and DM lines is provided for USB compliance.

While transmitting data, the PHY serializes data and generates SYNC and EOP fields. It also performs needed bit stuffing and NRZI encoding. Likewise, while receiving data, the PHY de-serializes incoming data, stripping SYNC and EOP fields and performs bit un-stuffing and NRZI decoding.

The GT3200-Die is shipped in wafer form on eight-inch diameter wafers. All shipped wafers meet internal SMSC critical parameter specifications for wafers. Each die is probed for compliance to datasheet electrical and functional specifications with bad die being marked with an ink dot. A complete die specification including die dimensions and bonding pad coordinates is available under a non-disclosure agreement.

To sign a NON-DISCLOSURE AGREEMENT and receive a detailed GT3200-DIE datasheet, please contact: **www.usb2info@smsc.com**

Applications

The Universal Serial Bus (USB) is the preferred interface to connect high-speed PC peripherals.

- Scanners
- Printers
- External Storage and System Backup
- Still and Video Cameras
- PDAs
- CD-RW
- Gaming Devices

GT3200 Die Reference Designs

- A GT3200 test chip is available in a 64-lead packaged device.
- The GT3000EVB is a card designed to plug into the user's test system for prototype testing using a standard interface. The board includes the GT3200 packaged silicon and all associated external components.
- The GT3000EVS is a mezzanine card designed to plug into an FPGA development board.