*Multi*GEN™ GF9331
SDTV/HDTV Motion Co-processor

PRELIMINARY DATA SHEET

FEATURES

- seamless interface to Gennum's GF9330 using the edge adaptive and vertical motion adaptive control bus (4-bits)
- support for multiple input data formats with multiplexed and separate Y/C channels
- ability to extract HVF information from embedded TRS
- edge detection along nine directions
- vertical motion detection
- support for both 8-bit and 10-bit video signals
- flexibility to handle generic input data formats that have less than 2046 active samples per line
- user configuration through a dedicated host interface, supporting parallel and serial interfaces
- seamless interface to Gennum's GS1500/GS1510/ GS9020
- seamless interface to popular NTSC/PAL decoders
- default power-up mode
- dedicated $\overline{\text{RESET}}$ pin
- 5V tolerant inputs
- 3.3V supply for device I/O and 2.5V for core logic
- IEEE 1149.1 compliant JTAG test port
- internal clock doubler

DEVICE OVERVIEW

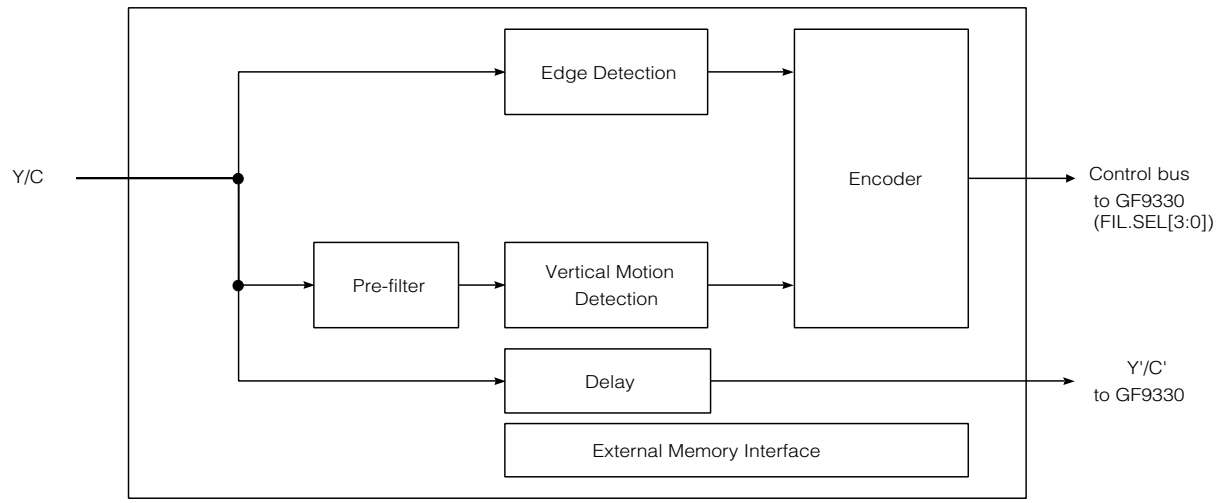
The GF9331 is a high performance motion co-processor that is used in conjunction with Gennum's GF9330 SDTV/ HDTV De-interlacer. Together, the GF9331 and the GF9330 implement a motion adaptive de-interlacer for both SDTV and HDTV digital television signals. The GF9331 contains pixel-based adaptive edge detectors that cover nine different edge directions and a vertical motion detector that covers special motions in the vertical direction. Edge sensitive and motion adaptive control signals are generated by the GF9331 and fed to the GF9330. The GF9331 integrates all the necessary line delays for the motion/edge detectors. The GF9331 also provides seamless interfaces to off-chip SDRAMs that form the required field delays.

APPLICATIONS

- HDTV Upconverters/Downconverters
- Projection Systems
- Plasma Displays/LCD Displays
- Video Walls
- Home Theater Systems
- HD DVD Players

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
GF9331-CBP	328 PIN BGA	0°C to 70°C



BLOCK DIAGRAM

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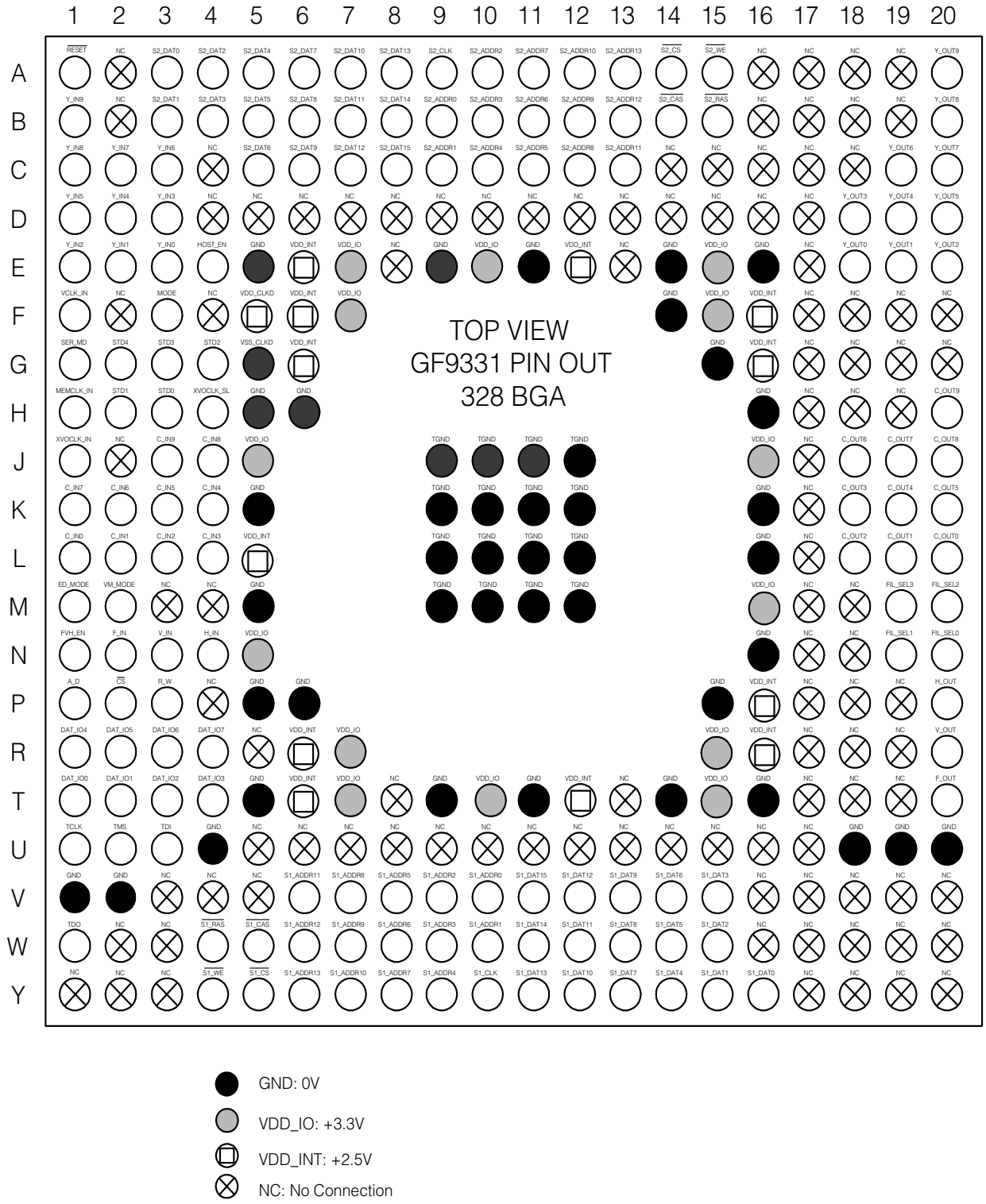


Fig. 1 Top View Pin Out 328 BGA

PIN DESCRIPTIONS

SYMBOL	PIN GRID	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	A1	I	Active low, asynchronous $\overline{\text{RESET}}$. Resets all internal logic to default conditions. Should be applied on power up
VCLK_IN	F1	I	Video Input Clock. When the input is SDTV the input clock will be 27, 36, 54 or 72MHz. When the input format is HDTV, the input clock will be 74.25 or 74.25/1.001MHz.
MEMCLK_IN	H1	I	Memory Clock for SDRAM operation to support HD modes, 90MHz input (supplied by an off-chip crystal oscillator).
XVOCLK_IN	J1	I	External Video Output Clock. This input may be used instead of the internal clock doubler for VCLK_IN to supply the internal VOCLK. SD only applications may use VOCLK to supply S1_CLK and S2_CLK rather than MEMCLK_IN.
XVOCLK_SL	H4	I	Control signal input. When high, selects external VOCLK source; when low, selects the internal VCLK_IN clock doubler for generation of the internal VOCLK signal (required only for SD only applications where VOCLK is used to supply S1_CLK and S2_CLK).
Y_IN[9:0]	B1,C1,C2,C3,D1,D2, D3,E1,E2,E3	I	8/10-bit input data bus for separate luminance or multiplexed luminance and colour difference video data. When supplying 8-bit data to the GF9331, Y_IN[1:0] will be set low and the 8-bit data supplied to Y_IN[9:2].
C_IN[9:0]	J3,J4,K1,K2,K3,K4,L4, L3,L2,L1	I	8/10-bit input data bus for colour difference video data. When supplying 8-bit data to the GF9331, C_IN[1:0] will be set low and the 8-bit data supplied to C_IN[9:2].
F_IN	N2	I	Video timing control. F_IN identifies the ODD and EVEN fields in the incoming video signal. F_IN will be low in Field 1 and high in Field 2.
V_IN	N3	I	Video timing control. V_IN represents the vertical blanking signal associated with the incoming video signal. V_IN is high during the vertical blanking interval and low during active video.
H_IN	N4	I	Video timing control. H_IN represents the horizontal blanking signal associated with the incoming video signal. H_IN is high during horizontal blanking and low during active video.
FVH_EN	N1	I	Control signal input. When high, the F_IN, V_IN, and H_IN input pins will be used for video data signaling. When low, embedded TRS's will be detected for video data signaling.
VM_MODE	M2	I	Control signal input. When high, the vertical motion detection is enabled.
ED_MODE	M1	I	Control signal input. When high, the edge direction detection is enabled.
STD[4:0]	G2,G3,G4,H2,H3	I	Video format definition. Defines the video standard when operating without the host interface. See Table 1. STD[4:0] is read into the device on a high to low transition of HOST_EN or after a $\overline{\text{RESET}}$.
MODE	F3	I	Operation mode selection. When high, the GF9331 motion co-processing is enabled. When low, the GF9331 motion co-processing is bypassed. See section 7.0. MODE is read into the device on a high to low transition of HOST_EN or after a $\overline{\text{RESET}}$.
HOST_EN	E4	I	Host interface enable. When set high, the GF9330 is then configured through the host interface. When set low, the GF9330 is manually configured via input pins.
SER_MD	G1	I	Host interface mode selection. Enables serial mode operation when high. Enables parallel mode operation when low.
$\overline{\text{CS}}$	P2	I	Functions as an active low chip select input for host interface parallel mode operation. Functions as a serial clock input for host interface serial mode operation.

PIN DESCRIPTIONS (Continued)

SYMBOL	PIN GRID	TYPE	DESCRIPTION
DAT_IO[7:0]	R4,R3,R2,R1,T4,T3, T2,T1	I/O	Host interface bi-directional data bus for parrallel mode. In serial mode, DAT_IO[7] serves as the serial data output pin and DAT_IO[0] serves as the serial data input pin.
R_W	P3	I	Host interface Read/Write control for parallel mode. A read cycle is defined when high, a write cycle is defined when low.
A_D	P1	I	Host interface Address/Data control for parallel mode. The DATA bus contains an address when high, a data word when low. In serial mode, this pin serves as the chip select (active low).
Y_OUT[9:0]	A20,B20,C20,C19,D20, D19,D18,E20,E19,E18	O	Output data bus for separate luminance or multiplexed luminance and colour difference video data.
C_OUT[9:0]	H20,J20,J19,J18,K20,K 19,K18,L18,L19,L20	O	Output data bus for colour difference video data.
FIL_SEL[3:0]	M19,M20,N19,N20	O	Filter Selection control bus output to the GF9330. The FIL_SEL[3:0] bus is used to switch the GF9330's internal directional filters on a pixel by pixel basis.
H_OUT	P20	O	Output control signal. H_OUT is a horizontal blanking output.
F_OUT	T20	O	Output control signal. F_OUT is an ODD/EVEN field indicator.
V_OUT	R20	O	Output control signal. V_OUT is a vertical blanking output.
S1_CLK	Y10	O	SDRAM bank 1 clock.
$\overline{\text{S1\_CS}}$	Y5	O	Active low SDRAM chip select for Field Buffer 1.
$\overline{\text{S1\_RAS}}$	W4	O	Active low SDRAM row address strobe for Field Buffer 1.
$\overline{\text{S1\_CAS}}$	W5	O	Active low SDRAM column address strobe for Field Buffer 1.
$\overline{\text{S1\_WE}}$	Y4	O	Active low SDRAM write enable for Field Buffer 1.
S1_ADDR[13:0]	Y6,W6,V6,Y7,W7,V7, Y8,W8,V8,Y9,W9,V9, W10,V10	O	SDRAM address for Field Buffer 1.
S1_DAT[15:0]	V11,W11,Y11,V12,W12, Y12,V13,W13,Y13,V14, W14,Y14,V15,W15, Y15,Y16	I/O	SDRAM data for Field Buffer 1.
S2_CLK	A9	O	SDRAM bank 2 clock.
$\overline{\text{S2\_CS}}$	A14	O	Active low SDRAM chip select for Field Buffer 2.
$\overline{\text{S2\_RAS}}$	B15	O	Active low SDRAM row address strobe for Field Buffer 2.
$\overline{\text{S2\_CAS}}$	B14	O	Active low SDRAM column address strobe for Field Buffer 2.
$\overline{\text{S2\_WE}}$	A15	O	Active low SDRAM write enable for Field Buffer 2.
S2_ADDR[13:0]	A13,B13,C13,A12,B12, C12,A11,B11,C11,C10, B10,A10,C9,B9	O	SDRAM address for Field Buffer 2.
S2_DAT[15:0]	C8,B8,A8,C7,B7,A7, C6,B6,A6,C5,B5,A5, B4,A4,B3,A3	I/O	SDRAM data for Field Buffer 2.
TDI	U3	I	JTAG data input; connect to GND if not used.
TMS	U2	I	JTAG mode select; connect to GND if not used.

PIN DESCRIPTIONS (Continued)

SYMBOL	PIN GRID	TYPE	DESCRIPTION
TCLK	U1	I	JTAG test clock; connect to GND if not used.
TDO	W1	O	JTAG data output.
VDD_CLKD	F5	NA	2.5 V supply for the internal clock doubler.
VSS_CLKD	G5	NA	Ground connection for the internal clock doubler.
VDD_IO	E7,E10,E15,F7,F15,J5, J16,M16,N5,R7,R15,T7, T10,T15	NA	3.3 V supply.
VDD_INT	E6,E12,F6,F16,G6,G16, L5,P16,R6,R16,T6,T12	NA	2.5 V supply.
GND / TGND	E5,E9,E11,E14,E16, F14,G15,H5,H6, H16,J9,J10,J11,J12,K5, K9,K10,K11,K12,K16, L9,L10,L11,L12,L16, M5,M9,M10,M11,M12, N16,P5,P6,P15,T5,T9, T11,T14,T16,U4,U18, U19,U20,V1,V2	NA	Device ground / Thermal ground (electrically equivalent).
NC	A2,A16,A17,A18,A19, B2,B16,B17,B18,B19, C4,C14,C15,C16,C17, C18,D4,D5,D6,D7,D8, D9,D10,D11,D12,D13, D14,D15,D16,D17,E8, E13,E17,F2,F4,F17, F18,F19,F20,G17,G18, G19,G20,H17,H18, H19,J2,J17,K17,L17, M3,M4,M17,M18,N17, N18,P4,P17,P18,P19, R5,R17,R18,R19,T8, T13,T17,T18,T19,U5, U6,U7,U8,U9,U10,U11, U12,U13,U14,U15,U16, U16,U17,V3,V4,V5,V16, V17,V18,V19,V20,W2, W3,W16,W17,W18, W19,W20,Y1,Y2,Y3, Y17,Y18,Y19,Y20	NA	No Connection.

ELECTRICAL CHARACTERISTICS

5V Tolerant Inputs

Input cells used in the design are able to withstand 3.3V or 5V CMOS input signals, as well as TTL compatible inputs without degrading performance or long-term reliability.

ESD Tolerance

GF9331 has 2 kV ESD protection. ESD testing is done in accordance with Gennum's standard ESD testing procedure.

3.3V Supply for Device I/0 and 2.5V for Core Logic

The GF9331 operates from a single +3.3V supply for device I/O and a single +2.5V supply for core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE
Device I/O Supply Voltage	V_{DDIO}	-0.5 to TBD V
Device Core Supply Voltage	V_{DDCORE}	-0.5 to TBD V
Input Voltage Range (any input)	V_{IN}	$-0.5 < V_{IN} < +4.6V$
Operating Temperature Range	T_A	$0°C < T_A < 70°C$
Storage Temperature Range	T_S	$-40°C < T_S < 125°C$
Lead Temperature (soldering 10 seconds)		260°C

DC ELECTRICAL CHARACTERISTICS

V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Device I/O Supply Voltage		V_{DDIO}	+3.0	+3.3	+3.6	V	1
Device Core Supply Voltage		V_{DDCORE}	+2.25	+2.5	+2.75	V	1
Device I/O Supply Current	V_{DDIO}=3.6V	I_{DDIO}			TBD	mA	1
Device Core Supply Current	V_{DDCORE}=2.75V	I_{DDCORE}			TBD	mA	1
Input Leakage Current	I_{IN}=0V or I_{IN}=V_{DD}	I_{LEAK}			10	µA	1
Input Logic LOW Voltage		V_{IL}	--	--	0.8	V	1
Input Logic HIGH Voltage		V_{IH}	2.1	--	--	V	1
Output Logic LOW Voltage	I_{OL}= 4mA	V_{OL}	--	0.2	0.4	V	1
Output Logic HIGH Voltage	I_{OH}= -4mA	V_{OH}	2.7	--	--	V	1

NOTES:
1. Production, test and QA are performed at room tempature.

AC ELECTRICAL CHARACTERISTICS - Video Interfaces

The Video Interface signals include VCLK, Y_IN, C_IN, FIL_SEL[3:0], F_IN, V_IN, H_IN, FVH_EN, FF_EN, Y_OUT, C_OUT, H_OUT, F_OUT and V_OUT.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI}	--	74.25	83	MHz	1, 2
Input Data Setup Time		t_{SU}	2.5	--	--	ns	1, 3
Input Data Hold Time		t_{IH}	1.5	--	--	ns	1, 3
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD}	--	--	10.0	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN}	--	--	10	ns	1
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS}	--	--	10	ns	1
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF}	--	--	2.0	ns	1, 4

NOTES:
1. Based on simulation results, verified during device characterization process.
2. Also supports 74.25/1.001MHz.
3. 50% levels.
4. 20% to 80% levels.

AC ELECTRICAL CHARACTERISTICS - SDRAM Interfaces

The SDRAM 1 Interface signals include S1_CLK, S1_CS, S1_RAS, S1_CAS, S1_WE, S1_ADDR[13:0] and S1_DAT[15:0]. The SDRAM 2 Interface signals include S2_CLK, S2_CS, S2_RAS, S2_CAS, S2_WE, S2_ADDR[13:0] and S2_DAT[15:0].
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI_SD}	--	85	90	MHz	1
Input Data Setup Time		t_{SU_SD}	2.0	--	--	ns	1, 2
Input Data Hold Time		t_{IH_SD}	2.5	--	--	ns	1, 2
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_SD}	--	--	9.1	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_SD}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_SD}	--	--	20	ns	1, 4
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_SD}	--	--	20	ns	1, 4
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_SD}	--	--	2.0	ns	1, 3

NOTES:
1. Based on simulation results, verified during device characterization process.
2. 50% levels.
3. 20% to 80% levels.
4. Two clock cycles allocated for data bus turnaround.

AC ELECTRICAL CHARACTERISTICS - Host Interface

The Host Interface signals include HOST_EN, SER_MD, CS, DAT_IO[7:0], R_W and A_D.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI_HI}	--	--	20	MHz	1
Input Data Setup Time		t_{SU_HI}	5	--	--	ns	1, 2
Input Data Hold Time		t_{IH_HI}	1.5	--	--	ns	1, 2
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_HI}	--	--	10.0	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_HI}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_HI}	--	--	15	ns	1
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_HI}	--	--	15	ns	1
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_HI}	--	--	2.0	ns	1, 3

NOTES:
1. Based on simulation results, verified during device characterization process.
2. 50% levels.
3. 20% to 80% levels.

DETAILED DEVICE DESCRIPTION

1. INPUT DATA FORMATS

The GF9331 supports multiple input data formats with multiplexed or separate Y/C channels. Data is supplied to the GF9331 through the Y_IN[9:0] and the C_IN[9:0] busses. Table 1 outlines the data formats that the GF9331 supports according to the setting of STD[4:0] pins or host interface bits, STD[4:0].

Note: For all progressive video standards the GF9331 must be manually set to bypass mode. (MODE[2:0] = 111)

TABLE 1: Encoding of STND[4:0] for Selecting Input Data Format

STD	STD[4:0]	DESCRIPTION
0	00000	525i (30/1.001) component SMPTE 125M. Multiplexed Y Cb Cr data applied to Y_IN. C_IN should be set low. Note: Input clock is 27MHz.
1	00001	RESERVED.
2	00010	525i (30/1.001) component 16x9 SMPTE 267M. Multiplexed Y Cb Cr data applied to Y_IN. C_IN should be set low. Note: Input clock is 36MHz.
3	00011	RESERVED
4	00100	625i (25Hz) component EBU tech. 3267E. Multiplexed Y Cb Cr data applied to Y_IN. C_IN should be set low. Note: Input clock is 27MHz.
5	00101	RESERVED
6	00110	625i (25Hz) component 16x9 ITU-R BT.601-5 Part B. Multiplexed Y Cb Cr data applied to Y_IN. C_IN should be set low. Note: Input clock is 36MHz.
7	00111	RESERVED
8	01000	525p (60/1.001Hz) SMPTE 293M. Y Cb Cr data stream applied to Y_IN. C_IN should be set low. Timing information is extracted from embedded TRS sequences. Note: Input clock is 54MHz.
9	01001	RESERVED
10	01010	RESERVED
11	01011	RESERVED
12	01100	625p (50Hz) ITU-R BT.1358. Y Cb Cr data stream applied to Y_IN. C_IN should be set low. Timing information is extracted from embedded TRS sequences. Note: Input clock is 54MHz.
13	01101	625p (50Hz) 16 x 9 with 18MHz sampling. Y Cb Cr data stream applied to Y_IN. C_IN should be set low. Timing information is extracted from embedded TRS sequences. Note: Input clock is 72MHz.
14	01110	Generic SD input data format with 4:1:1 sampling. Y Cb Cr data is applied to both Y_IN and C_IN. The externally supplied F, V and H signals are used to synchronize the input data stream. Note: Input clock is 27MHz.
15	01111	Generic SD input data format with 4:2:2 sampling and single multiplexed Y Cb Cr input format. Y Cb Cr data applied to Y_IN. C_IN should be set low. The externally supplied F, V and H signals are used to synchronize the input data stream. Note: Input clock is 27 or 36MHz.
16	10000	720p (60 & 60/1.001Hz) SMPTE 296M January 1999 Draft (System #1 and #2). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
17	10001	720p (30 & 30/1.001Hz) SMPTE 296M January 1999 Draft (System #4 and #5). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
18	10010	1080p (30 & 30/1.001Hz) SMPTE 274M (System #7 and #8). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
19	10011	720p (50Hz) SMPTE 296M January 1999 Draft (System #3). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.

TABLE 1: Encoding of STND[4:0] for Selecting Input Data Format

STD	STD[4:0]	DESCRIPTION
20	10100	1080p (25Hz) SMPTE 274M (System #9). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
21	10101	720p (25Hz) SMPTE 296M January 1999 Draft (System #6). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
22	10110	1080p (24 & 24/1.001Hz) SMPTE 274M (System # 10 and #11). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
23	10111	720p (24 & 24/1.001Hz) SMPTE 296M January 1999 Draft (System #7 and #8). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
24	11000	1080i (30 & 30/1.001Hz) SMPTE 274M (System #4 and #5). Y data applied to Y_IN. Cb/Cr data applied to C_IN. Note: Input clock is 74.25 MHz or 74.25/1.001MHz.
25	11001	1080p (30 & 30/1.001Hz in Segmented Frame Format) SMPTE Draft RP May 99 (System #12 and #13). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
26	11010	1080i (25Hz) SMPTE 274 (System # 6). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
27	11011	1080p (25Hz in Segmented Frame Format) SMPTE Draft RP May 99 (System #14). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
28	11100	1080i (25Hz) SMPTE 295M (System #2). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
29	11101	1080p (24 & 24/1.001Hz in Segmented Frame Format) Draft RP May 99 (System #15 & #16). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
30	11110	1035i (30Hz) SMPTE 260M. Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
31	11111	Generic HD input data format with 4:2:2 sampling and a separate Y/C format. Y Data applied to Y_IN. Cb Cr data applied to C_IN. The externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. Note: Input clock is 74.25MHz or 74.25/1.001MHz.

2. INPUT SYNCHRONIZATION

The GF9331 obtains relevant timing information from either embedded TRS information or externally supplied H_IN, V_IN, and F_IN signals.

When FVH_EN is set high using either the host interface or the external pin, the GF9331 relies on the externally supplied H_IN , V_IN and F_IN signals for timing information. When FVH_EN is set low, the GF9331 extracts the embedded TRS timing information from the video data stream and ignores any timing information present of the F_IN , V_IN and H_IN pins.

2.1 Support for Both 8-bit and 10-bit Input Data

The GF9331 supports 8-bit and 10-bit input data. When operating with 8-bit input data, the two LSBs of the GF9331's 10-bit input bus should be set low and the input data applied to the 8 MSBs of the input bus.

2.2 Generic Input Format Signaling

The GF9331 supports generic input data formats with either 4:1:1 or 4:2:2 sampling structures that require up to 2046 active samples per line and have maximum total line width of 4096 (active + blanking) samples. In addition, there is a limit of 2048 lines per interlaced frame. The following host interface parameters are programmable to describe the generic input data format relative to the F_IN , V_IN and H_IN signals. See figure 2.

2.2.1 H_BLANK_SIZE

This parameter defines the number of samples that comprise the horizontal blanking region. This parameter has a maximum value of 4095 and is to be less than the total line width (active + blanking) sample size. Twelve bits within the host interface are dedicated to this parameter. The GF9331 stores and processes active video samples only (i.e. H_IN =0).

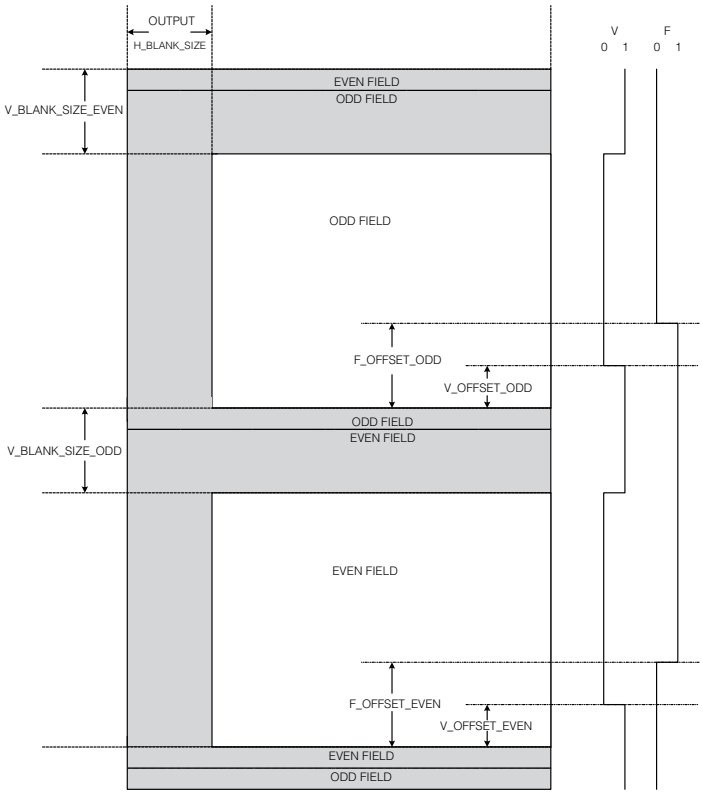


Fig. 2 Generic Input Format Definition

2.2.2 V_BLANK_SIZE_ODD

This parameter defines the number of lines that comprise the vertical blanking interval that follows the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9331 stores and processes active video samples only (i.e. V_IN =0)

2.2.3 V_BLANK_SIZE_EVEN

This parameter defines the number of lines that comprise the vertical blanking interval that follows the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9331 stores and processes active video samples only (i.e. V_IN =0). See Figure 2.

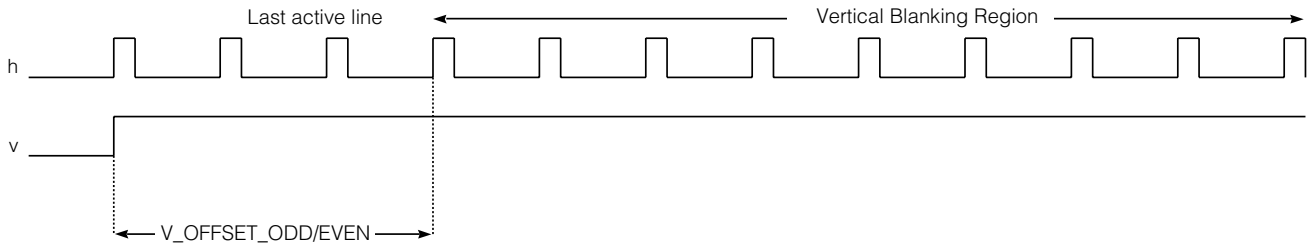


Fig. 2. V_Offset Definition

2.2.4 V_OFFSET_ODD

This parameter defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the V _IN signal. See Figure 2.

2.2.5 V_OFFSET_EVEN

This parameter defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the V_IN signal.

2.2.6 F_OFFSET_ODD

This parameter defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the F_IN signal.

2.2.7 F_OFFSET_EVEN

This parameter defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the F_IN signal.

2.2.8 H_POLARITY

This parameter defines the polarity of the H_IN pin. With H_POLARITY set low, a high-to-low transition on the H_IN pin indicates the end of active video. With H_POLARITY set high, a low-to-high transition on the H_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter.

TABLE 2: F_POLARITY

F_POLARITY	F_IN PIN	F_IN PIN FUNCTION
0	0	Even field
0	1	Odd Field
1	0	Odd Field
1	1	Even Field

2.2.9 F_POLARITY

This parameter defines the polarity of the F_IN pin. Refer to Table 2 for F_POLARITY encoding. One bit within the host interface is dedicated to this parameter.

2.2.10 V_POLARITY

This parameter defines the polarity of the V_IN pin. With V_POLARITY set low, a high-to-low transition on the V_IN pin indicates the end of active video. With V_POLARITY set high, a low-to-high transition on the V_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter

3. SEAMLESS INTERFACE TO THE GF9330 HIGH PERFORMANCE DE-INTERLACER FOR DIRECTIONAL FILTER CONTROL

The GF9330 can operate as a stand-alone de-interlacer or can operate in conjunction with the GF9331 Motion Co-processor. The GF9331 contains adaptive edge detectors that cover nine different directions and a vertical motion detector. Edge sensitive control signals are fed directly to the GF9330. These control signals adaptively switch the GF9330's internal de-interlacing filters on a pixel by pixel basis. These control signals are fed to the GF9330 by the GF9331 over the FIL_SEL[3:0] control bus.

NOTE: When using the GF9331, the Y_IN[9:0] of the GF9330 must be connect to the Y_OUT[9:0] of the GF9331 and the C_IN[9:0] of the GF9330 must be connected to the C_OUT[9:0] of the GF9331. The FIL_SEL[3:0] output of the GF9331 must be connected to the FIL_SEL[3:0] input of the GF9330. Refer to Figure 3 for a pictorial description of connections between the GF9330 and the GF9331.

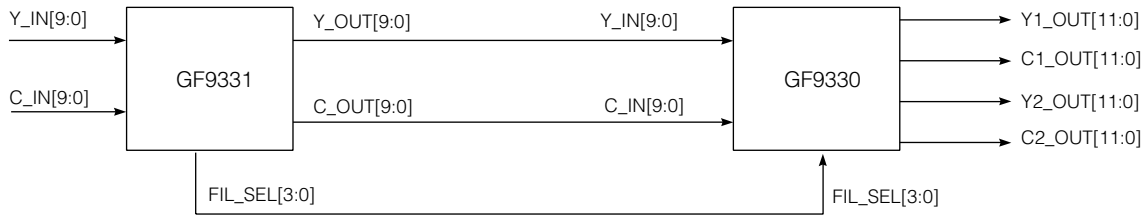


Fig. 3 Using the GF9331 with the GF9330 for Motion Adaptive De-interalcing

4. SEAMLESS INTERFACE TO EXTERNAL SDRAMS

The GF9331 requires two independent external field buffers, each implemented with a 1 Meg (min) x 16-bit SDRAM configuration. This configuration supports all operational modes. The following external SDRAM devices are supported for the external field buffer function.

- NEC: uPD4516161AG5, uPD4564163G5, uPD45128163G5
- Micron: MT48LC4M16A2, MT48LC8M16A2
- Samsung: K4S161622C, K4S641632C, K4S281632B

5. HOST INTERFACE

The GF9331 provides both serial and parallel host interface control ports for the configuration of internal parameters. The GF9331 is also able to operate in stand-alone mode, with no host interface control. In stand-alone mode, the video standard STD[4:0] and mode of operation MODE must be set using dedicated pins on the device. These values are loaded into the device on a high to low transition of HOST_EN or after setting $\overline{\text{RESET}}$ low.

Both the serial and parallel interfaces share common pins as described in Table 4.

TABLE 4: Host Interface Common Pins

GF9331 PIN NAME	PARALLEL MODE	SERIAL MODE
$\overline{\text{CS}}$	CHIP select	SCLK - Serial Clock
DAT_IO0	Data/address (bit 0)	SDI - Serial data in
DAT_IO1	Data/address (bit 1)	(NOT USED)
DAT_IO2	Data/address (bit 2)	(NOT USED)
DAT_IO3	Data/address (bit 3)	(NOT USED)
DAT_IO4	Data/address (bit 4)	(NOT USED)
DAT_IO5	Data/address (bit 5)	(NOT USED)
DAT_IO6	Data/address (bit 6)	(NOT USED)
DAT_IO7	Data/address (bit 7)	SDO - Serial data out
A_D	Address/data select	$\overline{\text{SCS}}$ - Serial chip select
R_W	Read/write select	(NOT USED)
HOST_EN	Host Interface enable	Host Interface enable
SER_MD	low = parallel mode enable	high = Serial mode enable

5.1 Host Interface Serial Mode

The Gennum Serial Peripheral Interface (GSPI) is a 4 wire interface comprised of serial data in (SDI), serial data out (SDO), an active low serial chip select ($\overline{SCS}$), and a clock (SCLK). The interface operates in a master/slave configuration, where the master provides the SCLK, SDI, and $\overline{SCS}$ signals to the slave or slaves. The master uC_SDO drives the slave(s) SDI input The SDO pin is a tristate output to allow multiple devices to drive the master uC_SDI. Serial mode operation supports both a continuous clock and a burst clock configuration. The interface is illustrated in Figure 4.

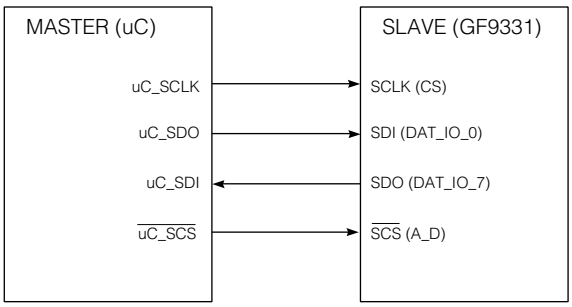


Fig.4 Host Interface Serial Mode

5.1.1 Serial Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Configure control bit, nine reserved bits and a 5-bit address as shown in Figure 5.

Fig. 5 Serial Command Word Bit Representation

The R/W bit indicates a Read command if R/W = high, and a write command when R/W = low.

5.1.2 Auto-Configure

The auto-configure feature will be executed when the Auto-Configure control bit is set (used during write operations only). All Auto-Configure registers will be updated to their appropriate settings based on the currently set video standard and operational mode.

When setting the Auto-Configure bit, the command word should be set with only the AC bit set to 1. All of the 15 other bits should be set to 0. To complete the Auto-Configuration 16 more data bits must be loaded into the device. The state of these bits can be either high or low. Before Auto-Configuring the device, the Standard and Mode must be set using either the Host interface (HOST_EN = 1) or the external pins (with a high to low transition of HOST_EN).

This simplifies configuration while allowing customization of many features and format parameters.

5.1.3 Serial Data Word Description

The serial data word consists of a 16-bit word as shown in Figure 6. Serial data is transmitted or received MSB first.

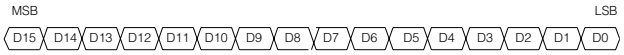


Fig. 6 Serial Data Word Bit Representation

Both command and data words are clocked into the GF9331 on the rising edge of the serial clock (SCLK) which may operate in either a continuous or burst fashion. The first bit (MSB) of the serial output (SDO) is available following the last falling SCLK edge of the "read" command word. The remaining bits are clocked out on the negative edges of SCLK.

5.1.4 Serial Write Operation

All write cycles consist of a command word followed by a data word, both transmitted to the GF9331 via SDI. The first 16-bit word transmitted following a high-to-low transition of $\overline{SCS}$ is a command word. Several write cycles may be performed while $\overline{SCS}$ is low. See Figure 7.

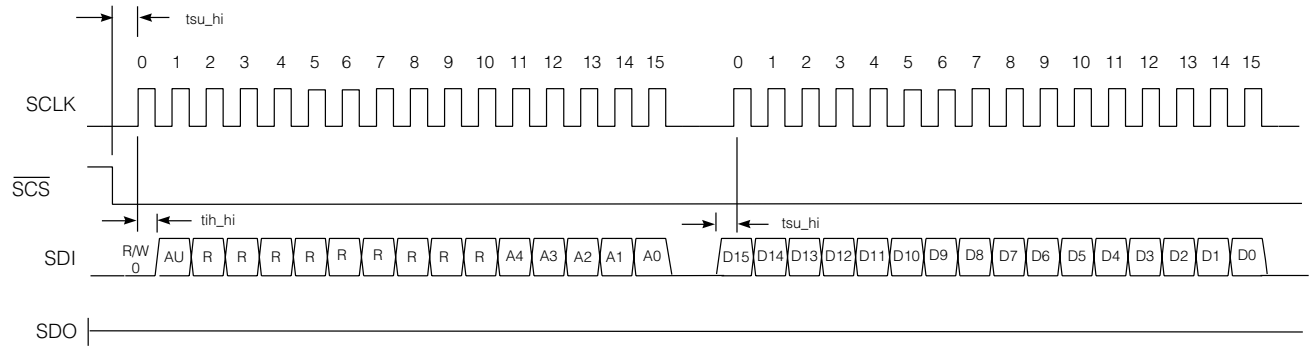


Fig. 7 Write Cycle

5.1.5 Serial Read Operation

All read cycles consist of a command word transmitted to the GF9331 via SDI followed by a data word transmitted from the GF9331 via SDO. The first 16-bit word transmitted following a high-to-low transition of $\overline{SCS}$ is a command word. Several read cycles may be performed while $\overline{SCS}$ is low. See Figure 8.

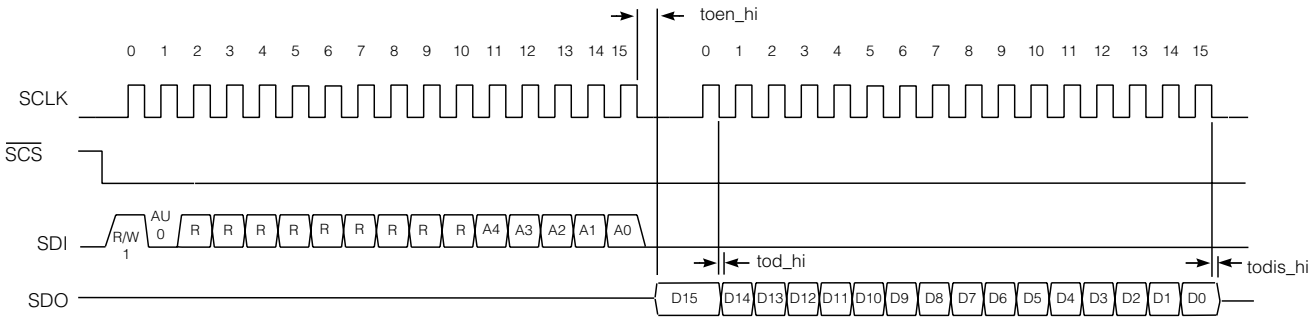


Fig. 8 Read Cycle

5.2 Host Interface Parallel Mode

The Gennum Parallel Peripheral Interface (GPPI) consists of an 8-bit multiplexed address/data bus (DATA_IO[7:0]), a chip select pin ($\overline{CS}$), a read/write pin (R_W), and an address/data pin (A_D) as shown in Figure 9.

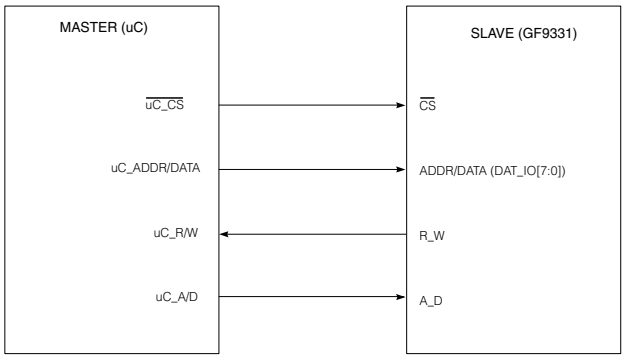


Fig. 9 Host Interface Parallel Mode

Data is strobed in/out of the parallel interface on the falling edge of $\overline{CS}$. The GF9331 drives the DATA_IO[7:0] bus when the R_W pin is HIGH and the $\overline{CS}$ pin is LOW, otherwise this port is in a high impedance state.

5.2.1 Parrallel Address Word Description

The 8-bit Address Word loads in the address to be accessed and allows the Auto-Configure bit to be set. The MSB is the Auto-Configure bit, followed by two reserved bits and a 5-bit address as shown in Figure 10.

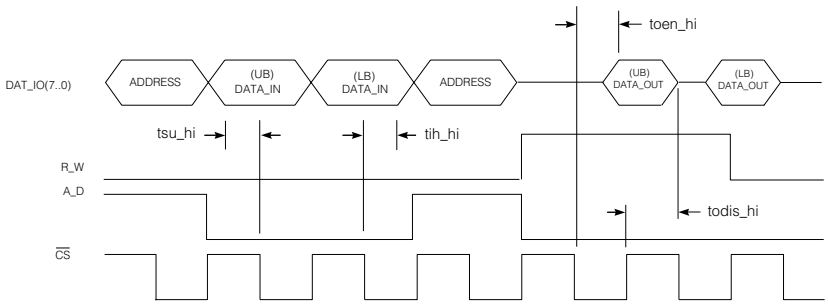


Fig. 10 Write Cycle to the Parallel Interface

5.2.2 Parrallel Write Operation

A write cycle to the parallel interface is shown below. First an 8-bit address word is provided to the DATA_IO port by asserting the R_W pin to LOW and A_D pin to HIGH. The MSB of the address word contains an auto-update flag, which allows automatic configuration of predefined registers (used during write operations only).

The 5 LSB's of the address word contain the address location for the read or write operation. The remaining address word bits DAT_IO[6:5] are reserved. The address word is registered on the falling edge of $\overline{CS}$.

Following this, the A_D pin is driven LOW and two DATA words are sent upper byte (UB) word first and are each clocked in on the falling edge of $\overline{CS}$. Two 8-bit data words must follow each address word to occupy each 16-bit parameter which are defined in Table 5.

5.2.3 Parrallel Read Operation

A read cycle begins with an ADDRESS write by asserting the R_W pin low and A_D HIGH. The address is clocked on the falling edge of CS. Following the address, the R_W pin must be driven HIGH and A_D driven LOW to allow the upper byte of data to be clocked out on the first falling edge of $\overline{CS}$ followed by the lower byte on the second negative edge of $\overline{CS}$. See Figure 10.

TABLE 5: Host Interface Register Allocation

	Hex	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 31	1F	CMD_RESET															START_OPERATION
Address 30	1E														CLK_X1_SEL		EXT_MEMCLK_SEL
Address 29	1D																
Address 28	1C																
Address 27	1B																
Address 26	1A																
Address 25	19																
Address 24	18																
Address 23	17								NO_LINE_DELAYS(9:0)								
Address 22	16		EVEN_LINES_PER_FRAME(1:0)		RELD2_HAS_TOP_LINE				H_BLANK_SIZE(11:0)								
Address 21	15		ID_MODE(1:0)		PROGRESSIVE_INPUT	FORMAT_SD											
Address 20	14																
Address 19	13					V_BLANK_SIZE_ODD(7:0)								V_BLANK_SIZE_EVEN(7:0)			
Address 18	12																
Address 17	11																
Address 16	10																
Address 15	F																
Address 14	E																
Address 13	D																
Address 12	C						CC_BLANK_START_LINE(7:0)							CC_BLANK_END_LINE(7:0)			
Address 11	B																
Address 10	A																
Address 9	9																
Address 8	8																
Address 7	7																
Address 6	6																
Address 5	5																
Address 4	4																
Address 3	3						V_OFFSET_ODD(7:0)							V_OFFSET_EVEN(7:0)			
Address 2	2						F_OFFSET_ODD(7:0)							F_OFFSET_EVEN(7:0)			
Address 1	1	H_POLARITY	V_POLARITY	F_POLARITY	FVH_EN_BIT						CC_BLANK_EN					EDGE_CTL	VM_CTL
Address 0	0												MODE		STD(4:0)		

5.3 Control Register Definition

The host interface internal registers are divided into two classes: User Configurable (UC) and Auto-Configurable (AC). Address locations 0 through 6 contain parameters which may be configured by the user.

Locations 7 through 31 are automatically configured based on the STD[4:0] and MODE registers, but can be user configured if desired.

CONTROL REGISTER DEFINITIONS

ADDRESS	BIT LOCATION	REGISTER NAME	CLASS	DESCRIPTION	DEFAULT
0	4:0	STD[4:0]	UC	Defines the video standard as described in Section 1.	00000
	5	MODE	UC	Enables (MODE=1) or bypasses (MODE=0) the GF9331 processing.	000
1	0	VM_CTL	UC	Enables (VM_CTL=1) or bypass (VM_CTL=0) vertical motion detection of the video input stream	0
	1	EDGE_CTL	UC	Enables (EDGE_CTL=1) or bypasses (EDGE_CTL=0) edge detection of the video input stream.	0
	6	CC_BLANK_EN	UC	Enables (CC_BLANK_EN=1) or bypasses (CC_BLANK_EN=0) blanking in the close captioned video region.	0
	12	FVH_EN_BIT	UC	Enables the GF9331 to use external F_IN, V_IN, H_IN controls (FVH_EN=1) in place of embedded TRS (FVH_EN=0).	0
	13	F_POLARITY	UC	When set to '1', F_IN follows normal convention where F_IN is '0' for field 1(odd) and '1' for field 2 (even).	1
	14	V_POLARITY	UC	Defines the polarity of the V_IN pin. When set to '1', V_IN follows normal convention where V_IN is high in the vertical blanking region.	1
	15	H_POLARITY	UC	Defines the polarity of the H_IN pin. When set to '1', H_IN follows normal convention where H_IN is high in the horizontal blanking region.	1
2	7:0	F_OFFSET_EVEN[7:0]	UC	Defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the even field. This parameter has a maximum value of 255.	00000000
	15:8	F_OFFSET_ODD[7:0]	UC	Defines the number of lines from the F_IN pin EAV transition to the vertical blanking interval following the odd field. This parameter has a maximum value of 255.	00000000
3	7:0	V_OFFSET_EVEN[7:0]	UC	Defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter has a maximum value of 255.	00000000
	15:8	V_OFFSET_ODD[7:0]	UC	Defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255.	00000000
6	7:0	CC_BLANK_END_LINE [7:0]	UC	Defines the last line number at which to end closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.	00000000
	15:8	CC_BLANK_START_LINE [7:0]	UC	Defines the first line number at which to start closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.	00000000

CONTROL REGISTER DEFINITIONS (Continued)

ADDRESS	BIT LOCATION	REGISTER NAME	CLASS	DESCRIPTION	DEFAULT
19	7:0	V_BLANK_SIZE_EVEN[7:0]	AC	Defines the number of lines that comprise the vertical blanking interval that follows the even input field. This parameter has a maximum value of 255.	Auto
	15:8	V_BLANK_SIZE_ODD[7:0]	AC	Defines the number of lines that comprise the vertical blanking interval that follows the odd input field. This parameter has a maximum value of 255.	Auto
21	12	FORMAT_SD	AC	Used to configure the GF9331 SDRAM controller into 8-bit mode for SD video formats. This bit is auto-configured based on standard and mode selection.	Auto
	13	PROGRESSIVE_INPUT	AC	Configures the GF9331 to accept a progressive video format. This bit is auto-configured based on standard and mode selection.	Auto
	15:14	ID_MODE[1:0]	AC	Defines the type of video sequence for input video de-multiplexing. When set to "00" the input represents a 4:2:2 sequence, "01" represents a 4:1:1 sequence, and "10" represents an HD format. This word can be auto-configured based on video standard and mode.	Auto
22	11:0	H_BLANK_SIZE[11:0]	AC	Defines the number of horizontal blanked input words per line which corresponds to 2 times the number of blanking pixels per line for 4:2:2 SD modes and is equal to the number of pixels per line for HD formats (maximum 4095). This value can be auto-configured.	Auto
	13	FIELD2_HAS_TOP_LINE	AC	Set high when field 2, line one is the first line in the video frame (SMPTE 260M).	Auto
	15:14	EVEN_LINES_PER_FRAME [1:0]	AC	Set to 11 for video standards that have an even number of lines per frame such as SMPTE 295M, otherwise set to 00.	Auto
23	9:0	NO_LINE_DELAYS[9:0]	AC	Defines the number of line delays to implement within the external field delay. This value is auto-configured based on standard and mode. The calculation is: No_line_delays = (Total number of lines per frame - 3) / 2.	Auto
30	0	EXT_MEMCLK_SEL	AC	Controls the selection of the SDRAM clock source. For VCLK_IN frequencies less than 36MHz, the internal clock doubler can be used. In all other modes an external source is required (MEMCLK_IN).	Auto
	2	CLK_X1_SEL	AC	This parameter is normally set for all HD modes and is '0' for all other cases	Auto
31	15	CMD_RESET	UC	This parameter forces the GF9331 to enter a reset state. The reset remains in effect until this parameter is cleared with a subsequent command.	0
	15	START_OPERATION	UC	If using external F_IN, V_IN and H_IN signals, this parameter must be set following the completion of programming the F_IN, V_IN and H_IN offsets.	0

6. CLOSED CAPTIONING

The GF9331 provides a blanking function for selected input video lines. Consecutive lines within each input field are blanked, when this function is enabled, beginning with the CC_BLANK_START_LINE and ending with the CC_BLANK_END_LINE. The blanking is applied prior to any processing of the video data.

The blanking function is enabled with the CC_BLANK_EN bit. BLANK_START_LINE and BLANK_END_LINE are each allocated 8-bits within the host interface.

7. RESET

The RESET pin is an active low pin which will reset all internal logic to it's default conditions when set low. On power up we recommend resetting the device to ensure all internal registers are set to their default state. When applying a reset, the GF9331 will load in the STD[4:0] and MODE[2:0] settings from the external pins. If no further configuration is done, these settings will be used for the operation of the device.

8. MODES OF OPERATION

The device supports enabled and disabled modes of operation. The basic operating mode for the GF9331 is selected using the MODE control bit or the MODE register within the host interface. See Table 6.

8.1 Motion Processing Mode (MODE=1)

When set to operate as a motion co-processor the GF9331 performs vertical motion detection, edge direction determination and provides control of the GF9330 filters through the FIL_SEL[3:0] bus on a pixel by pixel basis.

8.2 Disabled Mode (MODE=0)

The GF9331 may also be set to disabled mode of operation. In the disabled mode, no motion co-processing operations are performed and the FIL_SEL[3:0} output bus is set to “0000”. In this mode, the input video is still routed to the Y_OUT and C_OUT pins of the GF9330 (Note: Only the active portion of the input video signal is passed through the device to the GF9330, all other data will be lost from the input data stream). See Table 6.

TABLE 6: Modes of Operation

MODE	DESCRIPTION
0	Disabled
1	Motion processing of input video signal

9. PROCESSING OF INPUT FORMATS

The GF9331 provides motion processing for the formats identified in Table 7.

TABLE 7: Processing of Input Formats

STD[4:0]	INPUT FORMAT	MOTION PROCESSING MODE	DISABLED MODE
00000	525i (30/1.001) SMPTE 125M	Supported	Supported
00001	Reserved	NA	NA
00010	525i (30/1.001) SMPTE 267M - 16x9	Supported	Supported
00011	Reserved	NA	NA
00100	625i (25) EBU Tech 3267	Supported	Supported
00101	Reserved	NA	NA
00110	625i (25) 16 x9 ITU-R BT.601 Part B	Supported	Supported
00111	Reserved	NA	NA
01000	525p (60/1.001) SMPTE 293M	NA	Supported
01001	Reserved	NA	NA
01010	Reserved	NA	NA
01011	Reserved	NA	NA
01100	625p (50) ITU-R BT-1358	NA	Supported
01101	625p (50) 16x9	NA	Supported
01110	Generic SD 4:1:1	Supported	Supported
01111	Generic SD 4:2:2	Supported	Supported
10000	720p (60 & 60/1.001) SMPTE 296M Jan '99 Draft (System #1 and #2)	NA	Supported
10001	720p (30 & 30/1.001) SMPTE 296M Jan '99 Draft (System #4 and #5)	NA	Supported
10010	1080p (30 & 30/1.001) SMPTE 274M (System #7 and #8)	NA	Supported
10011	720p (50) SMPTE 296M Jan '99 Draft (System #3)	NA	Supported
10100	1080p (25) SMPTE 274M (System #9)	NA	Supported

TABLE 7: Processing of Input Formats (Continued)

STD[4:0]	INPUT FORMAT	MOTION PROCESSING MODE	DISABLED MODE
10101	720p (25) SMPTE 296M Jan '99 Draft (System #6)	NA	Supported
10110	1080p (24 & 24/1.001) SMPTE 274M (System #10 and #11)	NA	Supported
10111	720p (24 & 24/1.001) SMPTE 296M Jan '99 Draft (System #7 and #8)	NA	Supported
11000	1080i (30 & 30/1.001) SMPTE 274M (System #4 and #5)	Supported	Supported
11001	1080PsF (30 & 30/1.001) Draft RP May 99 (System #12 and #13)	NA	Supported
11010	1080i (25) SMPTE 274M (System #6)	Supported	Supported
11011	1080PsF (25) Draft RP May 99(System #14)	NA	Supported
11100	1080i (25) SMPTE 295M (System #2)	Supported	Supported
11101	1080PsF (24 & 24/1.001) Draft RP May 99 (System #15 & #16)	NA	Supported
11110	1035i (30 & 30/1.001) SMPTE 260M	Supported	Supported
11111	Generic HD 4:2:2	Supported	Supported

10. VERTICAL MOTION DETECTION

The GF9331 detects objects moving in the vertical direction (e.g. edit text in film). By performing motion detection, a special vertical filter may be enabled within the GF9331 for interpolating the pixels with vertical motion, thereby greatly reducing de-interlacing artifacts. This vertical motion detection signal is provided to the GF9330 through the control bus (FIL_SEL[3:0]).

10.1 Vertical Motion Feature Control

The GF9331 is able to operate in automatic or disabled mode for vertical motion detection of the video input stream. When set to operate in disabled mode (VM_MODE=0), the internal vertical motion detection circuitry is disabled. When set to operate in automatic mode (VM_MODE=1) the GF9331 internally detects vertical motion. See Table 8.

TABLE 8: VM_MODE

EXTERNAL VM_MODE PIN	HOST INFTERFACE VM_MODE BIT	DESCRIPTION
0	0	Vertical Motion Detection Disabled
0	1	Vertical Motion Detection Enabled
1	0	
1	1	

11. EDGE DIRECTION DETECTION

In order to reduce the artifacts caused by the de-interlacing process, interpolated pixels are calculated along different edge directions. When the GF9331 is used in conjunction with the GF9330, nine edge directions are analyzed and the appropriate filter for use within the GF9330 is selected using the control bus FIL_SEL[3:0]. Based on several complex techniques including vertical-temporal filtering, and gradient and morphological operations, the GF9331 detects edge directions so that temporal flickers are minimized.

11.1 EDGE DIRECTION DETECTION FEATURE CONTROL

The GF9331 is able to operate in automatic or disabled mode for edge direction detection of the video input stream. When set to operate in disabled mode (ED_MODE=0), the internal edge direction detection circuitry is disabled. When set to operate in automatic mode (ED_MODE=1) the GF9331 internally detects edge directions. See Table 9.

TABLE 9: ED_MODE

EXTERNAL ED_MODE PIN	HOST INTERFACE ED_MODE BIT	DESCRIPTION
0	0	Edge Direction Detection Disabled
0	1	Edge Direction Detection Enabled
1	0	
1	1	

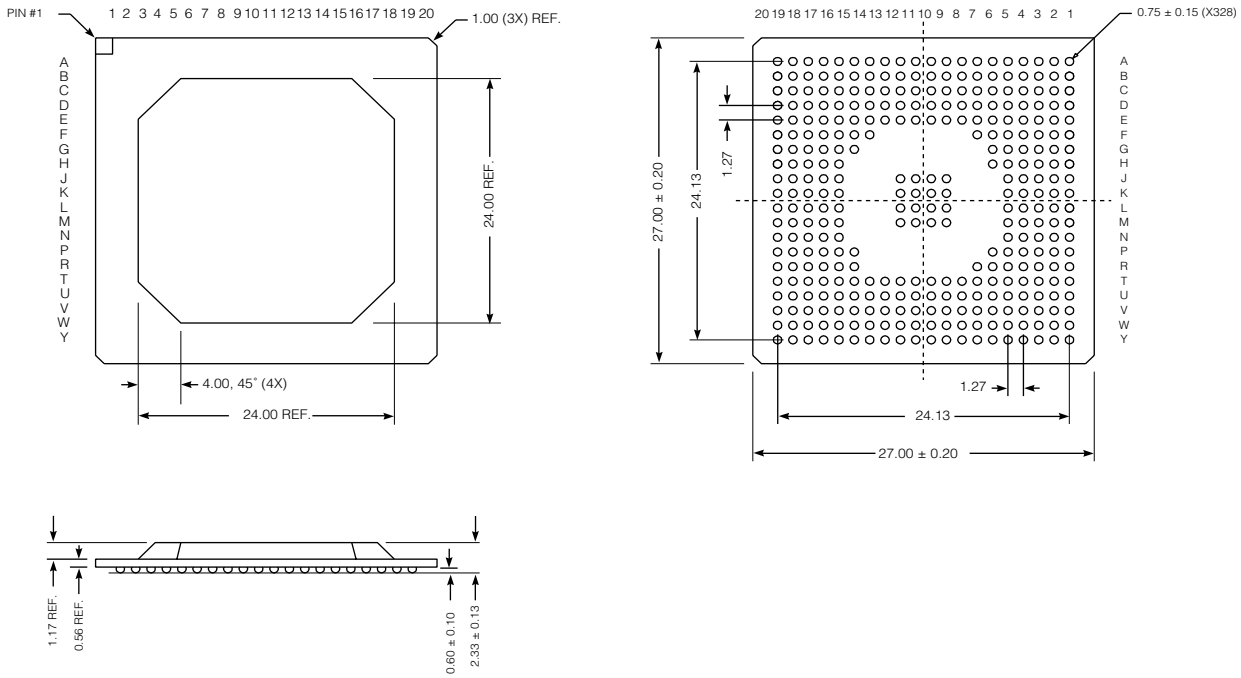
12. VIDEO OUTPUT

The GF9331 supports all input formats defined in Section 1. Routing of video data to the GF9330 is done via the Y_OUT[9:0] and C_OUT[9:0] busses. Note that only the active portion of the input video signal is passed through the device to the GF9330 unchanged. All other ancillary data is discarded from the input data stream.

13. PROCESSING LATENCY

For all modes of operation, the GF9331 video information processing latency is constant at 2 lines, 16 pixels.

PACKAGE DIMENSIONS



DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

REVISION NOTES:
Update to Document information and figures.

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