

GLT41016-10E

64k x 16 Embedded EDO DRAM

FEATURES

- ◆ Logical organization: 64k x 16 bits
- ◆ Physical organization: 256 x 256 x 16
- ◆ Single 3.3V ± 0.3 V power supply
- ◆ 256 cycle refresh in 4 ms
- ◆ Refresh modes: $\overline{\text{RAS}}$ only, CBR, and Hidden
- ◆ Dual $\overline{\text{CAS}}$ for Byte Write and Byte Read control
- ◆ Separate I/O operation
- ◆ 100 MHz page mode EDO cycle
- ◆ 30 ns row access time
- ◆ Redundancy: 2 WL/256K, 2 CS/1M

GENERAL DESCRIPTION

The 1 Mbit Embedded DRAM (EmDRAM) is an asynchronous design with non-multiplexed row and column addressing scheme. The memory operations are controlled by $\overline{\text{RAS}}$, $\overline{\text{CASH}}/\overline{\text{CASL}}$, and $\overline{\text{WE}}$. Byte access is controlled by $\overline{\text{CASH}}$ (upper byte) and $\overline{\text{CASL}}$ (lower byte).

The EmDRAM has been designed to support 200Mbyte data rate with a 30 ns latency when operated in the page mode with extended data output (EDO). this maximum rate can be sustained for one page of 12 bytes.

Performance Data

Parameter	-30
Max. $\overline{\text{RAS}}$ access time, t_{RAC}	30 ns
Max. column address access time, t_{AA}	12 ns
Max. $\overline{\text{CAS}}$ access time, t_{CAC}	8 ns
Min. extended data out page mode cycle time, t_{PC}	10 ns
Min. read/write cycle time, t_{RC}	60 ns

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FUNCTIONAL BLOCK DIAGRAM

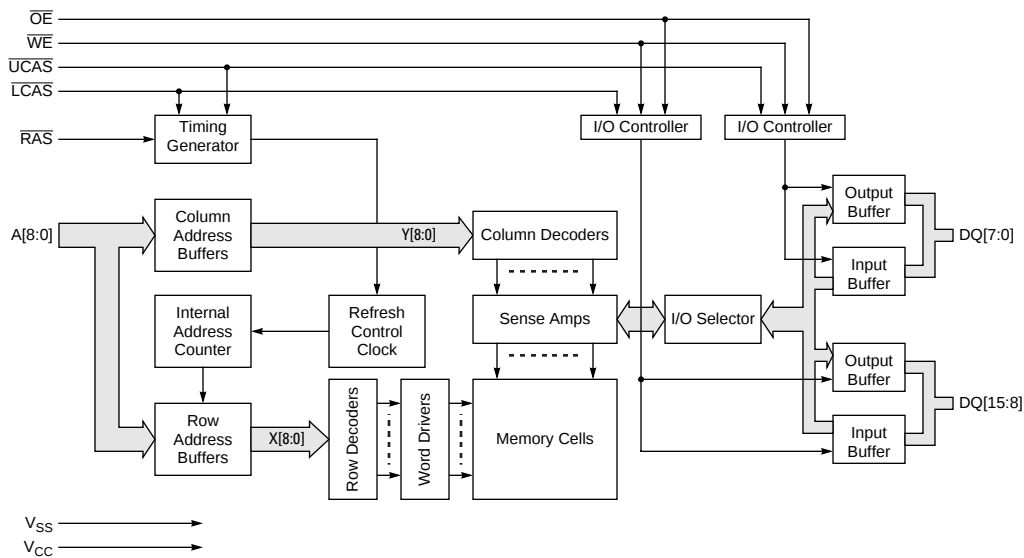


Figure 1. GLT44016 - 256K X 16

Signal Descriptions [1]

Symbol	Type	Description
DI[15:0]	Input	Data in.
DO[15:0]	Output	Data out.
XRA[7:0]	Input	Row address.
XCA[7:0]	Input	Column address.
$\overline{\text{RAS}}$	Input	Row address strobe (active low).
$\overline{\text{CASH}}$	Input	Column address strobe, access DI/DO[15:8] (active low)
$\overline{\text{CASL}}$	Input	Column address strobe, access DI/DO[7:0] (active low)
$\overline{\text{WE}}$	Input	Write enable (active low).
$\overline{\text{OE}}$	Input	Output enable (active low).
V _{DD}	Supply	3.3v voltage supply, 2 pairs double bond minimum
V _{SS}	Supply	Ground (voltage return), 2 pairs double bond minimum

1. On-chip power supply to the EmDRAM should be separated from the Logic portion.

Function Table

Input Pin					DQ Pin		Functional Mode
$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	DQ[7:0]	DQ[15:8]	
H	–	–	–	–	High-Z	High-Z	Standby
L	H	H	–	–	High-Z	High-Z	Refresh
L	L	H	H	L	D _{OUT}	High-Z	Lower Byte Read
L	H	L	H	L	High-Z	Dout	Upper Byte Read
L	L	L	H	L	Dout	Dout	Word Read
L	L	H	L	H	Din	Don't Care	Lower Byte Write
L	H	L	L	H	Don't Care	Din	Upper Byte Write
L	L	L	L	H	Din	Din	Word Write
L	L	L	H	H	High-Z	High Z	–

Truth Table

Function	RAS	CAS	WE	OE	Address	DQM0	DQM1	DQM2	DQM3	DI[31:0]	DO[31:0]
Standby	H	H	X	X	X	X	X	X	X	X	High-Z
Read	L	L	H	L	Row/Col	X	X	X	X	X	Data Out
Write (Early)	L	L	L	X	Row/Col	H	H	H	H	Data In	High-Z
Write DI[7:0]	L	L	L	X	Row/Col	L	H	H	H	Data In	High-Z
Write DI[15:8]	L	L	L	X	Row/Col	H	L	H	H	Data In	High-Z
Write DI[23:16]	L	L	L	X	Row/Col	H	H	L	H	Data In	High-Z
Write DI[31:24]	L	L	L	X	Row/Col	H	H	H	L	Data In	High-Z
Read-Write	L	L	H→L	L→H	Row/Col	H	H	H	H	Data In	Data Out
Page-Mode Read (First Cycle)	L	H→L	H	L	Row/Col	X	X	X	X	X	Data Out
Page-Mode Read (Subsequent Cycles)		H→L	H	L	Col	X	X	X	X	X	Data Out
Page-Mode Write (First Cycle)	L	H→L	L	X	Row/Col	H	H	H	H	Data In	High-Z
Page-Mode Write (Subsequent Cycle)	L	H→L	L	X	Col	H	H	H	H	Data In	High-Z
Page-Mode R-W (First Cycle)	L	H→L	H→L	L→H	Row/Col	H	H	H	H	Data In	Data Out
Page-Mode R-W (Subsequent Cycle)	L	H→L	H→L	L→H	Col	H	H	H	H	Data In	Data Out
CBR Refresh	H→L	L	X	X	X	X	X	X	X	X	High-Z
RAS-only Refresh	L	H	X	X	Row	X	X	X	X	X	High-Z

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ^[1]

Symbol	Parameter	Conditions	Value	Unit
V_T	Voltage on any pin relative to V_{SS}	$T_A = 25^\circ\text{C}$	-0.5 to +4.6	V
I_{OS}	Short circuit output current	$T_A = 25^\circ\text{C}$	50	mA
P_D	Power dissipation	$T_A = 25^\circ\text{C}$	1	W
T_{OPR}	Operating temperature	—	0 to +70	$^\circ\text{C}$
T_{STG}	Storage temperature	—	-55 to +150	$^\circ\text{C}$

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Power supply voltage	3.0	3.3	3.6	V
V_{SS}		0	0	0	V
V_{IH}	Input high voltage	2.4	—	$V_{CC} + 1$	V
V_{IL}	Input low voltage	-1.0	—	0.8	V

Capacitance ($V_{CC} = 5V \pm 10\%$, $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN1}	Input capacitance (A[8:0])	—		1	pF
C_{IN2}	Input capacitance ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{WE}$, $\overline{OE}$)	—		1	pF
$C_{I/O}$	Input/Output capacitance (DQ[15:0])	—		1	pF

DC Characteristics ($V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

Symbol	Parameter	Condition	-30		Units	Note
			Min	Max		
V_{OH}	Output High Voltage	$I_{OH} = -2\text{ mA}$	2.4	V_{CC}	V	
V_{OL}	Output Low Voltage	$I_{OL} = -1.0\text{ mA}$	0	0.4	V	
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	-2	-2	μA	
I_{LO}	Output Leakage Current	DQi Disable $0V \leq V_O \leq 3.6V$	-10	-10	μA	
I_{CC1}	Average Power Supply Current (Operating)	$\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = \text{Min.}$		200	mA	[1] [2]
I_{CC2}	Power Supply Current (Standby)	$\overline{RAS}$, $\overline{CAS} = V_{IH}$			mA	[1]
I_{CC3}	Average Power Supply Current (RAS-only Refresh)	$\overline{RAS}$ -Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = \text{Min.}$		200	mA	[1] [2]
I_{CC4}	Average Power Supply Current (Fast Page Mode)	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling, $t_{HCP} = \text{Min.}$		140	mA	[1] [3]
I_{CC5}	Average Power Supply Current ($\overline{CAS}$ -before- $\overline{RAS}$ Refresh)	$\overline{RAS}$ Cycling, $\overline{CAS}$ -before- $\overline{RAS}$		200	mA	

1. I_{CC} Max. is specified for I_{CC} for the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while $\overline{CAS} = V_{IH}$.

AC Characteristics ($V_{CC} = 3.3\text{ V} \pm 10\%$, $T_A = 0\text{ }^{\circ}\text{C} - 70\text{ }^{\circ}\text{C}$, $C_L = 1\text{ pF}$)

Symbol	Description	Min	Max	Units	Notes
t_{RC}	Random Read/Write cycle time	60	—	ns	
t_{PC}	Page Mode Read/Write cycle	10	—	ns	[1] [2]
t_{OFF}	Read Data valid from $\overline{RAS}$ high	0	—	ns	[3]
t_{DOH}	Read Data valid from next $\overline{CAS}$ low	3	—	ns	[4]
t_{AA}	Access time from Column Address	—	12	ns	
t_{RAC}	Access time from $\overline{RAS}$ low	—	30	ns	
t_{CAC}	Access time from $\overline{CAS}$ low	—	8	ns	[2]
t_{CPA}	Access time from $\overline{CAS}$ precharge	—	14	ns	[3]
t_{RAS}	$\overline{RAS}$ pulse width	30	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay time	15	35	ns	
t_{CSH}	$\overline{CAS}$ hold time for $\overline{RAS}$	30	—	ns	[5]
t_{CAS}	$\overline{CAS}$ pulse width	4	—	ns	[6]
t_{ASR}	Row Address setup time	3	—	ns	
t_{RAH}	Row Address hold time	3	—	ns	
t_{ASC}	Column Address setup time	3	—	ns	[4]
t_{CAH}	Column Address hold time	3	—	ns	[2]
t_{CP}	$\overline{CAS}$ precharge time	4	—	ns	[7]
t_{DS}	Write Data setup time	3	—	ns	[4]
t_{DH}	Write Data hold time	3	—	ns	[2]
t_{RP}	$\overline{RAS}$ precharge time	20	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ precharge time	15	—	ns	[3]
t_{RSH}	$\overline{CAS}$ low to $\overline{RAS}$ high hold time	10	—	ns	[2]
t_{RCS}	Read command setup time	0	—	ns	[4]
t_{RCH}	Read command hold time from $\overline{CAS}$ high	0	—	ns	[3]
t_{RRH}	Read command hold time from $\overline{RAS}$ high	0	—	ns	
t_{WCS}	Write command setup time	5	—	ns	
t_{WCH}	Write command hold time	5	—	ns	
t_{WP}	$\overline{WE}$ pulse width	8	—	ns	
t_T	Transition time (rise and fall)	—	1.5	ns	
t_{RWL}	Write command to $\overline{RAS}$ high	8	—	ns	
t_{CWL}	Write command to $\overline{CAS}$ high	8	—	ns	[5]

1. Maximum $\overline{CAS}$ to $\overline{CAS}$ skew is 1 ns.
2. Last $\overline{CASx}$ LOW.
3. Last $\overline{CASx}$ HIGH.
4. First $\overline{CASx}$ LOW.
5. First $\overline{CASx}$ HIGH.
6. Last $\overline{CASx}$ LOW to first $\overline{CASx}$ HIGH.
7. Last $\overline{CASx}$ HIGH to first $\overline{CASx}$ LOW.

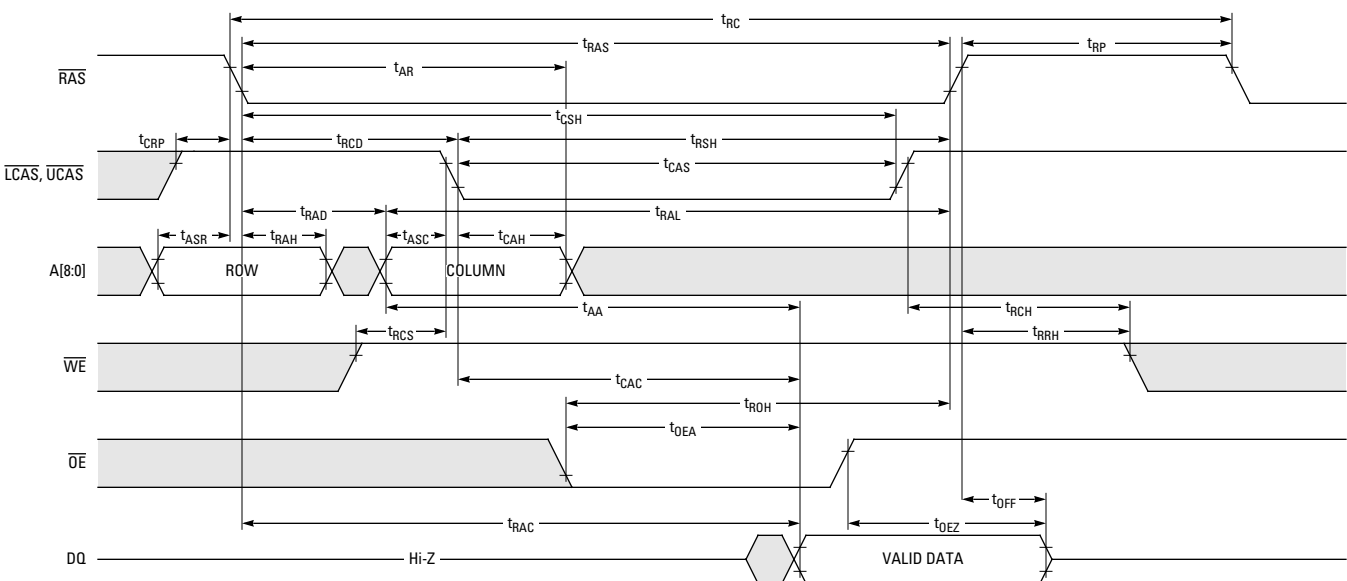


Figure 2. Read Cycle ($\overline{\text{RAS}}$ Output Control)

□ Don't Care

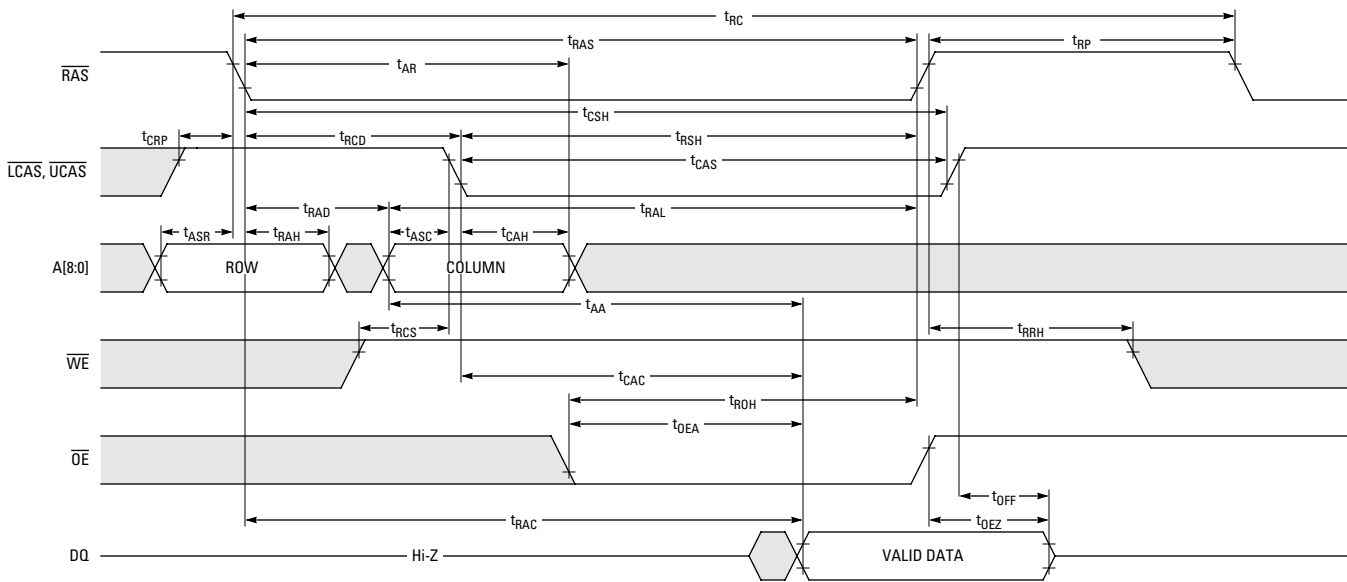


Figure 3. Read Cycle ($\overline{\text{CAS}}$ Output Control)

□ Don't Care

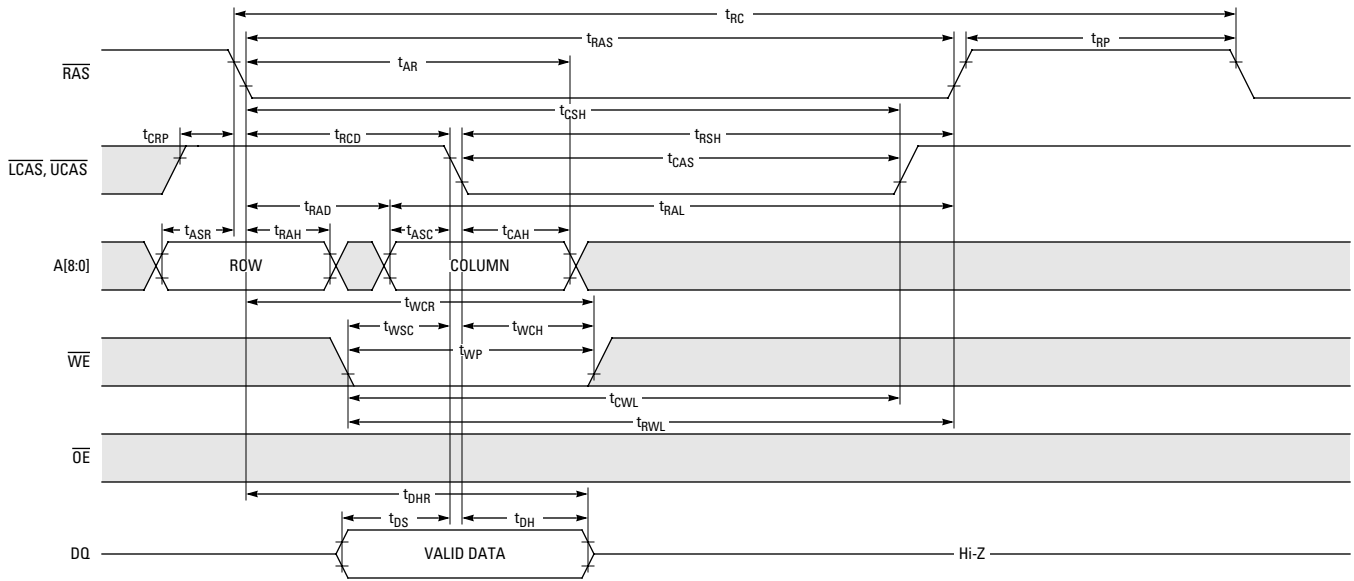


Figure 4. Early Write ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)

□ Don't Care

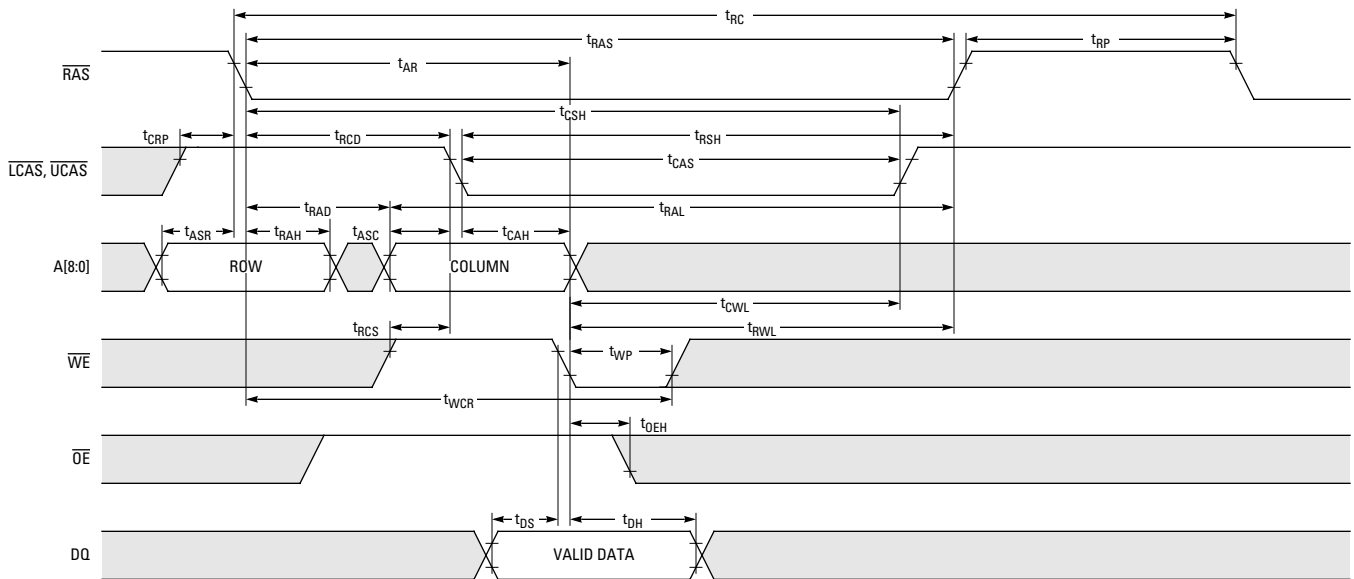


Figure 5. Late Write ($\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ Active)

□ Don't Care

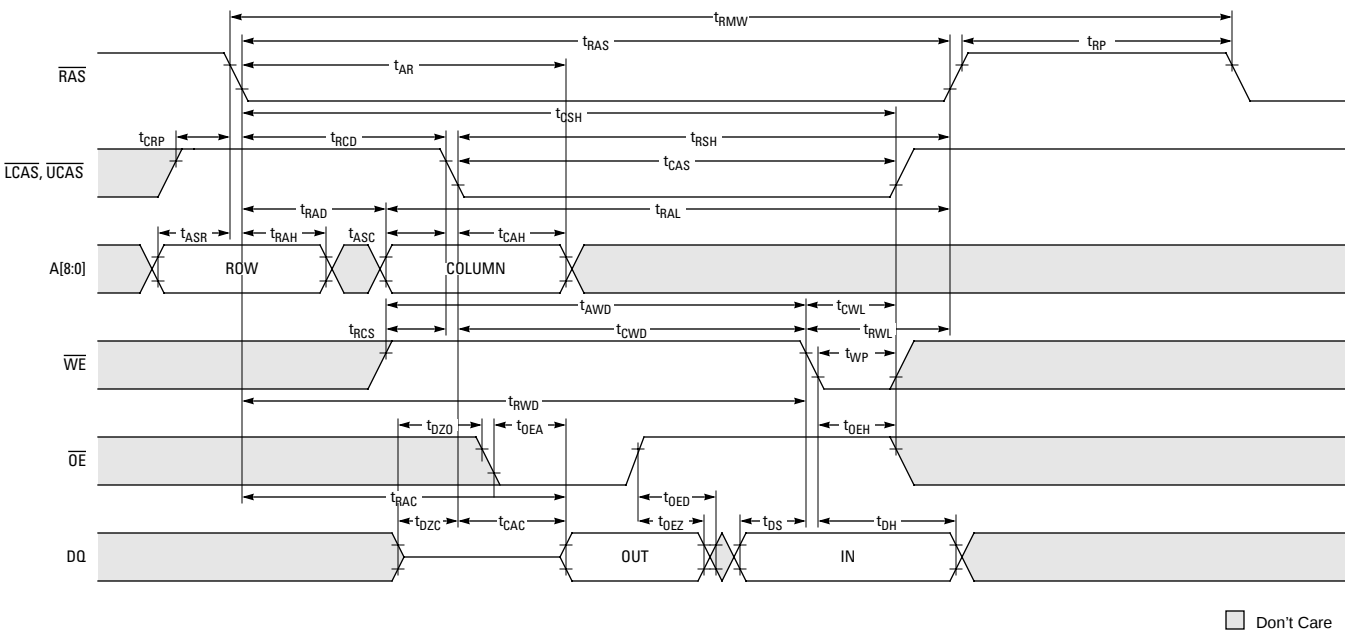


Figure 6. Read Modify Write Cycle (LCAS and UCAS Active)

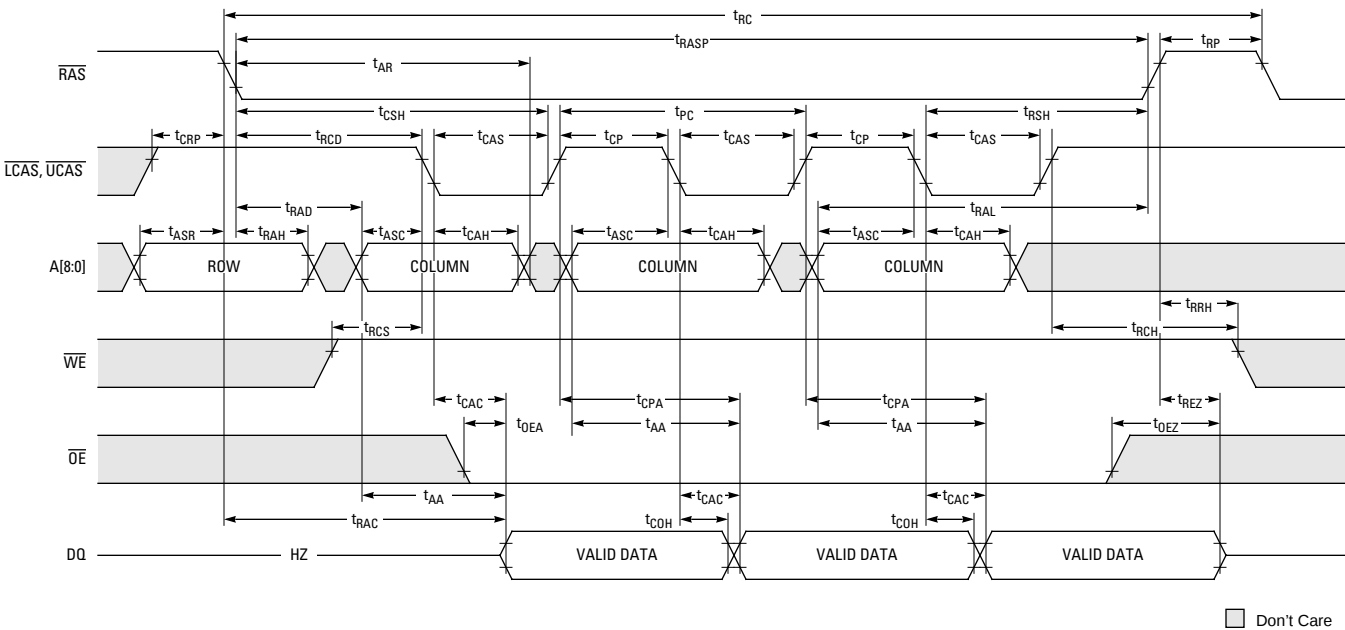


Figure 7. Fast Page Mode Read Cycle with Extended Data Out

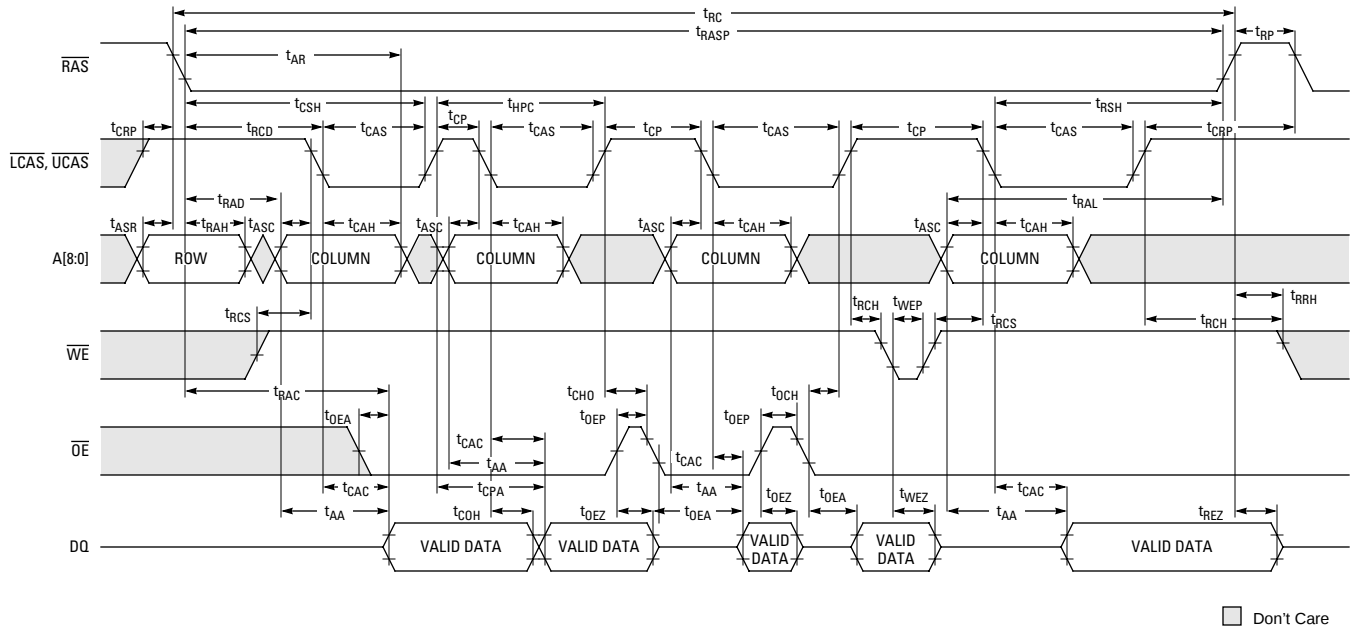


Figure 8. Fast Page Mode Read Hi-Z Operation

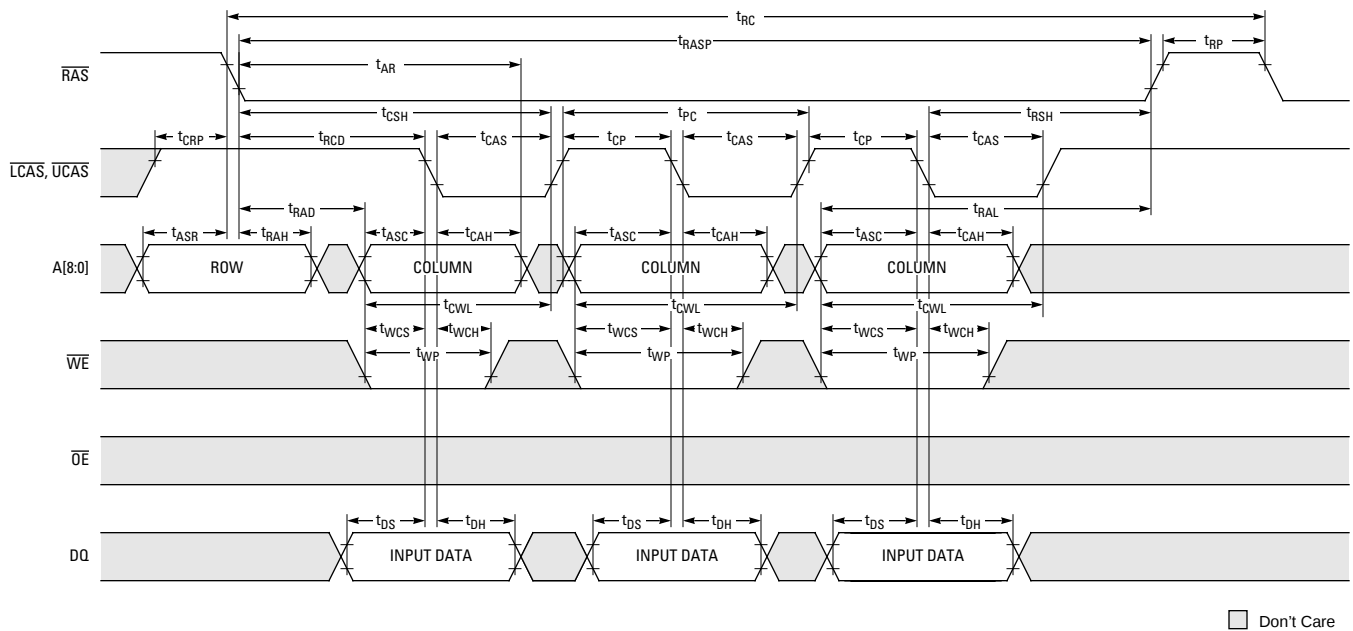


Figure 9. Fast Page Mode Early Write Cycle

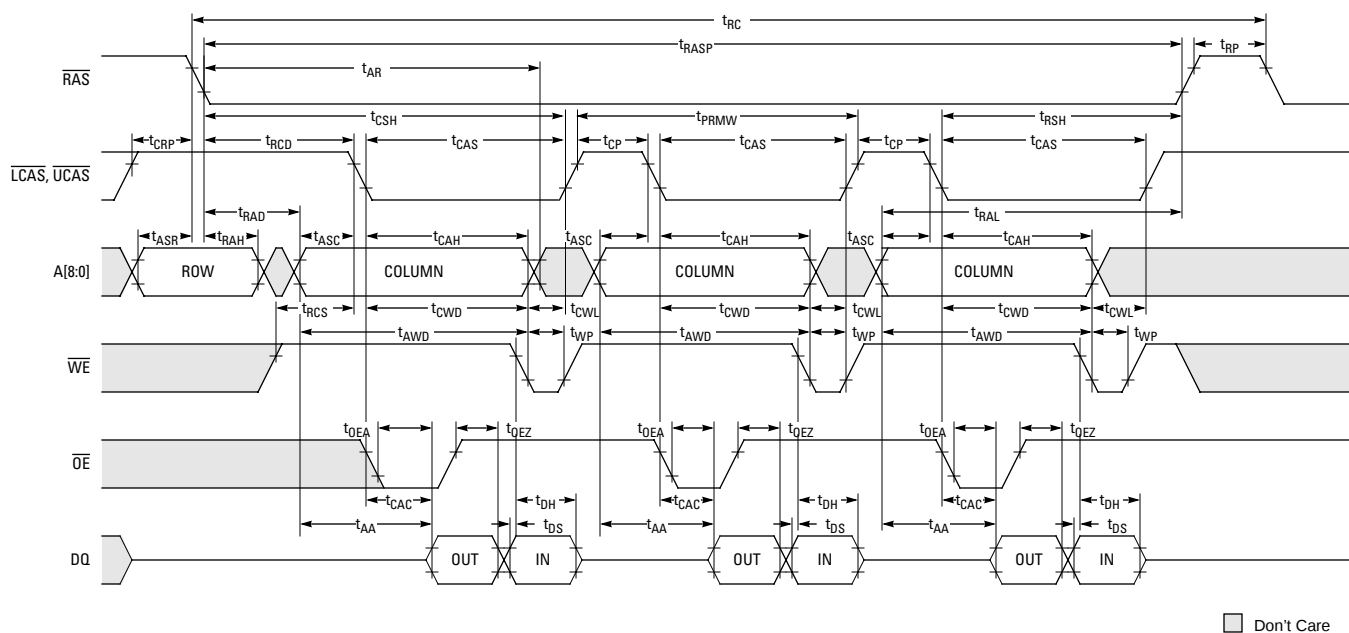


Figure 10. Fast Page Mode Read Modify Write Cycle

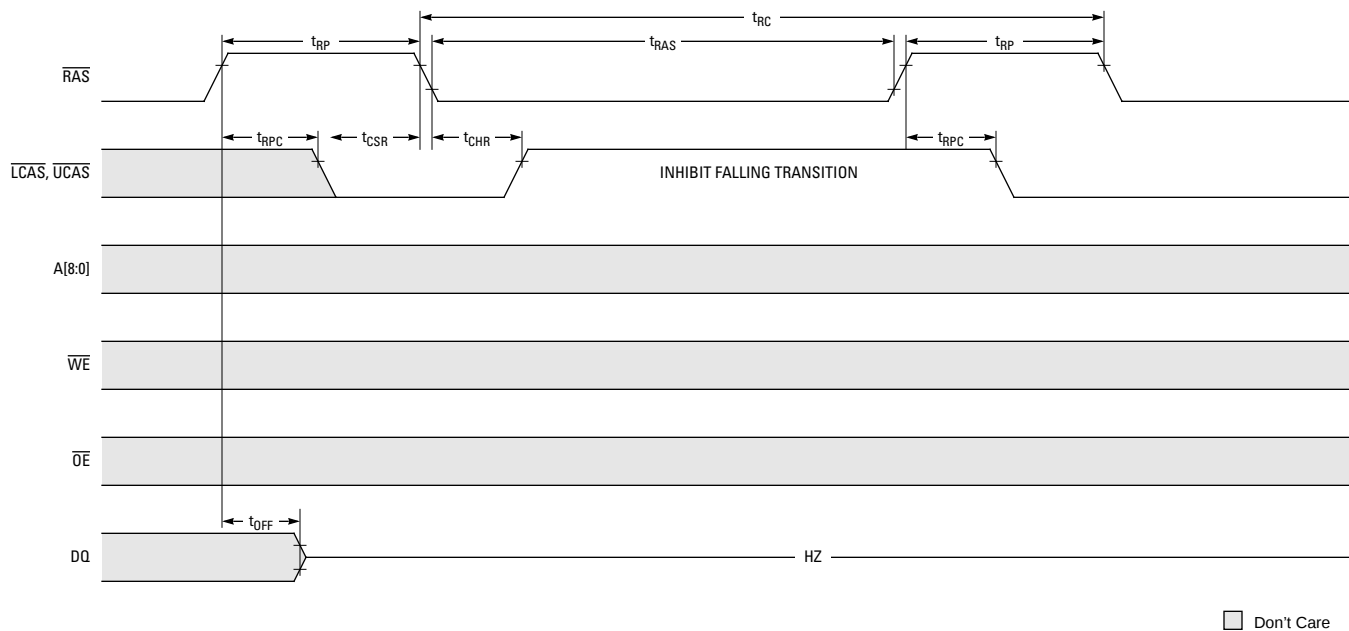


Figure 11. $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle

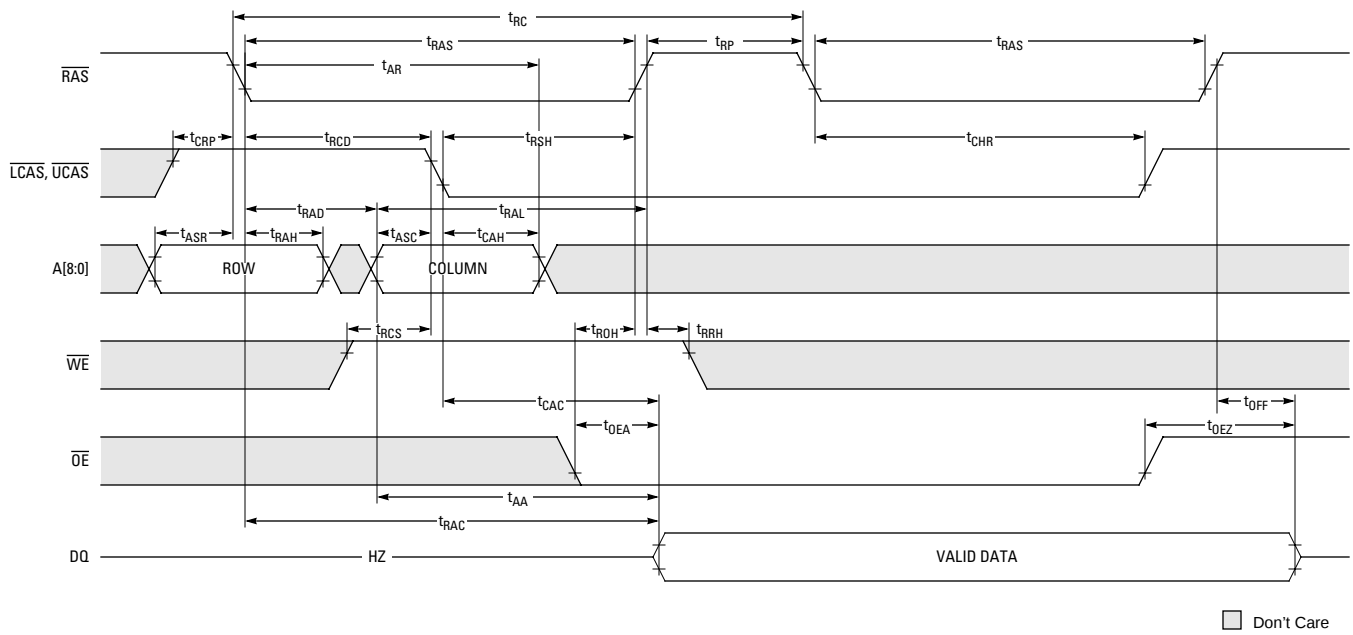


Figure 12. Hidden Refresh Cycle

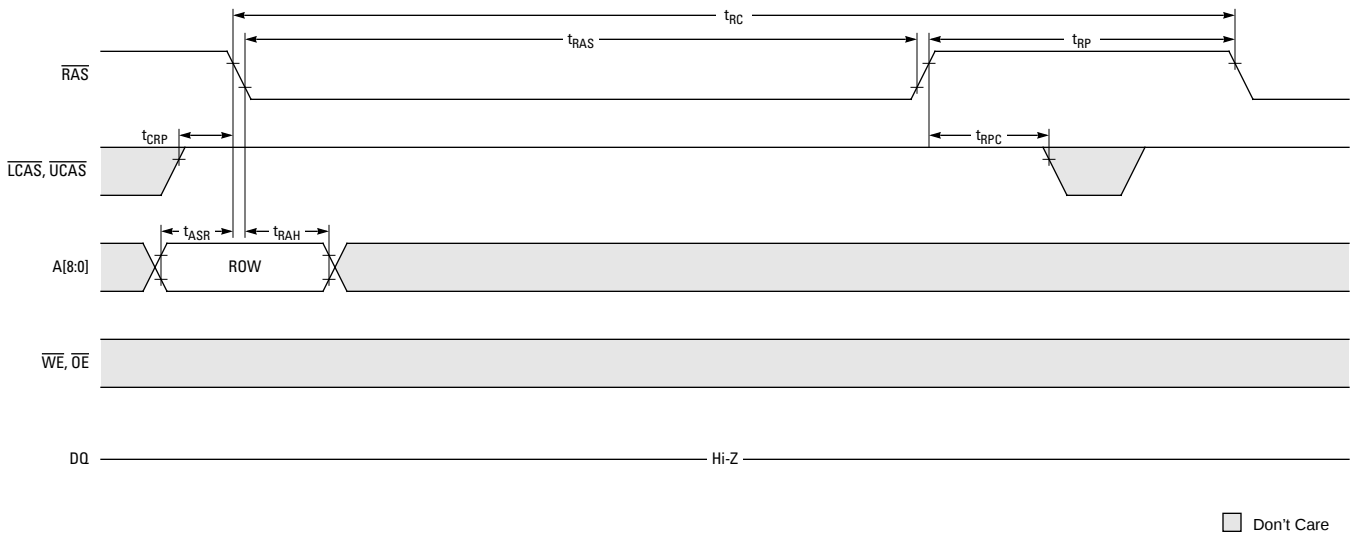


Figure 13. $\overline{\text{RAS}}$ -Only Refresh Cycle



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