

Features :

- * Low-power consumption.
 -active: 45mA I_{cc} at 85ns.
 -stand by :
 20 μ A (CMOS input / output , LL)
 5 μ A (CMOS input / output, SL)
- * Single +2.7V to 3.6V power supply.
- * Equal access and cycle time.
- * 70ns/85ns access time
- * Tri-state output.
- * Automatic power-down when deselected.
- * Multiple center power and ground pins for improved noise immunity.
- * Individual byte controls for both read and write cycles.
- * Industrial grade (-40°C ~ 85°C) available.
- * Available in 48-fpBGA/44L TSOPII.
- * CE2 pin available for fpBGA only.

Description :

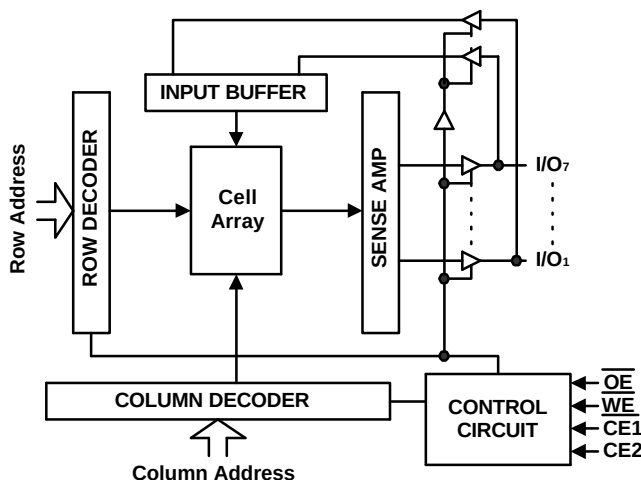
The GLT6400L16 is a low power CMOS Static RAM organized as 262,144 words by 16 bits. Easy memory expansion is provided by an active LOW $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ pin and active HIGH CE2.

This device has an automatic power – down mode feature when deselected. Separate Byte Enable controls ($\overline{\text{BLE}}$ and $\overline{\text{BHE}}$) allow individual bytes to be accessed. $\overline{\text{BLE}}$ controls the lower bits I/O0 – I/O7. $\overline{\text{BHE}}$ controls the upper bits I/O8 – I/O15.

Writing to these devices is performed by taking Chip Enable $\overline{\text{CE1}}$ with Write Enable $\overline{\text{WE}}$ and byte Enable ($\overline{\text{BLE}}$ / $\overline{\text{BHE}}$) Low while CE2 remains HIGH.

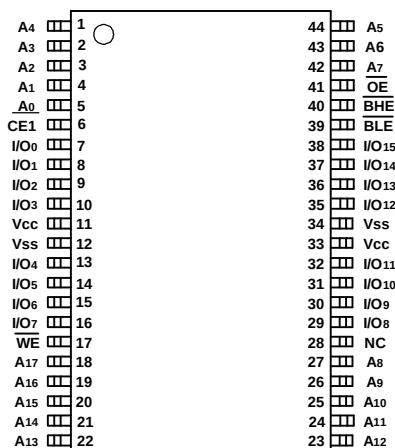
Reading from the device is performed by taking Chip Enable $\overline{\text{CE1}}$ with Output enable $\overline{\text{OE}}$ and byte Enable ($\overline{\text{BLE}}$ / $\overline{\text{BHE}}$) Low while Write Enable $\overline{\text{WE}}$ and CE2 are held HIGH.

Function Block Diagram :

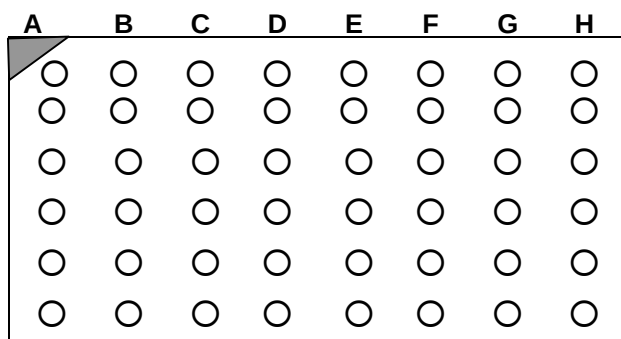


Pin Configurations :

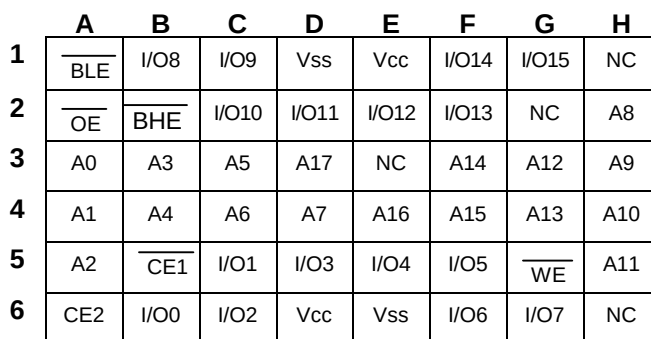
GLT6400L16



48 Ball fpBGA :



(Bottom View)



(Bottom View)

Note : NC means no Ball.

Pin Descriptions:

Name	Function
A ₀ – A ₁₇	Address Inputs
CE ₁ and CE ₂	Chip Enable Input
OE	Output Enable Input
WE	Write Enable Input
I/O ₀ – I/O ₁₅	Data Input and Data Output
V _{CC}	Power Supply
BLE	Lower Byte Enable Input (I/O ₀ to I/O ₇)
BHE	Higher Byte Enable Input (I/O ₈ to I/O ₁₅)
GND	Ground
NC	No Connection

Truth Table:

CE1	CE2	OE	WE	BLE	BHE	I/O0-I/O7	I/O8-I/O15	Power	Mode
H	X	X	X	X	X	High-Z	High-Z	Standby	Deselected
X	L	X	X	X	X	High-Z	High-Z	Standby	Deselected
X	X	X	X	H	H	High-Z	High-Z	Standby	Deselected
L	H	H	H	L	X	High-Z	High-Z	Active	Output Disabled
L	H	H	H	X	L	High-Z	High-Z	Active	Output Disabled
L	H	L	H	L	H	Data Out	High-Z	Active	Lower Byte Read
L	H	L	H	H	L	High-Z	Data Out	Active	Upper Byte Read
L	H	L	H	L	L	Data Out	Data Out	Active	Word Read
L	H	X	L	L	H	Data In	High-Z	Active	Lower Byte Write
L	H	X	L	H	L	High-Z	Data In	Active	Upper Byte Write
L	H	X	L	L	L	Data In	Data In	Active	Word Write

Note ; X means don care. (Must be low or high state).

Absolute Maximum Ratings*

Parameter	Symbol	Minimum	Maximum	Unit
Voltage on Any Pin Relative to Gnd	Vt	-0.5	Vcc + 0.3	V
Power Dissipation	P _T	-	1.0	W
Storage Temperature (Plastic)	Tstg	-55	+150	°C
Temperature Under Bias	Tbias	-25	+85	°C

*Note : Stresses greater than those listed above Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions (TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	2.7	3	3.6	V
	Gnd	0.0	0.0	0.0	V
Input Voltage	V _{IH}	2.2	-	V _{CC} +0.2	V
	V _{IL}	-0.5*	-	0.6	V

* V_{IL} min = -2.0V for pulse width less than t_{RC}/2.

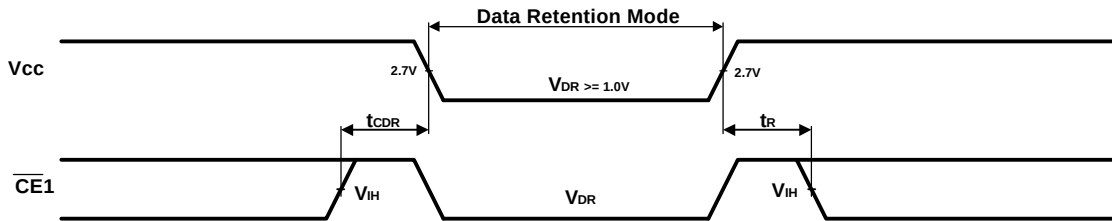
DC Operating Characteristics ($V_{CC} = 2.7V$ to $3.6V$, $T_A = -0^{\circ}C$ to $70^{\circ}C$)

Parameter	Sym.	Test Conditions	70		85		Unit
			Min	Max	Min	Max	
Input Leakage Current	$ I_{LI} $	$V_{CC} = \text{Max},$ $V_{in} = \text{Gnd to } V_{CC}$		1		1	μA
Output Leakage Current	$ I_{LO} $	$\overline{CE}_1 = V_{IH}$ or $CE2 = V_{IH}$ $V_{CC} = \text{Max}, V_{OUT} = \text{Gnd to } V_{CC}$		1		1	μA
Operating Power Supply Current	I_{CC}	$\overline{CE}_1 = V_{IL}, CE2 = V_{IH}$ $V_{IN} = V_{IH}$ or $V_{IL}, I_{OUT} = 0mA$		5		5	mA
Average Operating Current	I_{CC1}	$\overline{CE}_1 = V_{IL}, CE2 = V_{IH}$ $I_{OUT} = 0mA,$ Min Cycle, 100% Duty		50		45	mA
	I_{CC2}	$\overline{CE}_1 = 0.2V$ $CE2 = V_{CC} - 0.2V$ $I_{OUT} = 0mA,$ Cycle Time=1 μs , 100% Duty		5		5	mA
Standby Power Supply Current(TTL Level)	I_{SB}	$\overline{CE}_1 = V_{IH}$ or $CE2 = V_{IL}$		0.3		0.3	mA
Standby Power Supply Current (CMOS Level)	I_{SB1}	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V, f=0$	GLT6400L16LL	20		20	μA
		$V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	GLT6400L16SL	5		5	μA
Output Low Voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$		0.4		0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4		2.4		V

Data Retention

Parameter	Sym.	Test Conditions	Min.	Max.	Unit
V_{CC} for Data retention	V_{DR}	$\overline{CE}_1 \geq V_{CC} - 0.2V$	1.0	-	V
Data Retention Current	I_{CCDR}	$CE2 \leq +0.2V$	-	4	μA
Chip Deselect to Data Retention Time	t_{CDR}	$V_{IN} \geq V_{CC} - 0.2V$ or	0	-	ns
Operating Recovery Time ⁽²⁾	t_R	$V_{IN} \leq 0.2V$	t_{RC}	-	ns

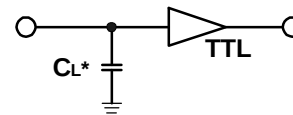
Data Retention Waveform ($T_A = 0^\circ\text{C}$ to 70°C)



AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Level	1.4V

AC Test Loads and Waveforms



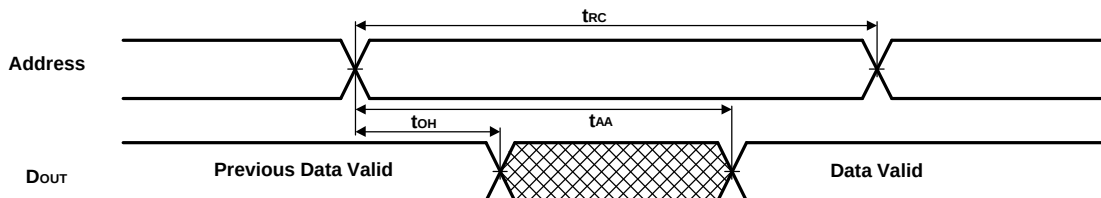
Output Load Condition
 $C_L = 30\text{pf} + 1\text{TTL Load}$

*Including Scope and Jig Capacitance

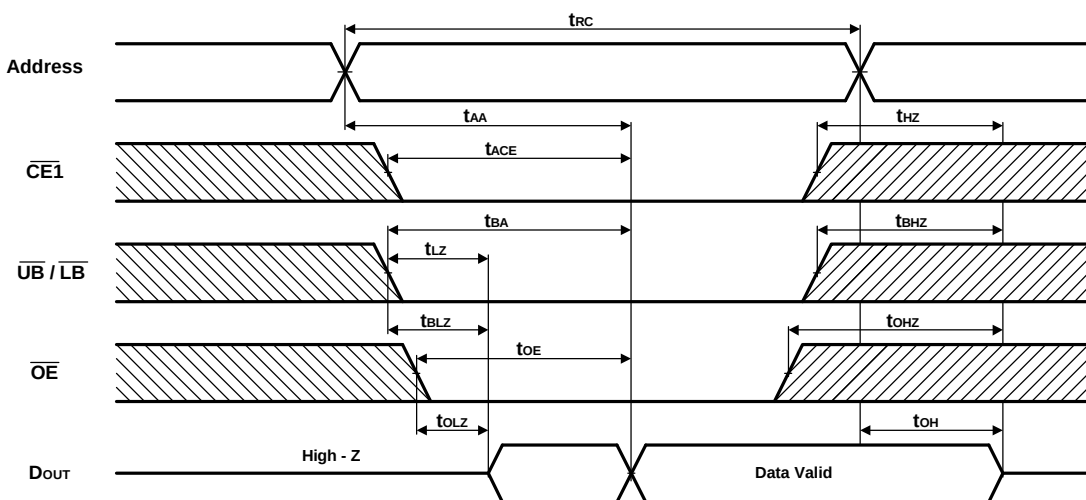
Read Cycle ⁽⁹⁾ ($V_{CC} = 2.7\text{V}$ to 3.6V , $T_A = 0^\circ\text{C}$ to 70°C)

Parameter	Symbol	70		85		Unit	Note
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	70		85		ns	
Address Access Time	t_{AA}		70		85	ns	
Chip Enable Access Time	t_{ACE}		70		85	ns	
Output Enable Access Time	t_{OE}		40		40	ns	
Output Hold from address Change	t_{OH}	10		10		ns	
Chip Enable to Output in Low-Z	t_{LZ}	10		10		ns	4,5
Chip Disable to Output in High-Z	t_{HZ}		25		35	ns	3,4,5
Output Enable to Output in Low-Z	t_{OLZ}	5		5		ns	
Output Disable to Output in High-Z	t_{OHZ}		25		30	ns	
$\overline{BLE}$, $\overline{BHE}$ Enable to Output in Low-Z	t_{BLZ}	5		5		ns	4,5
$\overline{BLE}$, $\overline{BHE}$ Disable to Output in High-Z	t_{BHZ}		25		30	ns	3,4,5
$\overline{BLE}$, $\overline{BHE}$ Access Time	t_{BA}		40		40	ns	

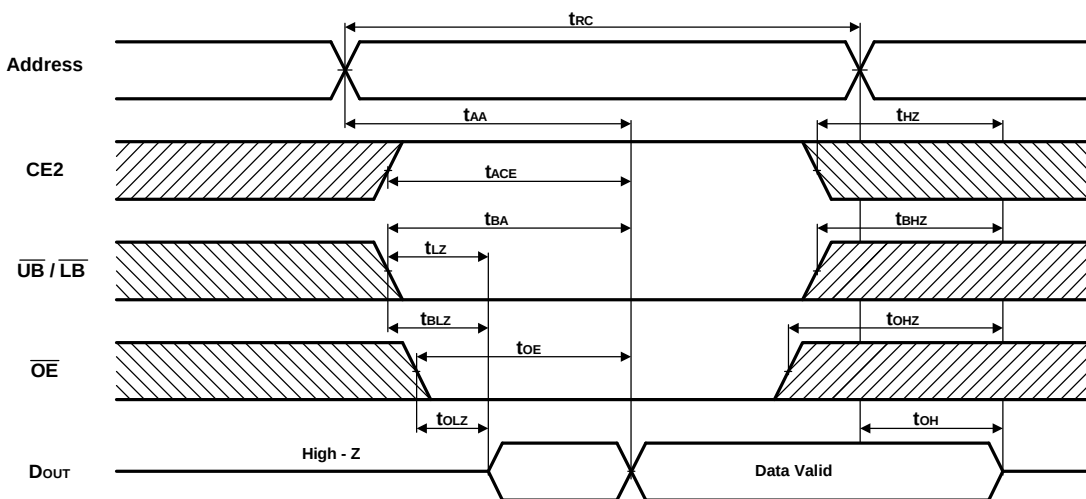
Timing Waveform of Read Cycle 1 (Address Controlled)



Timing Waveform of Read Cycle 2 ^(3~5)



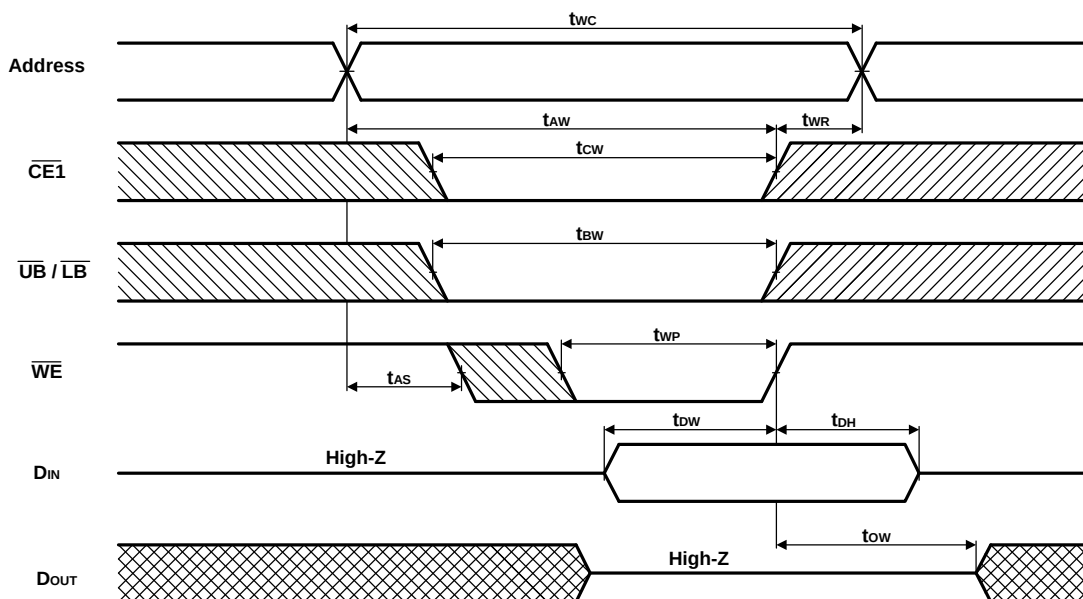
Timing Waveform of Read Cycle 3 ^(3~5)



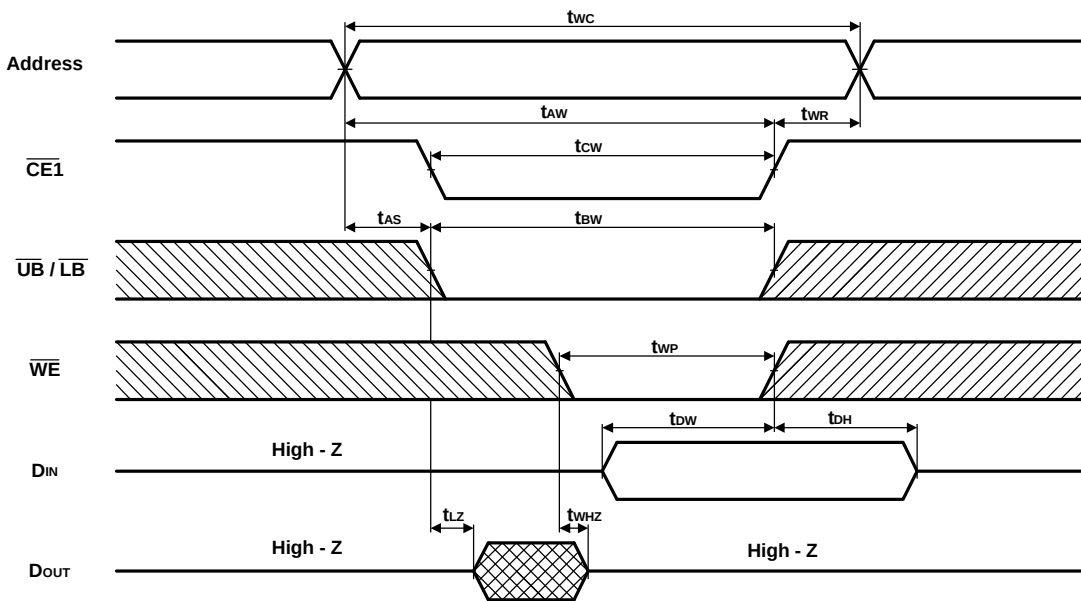
Write Cycle ⁽¹¹⁾ ($V_{CC} = 2.7V$ to $3.6V$, $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	70		85		Unit	Note
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	70		85		ns	
Chip Enable to Write End	t_{CW}	60		70		ns	
Address Setup to Write End	t_{AW}	60		70		ns	
Address Setup Time	t_{AS}	0		0		ns	
Write Pulse Width	t_{WP}	50		60		ns	
Write Recovery Time	t_{WR}	0		0		ns	
Data Valid to Write End	t_{DW}	30		35		ns	
Data Hold Time	t_{DH}	0		0		ns	
Write Enable to Output in High-Z	t_{WHZ}		25		35	ns	
Output Active from Write End	t_{OW}	5		5		ns	
$\overline{BLE}$, $\overline{BHE}$ Setup to Write End	t_{BW}	65		70		ns	

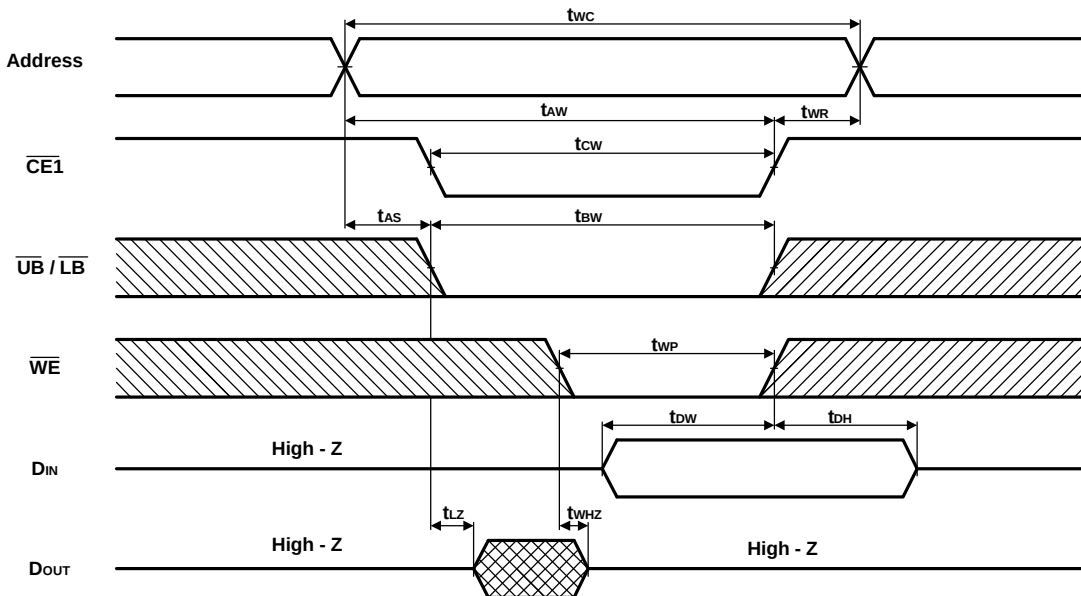
Timing Waveform of Write Cycle 1 (Address Controlled) ^(2~6,8)



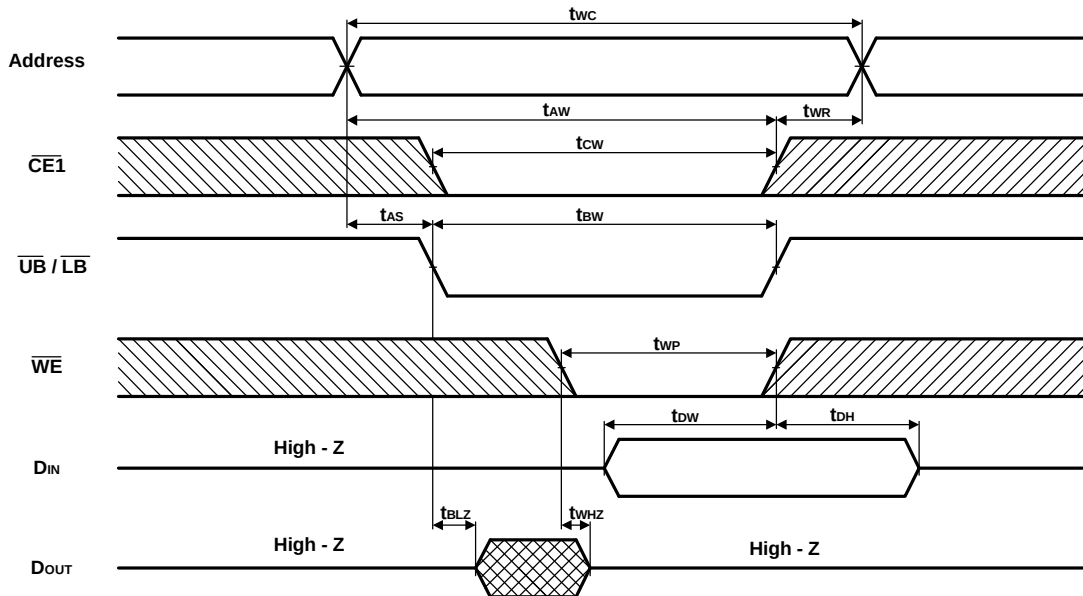
Timing Waveform of Write Cycle 2 ($\overline{\text{CE1}}$ Controlled)^(2-6,8)



Timing Waveform of Write Cycle 3 (CE2 Controlled)^(2-6,8)



Timing Waveform of Write Cycle 4 ($\overline{UB}$ / $\overline{LB}$ Controlled)^(2~6,8)

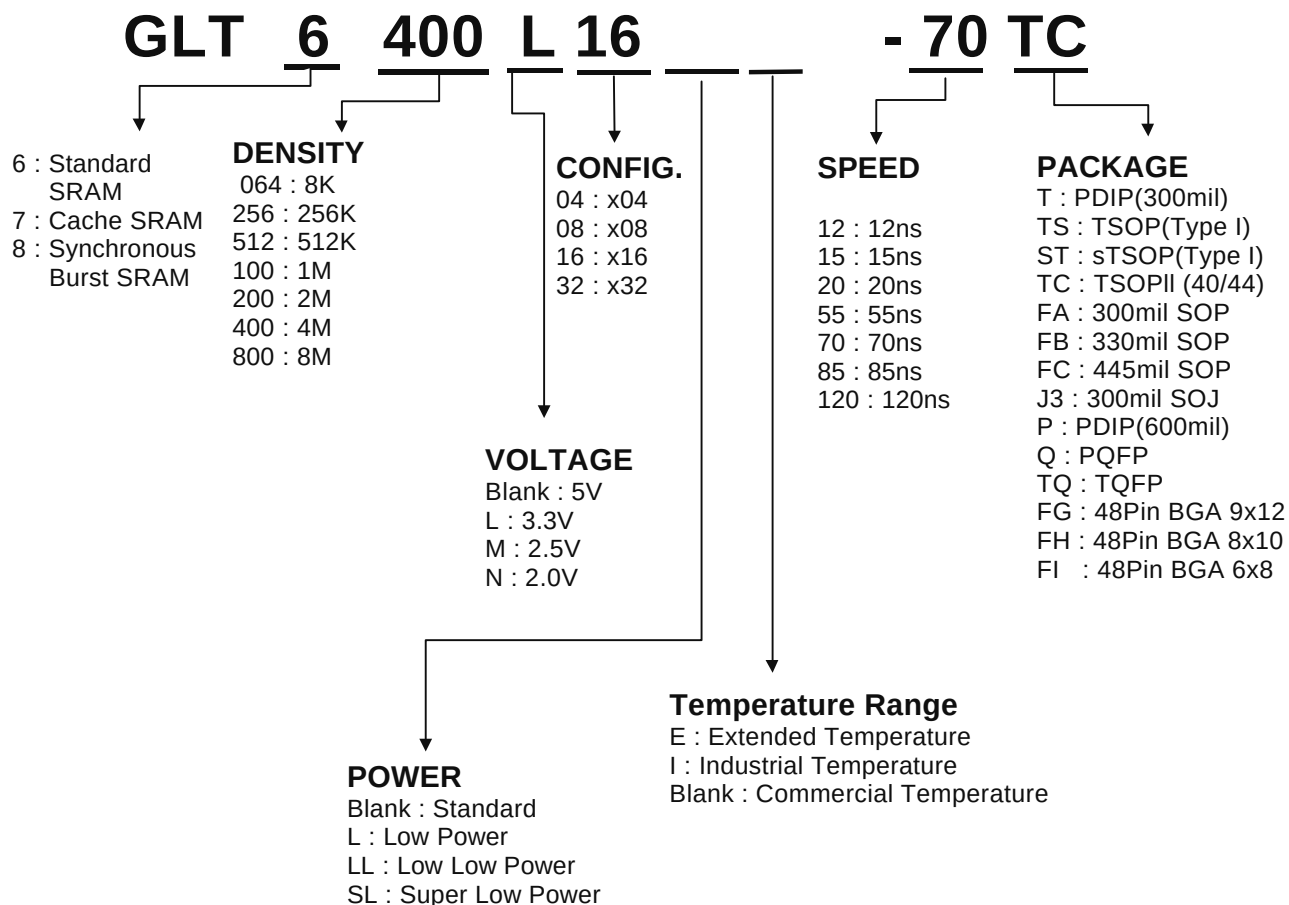


Notes :

1. L-version includes this feature.
2. This Parameter is samples and not 100% tested.
3. For test conditions, see AC Test Condition.
4. This parameter is tested with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady – state voltage.
5. This parameter is guaranteed, but is not tested.
6. $\overline{\text{WE}}$ is HIGH for read cycle.
7. $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ are LOW and CE2 is HIGH for read cycle.
8. Address valid prior to or coincident with $\overline{\text{CE1}}$ transition LOW or CE2 transition HIGH.
9. All read cycle timings are referenced from the last valid address to the first transition address.
10. $\overline{\text{CE1}}$ or $\overline{\text{WE}}$ must be HIGH or CE2 must be LOW during address transition.
11. All write cycle timings are referenced from the last valid address to the first transition address.

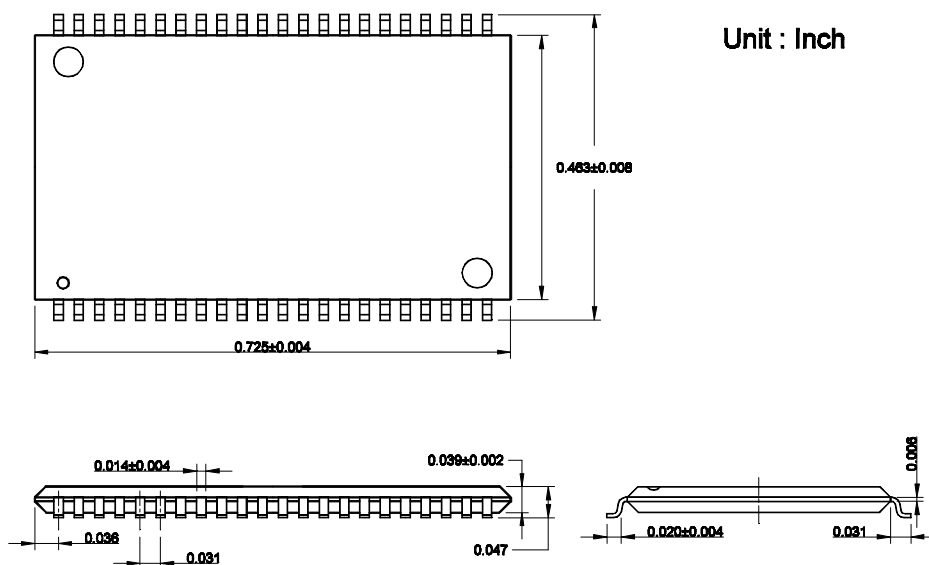
Ordering Information

Part Number	SPEED	POWER	PACKAGE
GLT6400L16LL-70TC	70ns	Normal	TSOPII 44L
GLT6400L16SL-70TC	70ns	Normal	TSOPII 44L
GLT6400L16LLI-70TC	70ns	Normal	TSOPII 44L
GLT6400L16SLI-70TC	70ns	Normal	TSOPII 44L
GLT6400L16LL-85TC	85ns	Normal	TSOPII 44L
GLT6400L16SL-85TC	85ns	Normal	TSOPII 44L
GLT6400L16LLI-85TC	85ns	Normal	TSOPII 44L
GLT6400L16SLI-85TC	85ns	Normal	TSOPII 44L

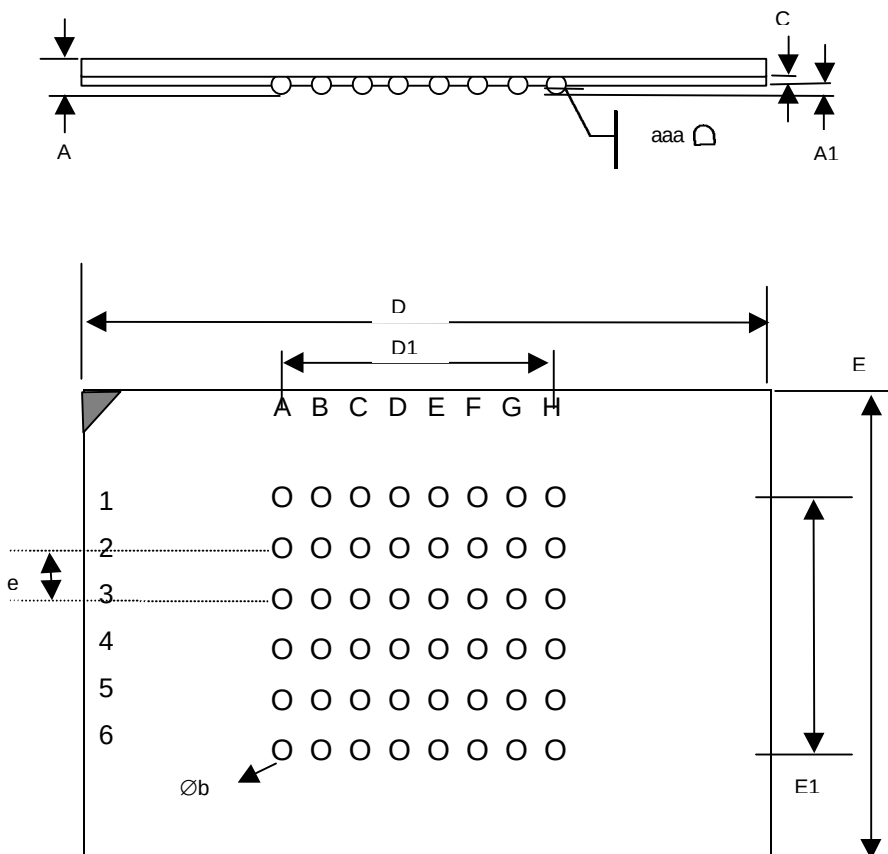
Parts Numbers (Top Mark) Definition for SRAM :


Package Information

44 pin Small Outline J-form Package (TSOPII)



GLT6400L16 fpBGA



PACKAGE OUTLINE DWG.

SYMBOL	UNIT : MM
A	1.10±0.1
A1	0.22±0.05
ϕb	0.35
C	0.32TYP
D	10.00±0.10
D1	5.25
E	8.00±0.10
E1	3.75
e	0.75TYP
aaa	0.10