GLT441L08

512K X 8 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Oct 2001 (Rev. 1.0)

Features :

- 524,288 words by 8 bits organization.
- Fast access time and cycle time.
- Low power dissipation.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 1024 refresh cycles/16ms.
- Available in 28-pin 400milSOJ/TSOP(II).
- Single +3.3V±0.3V Power Supply.
- All inputs and Outputs are TTL compatible.
- Fast Page Mode operation.

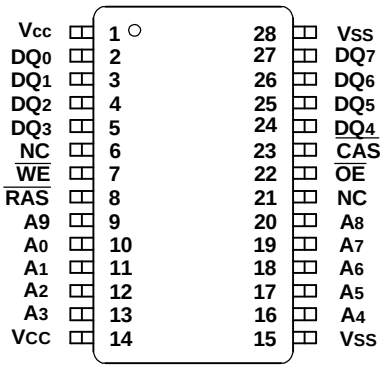
Description :

The GLT441L08 is a 524,288 x 8 bit high-performance CMOS dynamic random access memory. The GLT441L08 offers Fast Page mode ,and has both BYTE WRITE and WORD WRITE access cycles via two $\overline{CAS}$ pins. The GLT441L08 has symmetric address and accepts 1024-cycle refresh in 16ms interval.

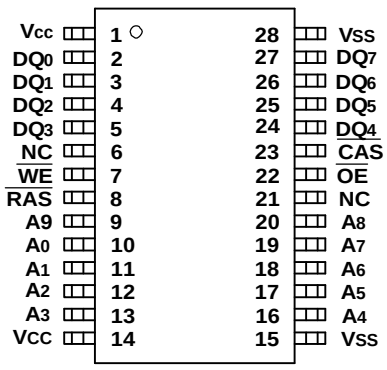
All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 8 bits, within a page, with cycle times as short as 40ns.

Pin Configuration :

28 Lead SOJ
TOP VIEW



TSOP(TYPE II)
TOP VIEW



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HIGH PERFORMANCE	60	70
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns
Min. Read/Write Cycle Time, (t_{RC})	110 ns	130 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	15 ns	20 ns

Pin Descriptions:

Name	Function
$A_0 – A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_7	Data Inputs / Outputs
V_{CC}	3.3V Power Supply
V_{SS}	Ground

Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....0°C to +70°C
Storage Temperature(plastic)....-55°C to +150°C
Voltage Relative to V_{SS}.....-1.0V to + 4.6V
Short Circuit Output Current.....50mA
Power Dissipation.....1.0W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=3.3V±0.3V, V_{SS}=0V

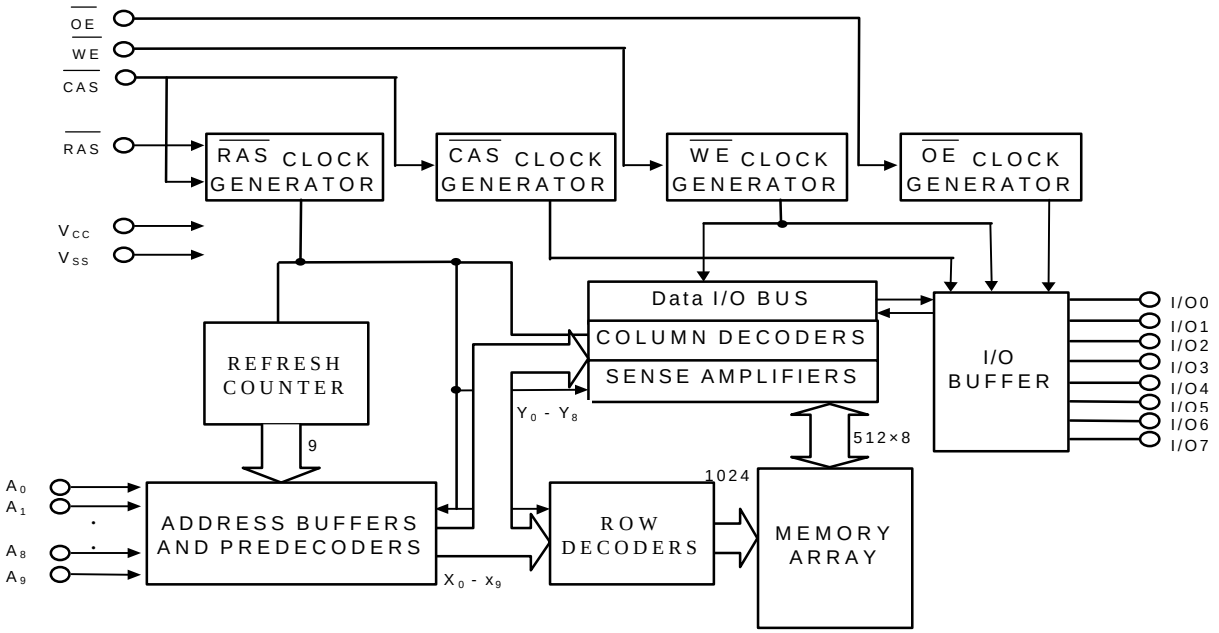
Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Block Diagram :



Truth Table: GLT441L08

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	DQs	Notes
Standby		H	H→X	X	X		High-Z	
Read		L	L	H	L	ROW/COL	Data Out	
Write: (Early Write)		L	L	L	X	ROW/COL	Data-In	
Read Write		L	L	H→L	L→H	ROW/COL	Data-Out, Data-In	
EDO-Page-Mode Read	1st Cycle	L	H→L	H	L	ROW/COL	Data-Out	
	2nd Cycle	L	H→L	H	L	COL	Data-Out	
EDO-Page-Mode Write	1st Cycle	L	H→L	L	X	ROW/COL	Data-In	
	2nd Cycle	L	H→L	L	X	COL	Data-In	
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	L→H	ROW/COL	Data-Out, Data-In	
	2nd Cycle	L	H→L	H→L	L→H	COL	Data-Out, Data-In	
Hidden Refresh	Read	L→H→L	L	H	L	ROW/COL	Data-Out	
	Write	L→H→L	L	L	X	ROW/COL	Data-In	1
RAS-Only Refresh		L	H	X	X	ROW	High-Z	
CBR Refresh		H→L	L	X	X		High-Z	

Notes:

1. EARLY WRITE only.

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC}=3.3V±0.3V, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	$V_{SS} \le V_{IN} \le V_{CC}$		-5		+5	µA	
I_{LO}	Output Leakage Current (for High-Z State)	$V_{SS} \le V_{out} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		-5		+5	µA	
I_{CC1}	V_{CC} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	t_{RAC} = 60ns t_{RAC} = 70ns			140 130	mA	1,2
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$				2	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	$t_{RC} = t_{RC}$ (min.)	t_{RAC} = 60ns t_{RAC} = 70ns			140 130	mA	2
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	Minimum Cycle	t_{RAC} = 60ns t_{RAC} = 70ns			140 130	mA	1,2
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled Other inputs $\ge V_{SS}$	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}				2	mA	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{CC}$-0.2V, $\overline{CAS} \ge V_{CC}$-0.2V, All other inputs $\ge V_{SS}$				1	mA	
V_{IL}	Input Low Voltage			-0.3		+0.8	V	3
V_{IH}	Input High Voltage			2.0		V_{CC}+0.3	V	4
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -2.0mA		2.4			V	

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC(max.)}$ is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions specified $I_{CC(max.)}$ is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.
3. Specified $V_{IL(min.)}$ is steady state operation. During transitions $V_{IL(min.)}$ may undershoot to –0.3V for a period not to exceed 20ns. All AC parameters are measured with $V_{IL(min.)} \ge V_{SS}$ and $V_{IH(max.)} \le V_{CC}$.
4. Specified V_{IH}(max.) is steady state operation . During transitions V_{IH}(max.) may overshoot to V_{CC}+0.9V for a period not to exceed 10ns. All AC parameters are measured with V_{IL}(min.) ≥ V_{SS} and VIH(max.) ≤ V_{CC} .

AC Characteristics ($0^{\circ}C \le T_A \le 70^{\circ}C$,See note 1,2)

Test condition:V_{CC}=3.3V±0.3V V_{IH}/V_{IL} = 3.0/0V , V_{OH}/V_{OL} = 2.0/0.8V

Parameter	Symbol	60		70			
		Min.	Max.	Min.	Max.	Unit	Notes
Read or Write Cycle Time	t_{RC}	110		130		ns	
Read Modify Write Cycle Time	t_{RWC}	155		185		ns	
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10k	70	10k	ns	
Access Time from $\overline{RAS}$	t_{RAC}		60		70	ns	3, 4, 9
Access Time from $\overline{CAS}$	t_{CAC}		15		20	ns	3, 4
Access Time from Column Address	t_{AA}		30		35	ns	3, 9
$\overline{CAS}$ to Output Low-Z	t_{CLZ}	0		0		ns	3
$\overline{RAS}$ Hold Time	t_{RSH}	15		20		ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10k	20	10k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	7
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		ns	
Column Address Set-Up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	10		15		ns	
Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30		35		ns	
Read Command Set-Up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	4
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	4
Write Command Set-Up Time	t_{WCS}	0		0		ns	8, 9
Write Command Hold Time	t_{WCH}	10		15		ns	
Write Command Pulse Width	t_{WP}	10		15		ns	
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15		20		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		20		ns	
Data Set-Up Time	t_{DS}	0		0		ns	
Data Hold Time	t_{DH}	10		15		ns	

AC Characteristics

Parameter	Symbol	60		70		Unit	Notes
		Min.	Max.	Min.	Max.		
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	85		100		ns	
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	40		50		ns	
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	55		65		ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay	t_{CPWD}	60		70		ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5		5		ns	
$\overline{CAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Counter Test Cycle)	t_{CPT}	20		30		ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		35		40	ns	
Page Mode Cycle Time	t_{PC}	40		45		ns	
Page Mode Read-Modify-Write Cycle Time	t_{PRWC}	85		100		ns	
$\overline{CAS}$ Precharge Time (Page Mode)	t_{CP}	10		10		ns	
$\overline{RAS}$ Pulse Width (Page Mode Only)	t_{RASP}	60	100k	70	100k	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		ns	
Access Time from $\overline{OE}$	t_{OEA}		15		20	ns	8
$\overline{OE}$ to Data Delay Time	t_{OED}	15		20		ns	
$\overline{OE}$ to Output High-Z	t_{OEZ}	0	15	0	20	ns	
$\overline{OE}$ Command Hold Time	t_{OEH}	15		20		ns	
$\overline{CAS}$ Set-Up Time for $\overline{CAS}$-Before-$\overline{RAS}$ Cycle	t_{CSR}	5		5		ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$-Before-$\overline{RAS}$ Cycle	t_{CHR}	10		15		ns	
$\overline{WE}$ to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WRP}	10		10		ns	
$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WRH}	10		10		ns	
Transition Time	t_T	3	50	3	50	ns	
Refresh Period (2,048 cycles)	t_{REF}		16		16	ms	

Notes

1. An initial pause of 100μs is required after power-up followed by any 8 $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh cycles to initialize the internal circuit.

2. $V_{IH(min.)}$ and $V_{IL(min.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$, AC measurements assume t_T = 5ns.

3. Measured with an equivalent to 1 TTL loads and 50pF.

4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CACMAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

5. t_{WCS},t_{RWD},t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD(min.)}$,$t_{RWD} \geq t_{RWD\ (min.)}$ and $t_{AWD} \geq t_{AWD(min.)}$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data
out is indeterminate.

6. t_{AR},t_{WCR}, and t_{DHR} are referenced to $t_{RAD(max.)}$.

7. $t_{OFF(max.)}$ and $t_{OEZ(max.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

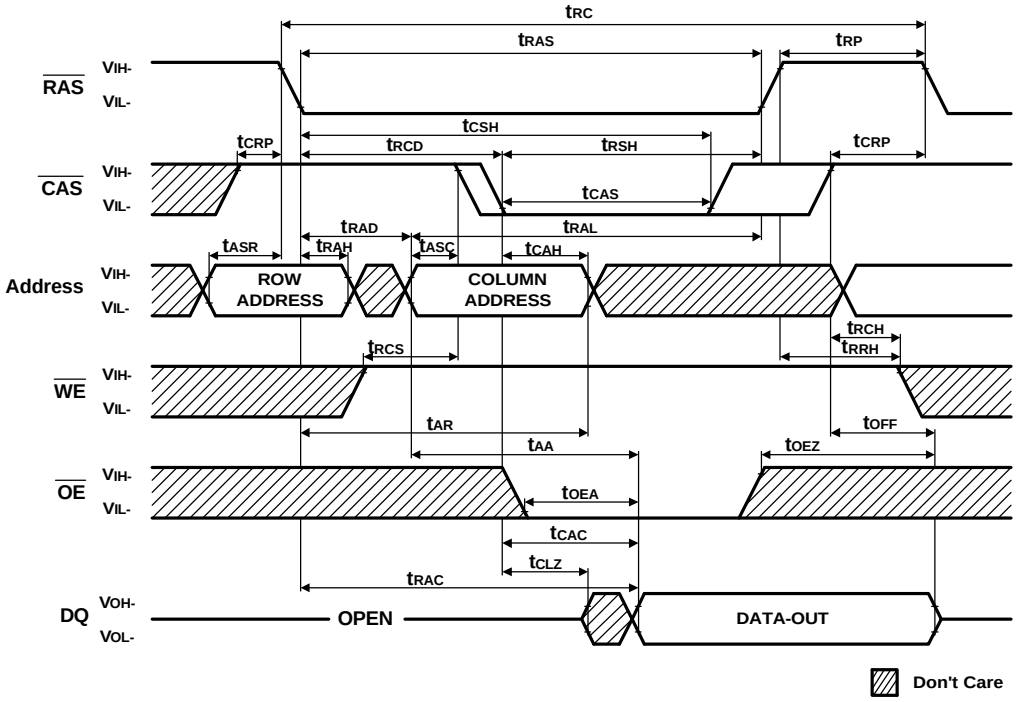
8. $t_{CRP(min)}$ requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycle preceded by any cycles.

9. Either $t_{RCH(min.)}$ or $t_{RRH(min.)}$ must be satisfied for a read cycle.

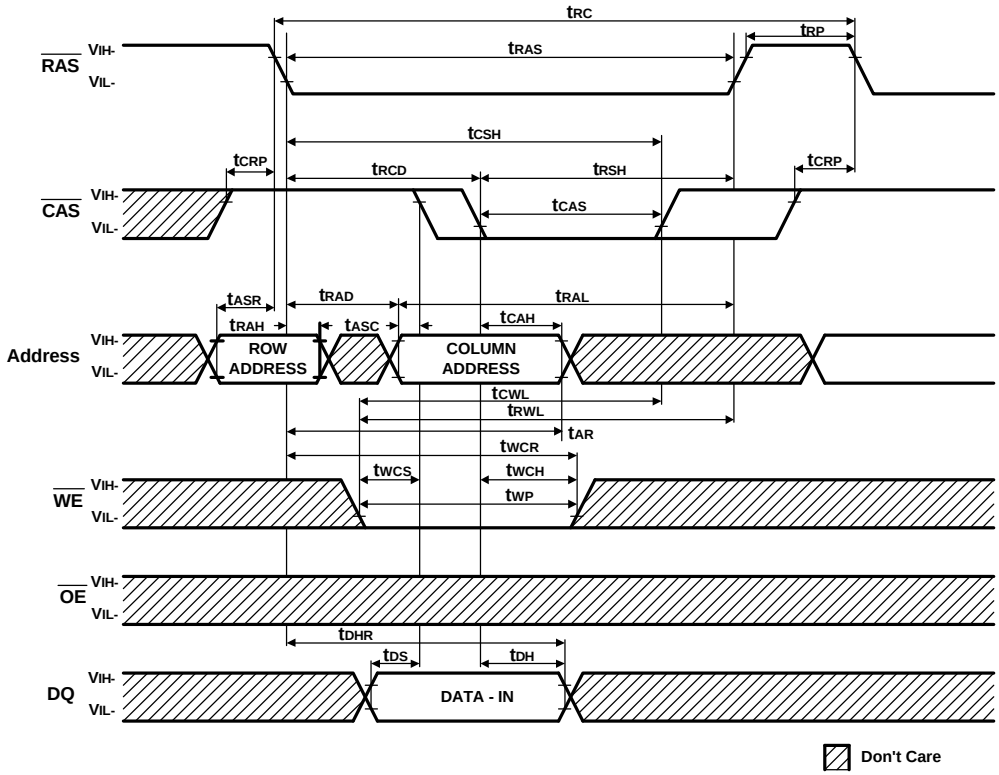
10. $t_{WP(min.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles,$t_{WCH(min.)}$ should be satisfied.

11. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.

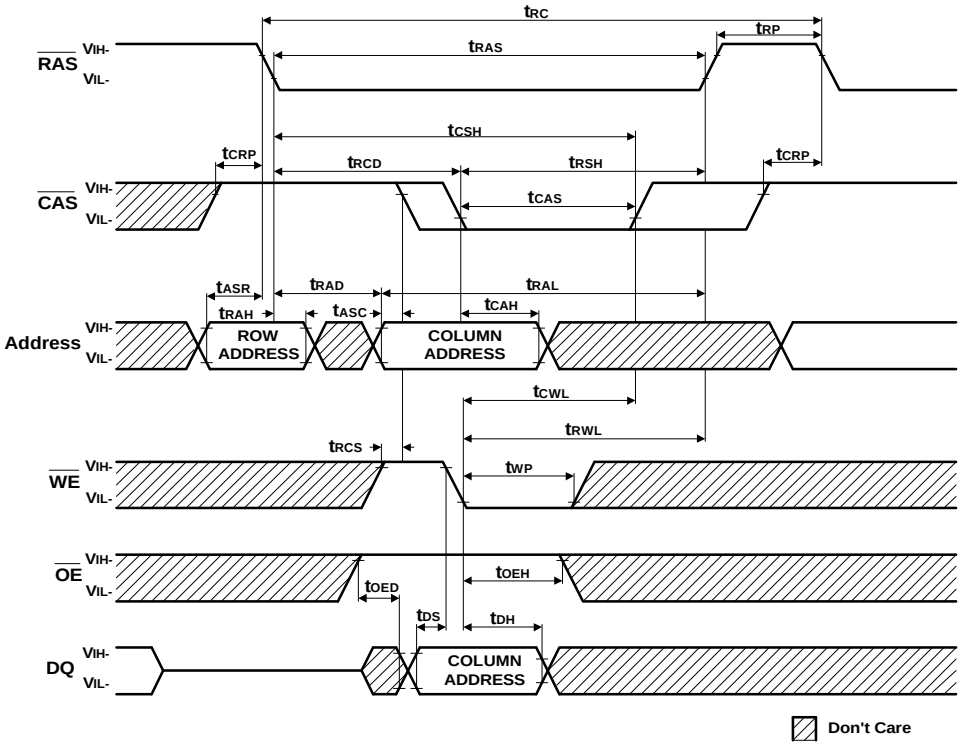
Read Cycle



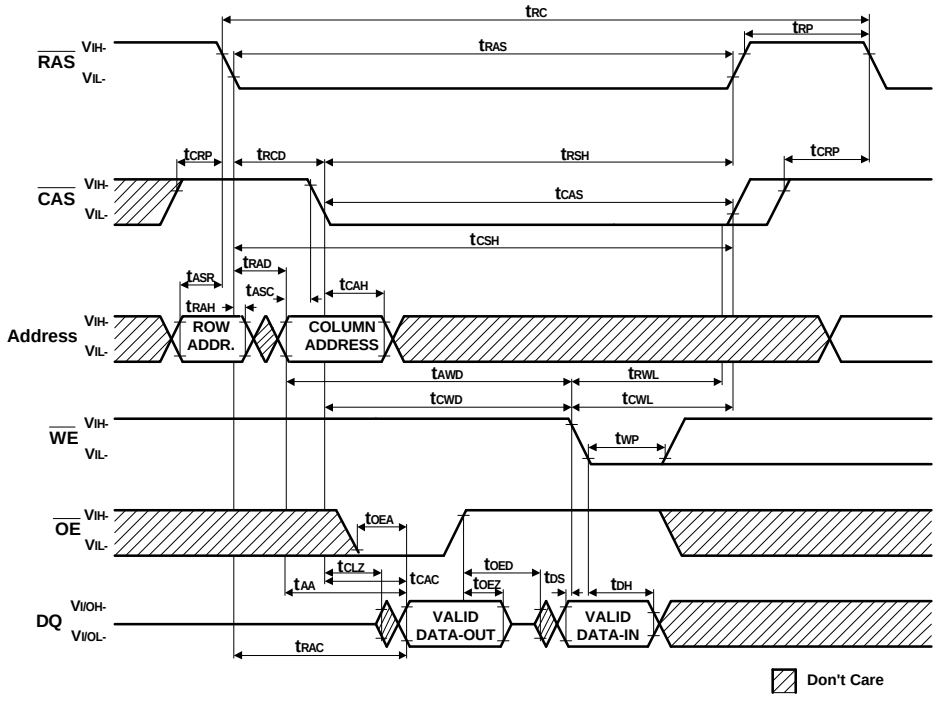
Early Write Cycle NOTE : D_{OUT} = Open



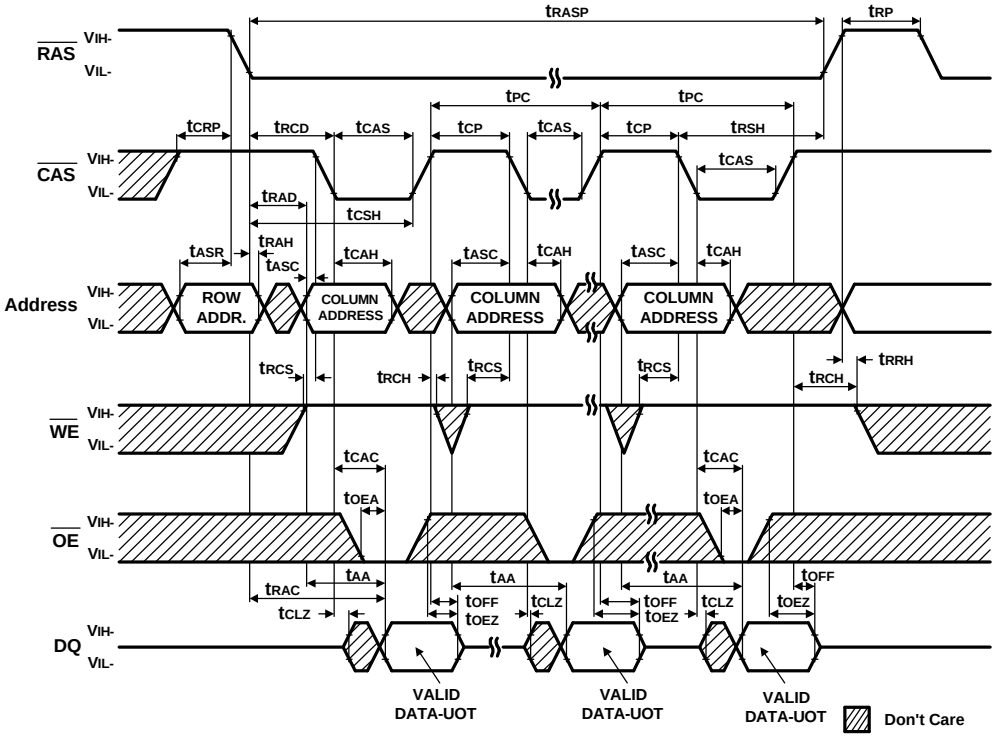
Late Write Cycle ($\overline{OE}$ Controlled Write) **NOTE : D_{OUT} = Open**



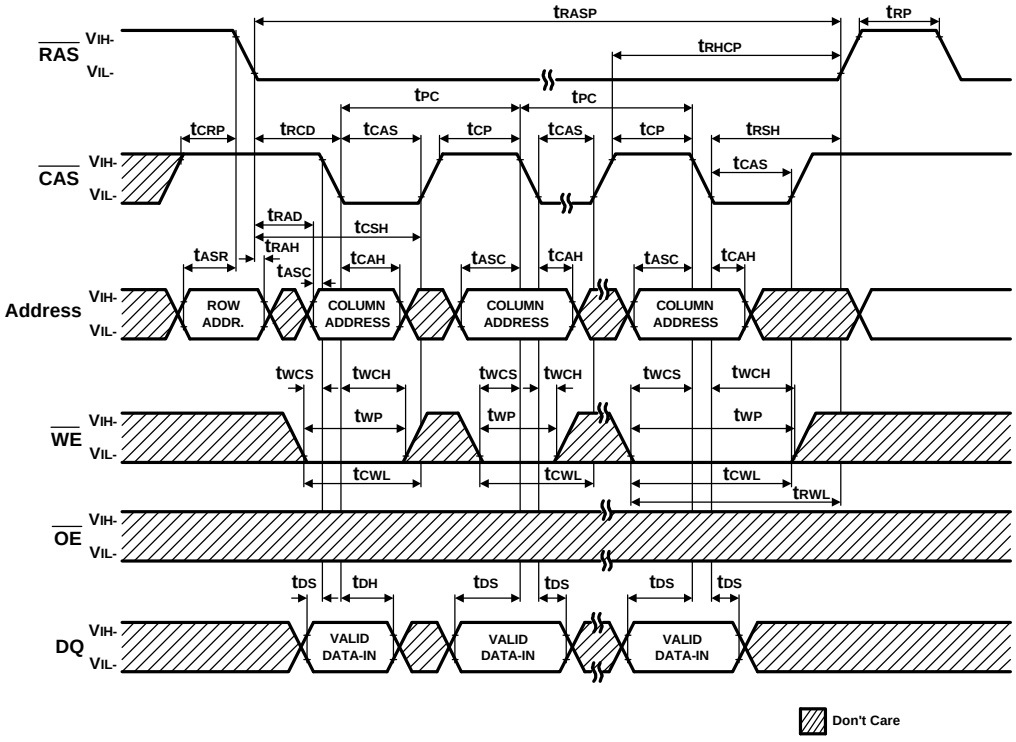
Read - Modify - Write Cycle



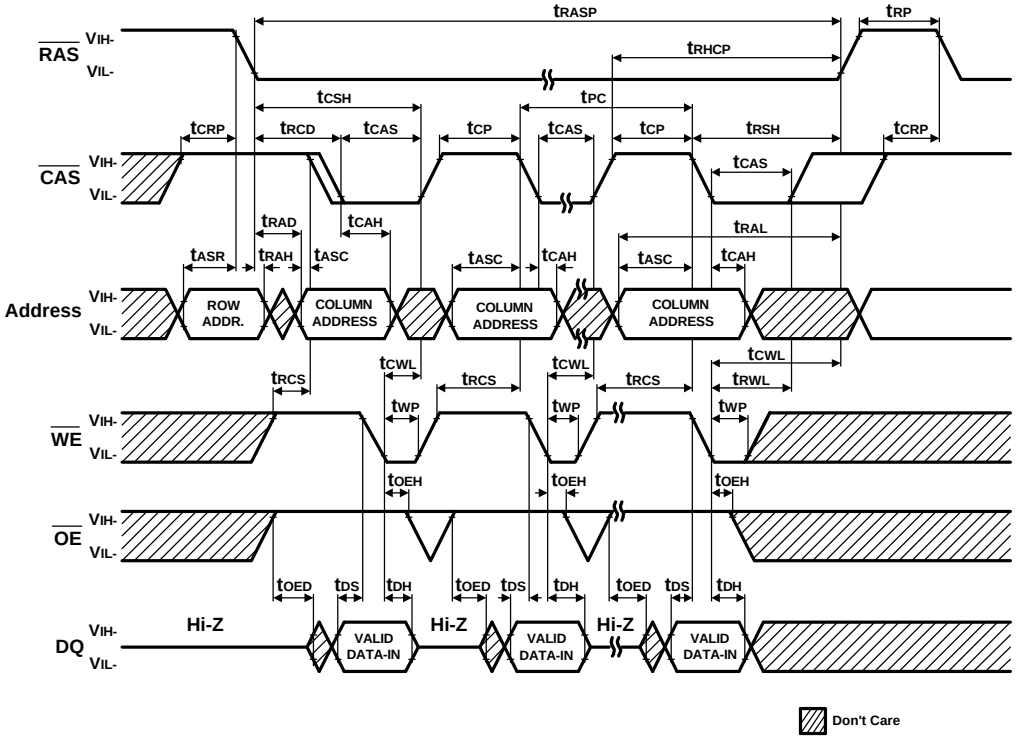
Fast Page Read Cycle



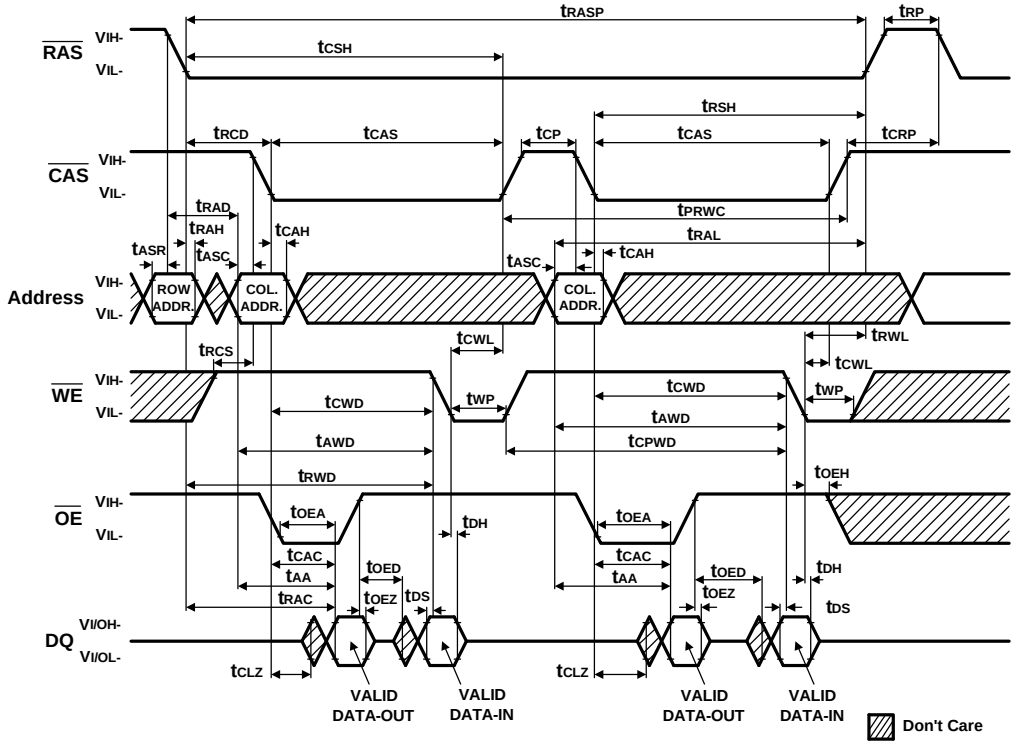
Fast Page Write Cycle NOTE : D_{OUT} = Open



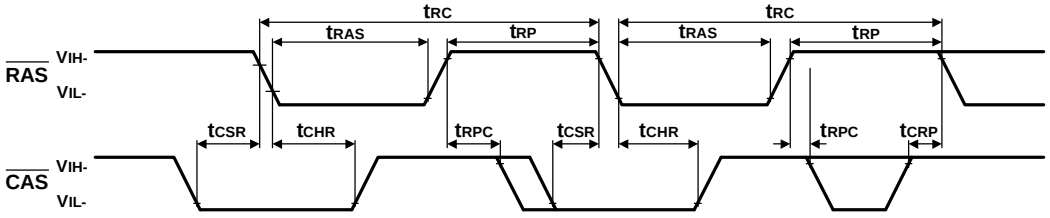
Fast Page Mode Late Write Cycle



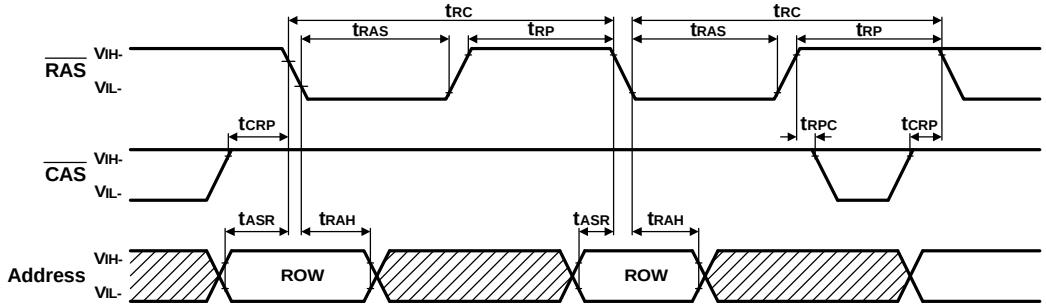
Fast Page Read - Modify - Write Cycle



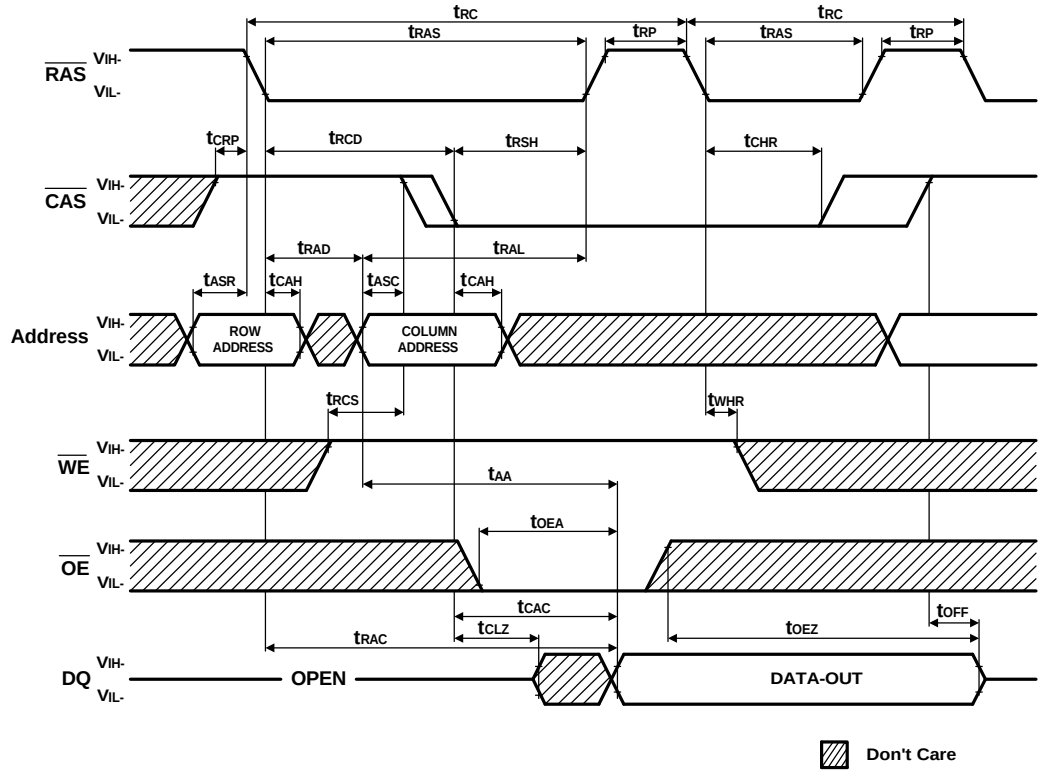
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



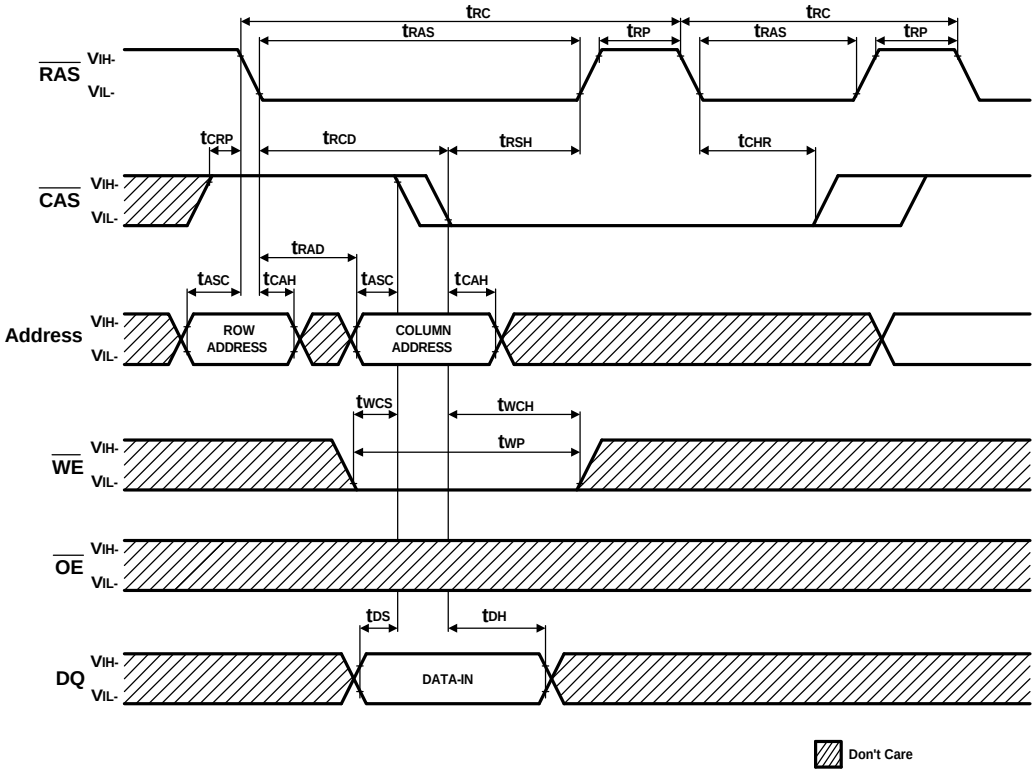
$\overline{RAS}$ -Only Refresh Cycle



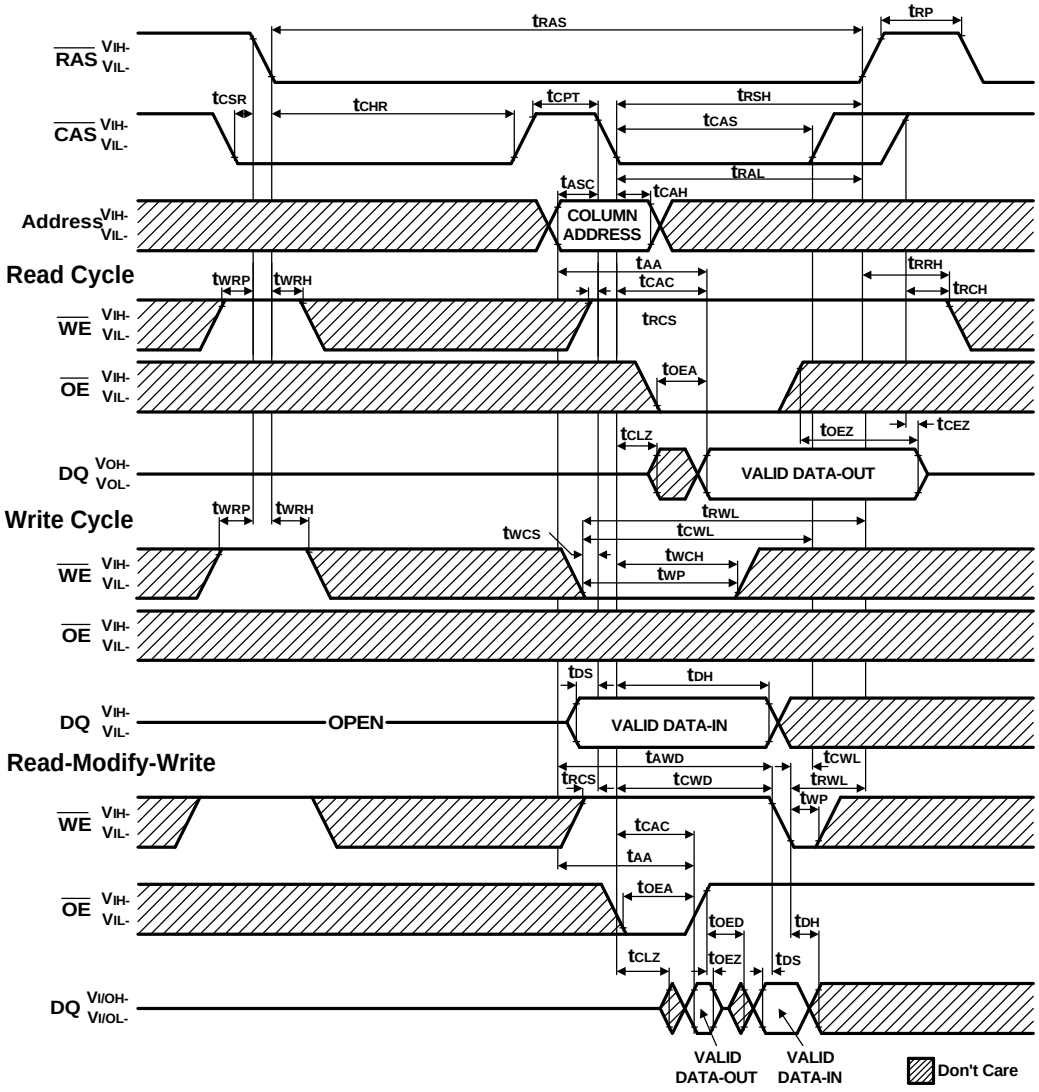
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



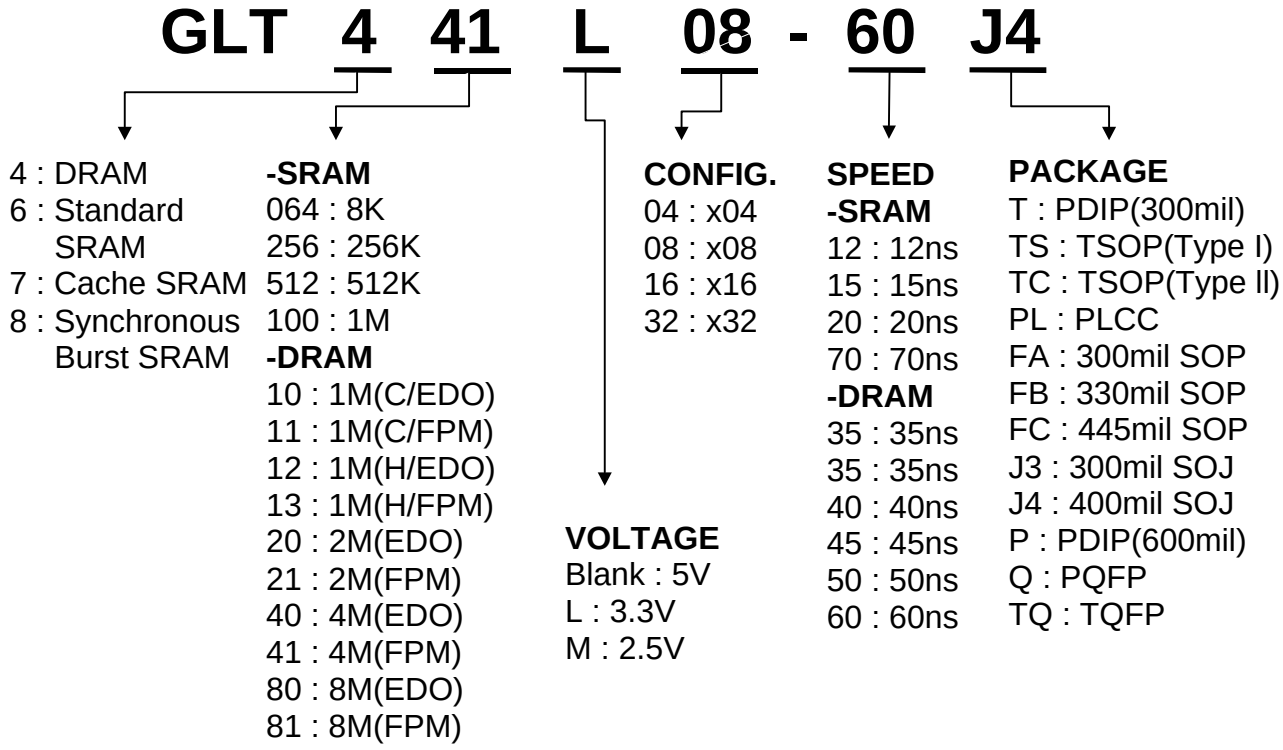
$\overline{CAS}$ - Before $\overline{RAS}$ Refresh Counter Test Cycle



Ordering Information

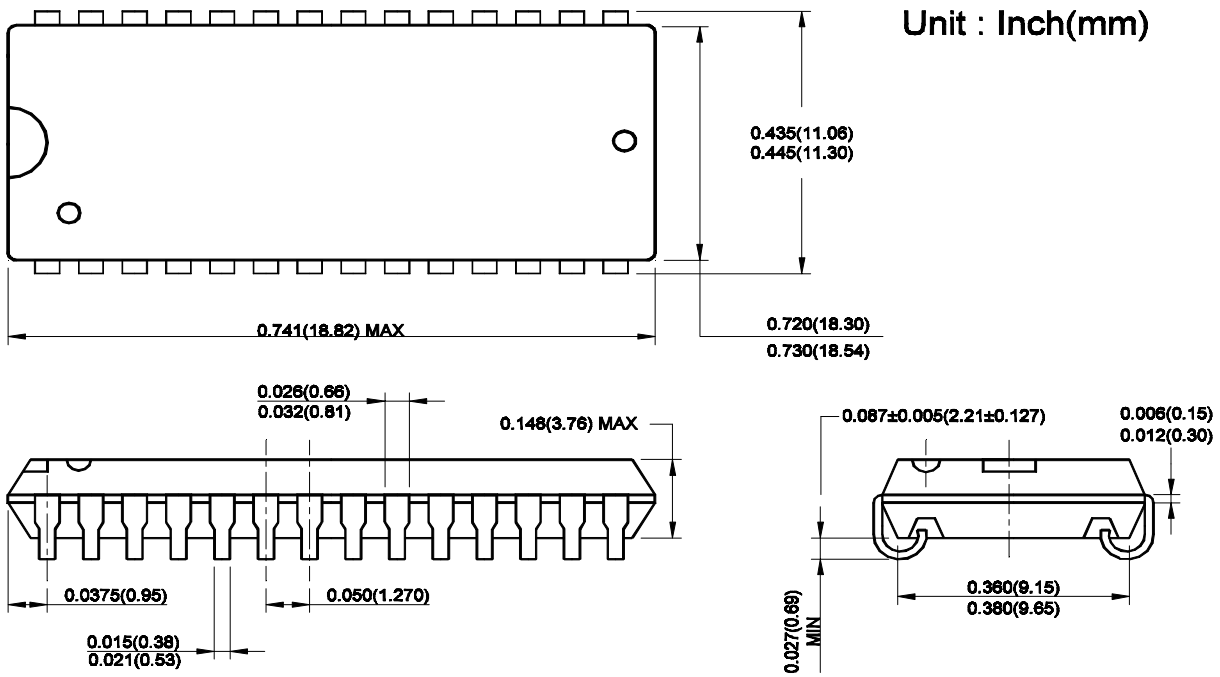
Part Number	SPEED	POWER	FEATURE	PACKAGE
GLT441L08-60J4	60ns	Normal	FPM	28L 400mil SOJ
GLT441L08-70J4	70ns	Normal	FPM	28L 400mil SOJ
GLT441L08-60TC	60ns	Normal	FPM	28L 400mil TSOP II
GLT441L08-70TC	70ns	Normal	FPM	28L 400mil TSOP II

Parts Numbers (Top Mark) Definition :



Package Information

400mil 28 Lead Small Outline J-form Package (SOJ)



400mil 28 Lead Thin Small Outline Package (TSOP) Type II