Genesys Logic, Inc.

GL814E

USB 2.0
Flash Drive Controller

Datasheet
Revision 1.00
Oct. 03, 2003

Copyright:

Disclaimer:

ALL MATERIALS ARE PROVIDED "AS IS" WITHOUT EXPRESS OR IMPLIED WARRANTY OF ANY KIND. NO LICENSE OR RIGHT IS GRANTED UNDER ANY PATENT OR TRADEMARK OF GENESYS LOGIC INC.. GENESYS LOGIC HEREBY DISCLAIMS ALL WARRANTIES AND CONDITIONS IN REGARD TO MATERIALS, INCLUDING ALL WARRANTIES, IMPLIED OR EXPRESS, OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF INTELLECTUAL PROPERTY. IN NO EVENT SHALL GENESYS LOGIC BE LIABLE FOR ANY DAMAGES INCLUDING, WITHOUT LIMITATION, DAMAGES RESULTING FROM LOSS OF INFORMATION OR PROFITS. PLEASE BE ADVISED THAT THE MATERIALS MAY CONTAIN ERRORS OR OMMISIONS. GENESYS LOGIC MAY MAKE CHANGES TO THE MATERIALS OR TO THE PRODUCTS DESCRIBED THEREIN AT ANY TIME WITHOUT NOTICE.

Trademarks:

is a registrated trademark of Genesys Logic Inc..
All trademarks are the properties of their respective owners.

Office:

Genesys Logic, Inc.
12F, No. 205, Sec. 3, Beishin Rd., Shindian City,
Taipei, Taiwan
Tel: (886-2) 8913-1888
Fax: (886-2) 6629-6168

http://www.genesyslogic.com

Revision History

Revision	Date	Description
1.00	10/03/2003	First formal release

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 GENERAL DESCRIPTION

The GL814E is a highly compatible, best performance USB 2.0 Flash Drive Controller. It supports USB 2.0 high-speed transmission to NAND type flash memory (Flash Drive). The GL814E integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver, the Serial Interface Engine (SIE), and compatible 8-bit micro-controller.

By complies with Universal Serial Bus specification rev. 2.0 and USB Storage Class specification ver.1.0, the GL814E can be supported by Windows XP/ 2000/ Me default driver. Also it is supported in Windows 98/ 98SE, Mac, and Linux operating system. For the power consumption consideration, the GL814E complies with USB power specification for bus-powered devices. And for the Flash Drive application, the GL814E supports 4 data flash banks, “Write Protect” security function, and PC boot up from USB Flash Drive.

The GL814E is available in 48-pin LQFP (Internal Mask ROM code), and it is the best cost/ performance solution for your USB 2.0 high-speed Flash Drive application.

CHAPTER 2 FEATURES

- Complies with 480Mbps Universal Serial Bus specification rev. 2.0.vc
- Complies with USB Storage Class specification rev. 1.0. (Bulk only protocol).
- Operating System supported: Win XP/ 2000/ Me/ 98/ 98SE, Mac OS 9.x/ X, Linux.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Integrated MCU compatible 8-bit micro-controller.
- Hardware ECC generation and verification.
- Supports firmware correct page ECC error capability.
- Supports automatic page copy (source page read + destination page write).
- Supports 4 data Flash Banks (maximum).
- Supports PC boot up from USB HDD or USB ZIP.
- Supports “Write Protect” security function to protect data in USB Flash Disk.
- Supports serial EEPROM 93C46 interface/on board NAND Flash for the flexibility of vendor or firmware parameters.
- Complies with USB power specification for bus-powered devices.
- Supports Suspend and Wake-up Resume.
- Provides LED indicator when USB Flash Drive is in Ready/ Working mode.
- 3.3 Volt operation.
- Available in 48-pin LQFP package.

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

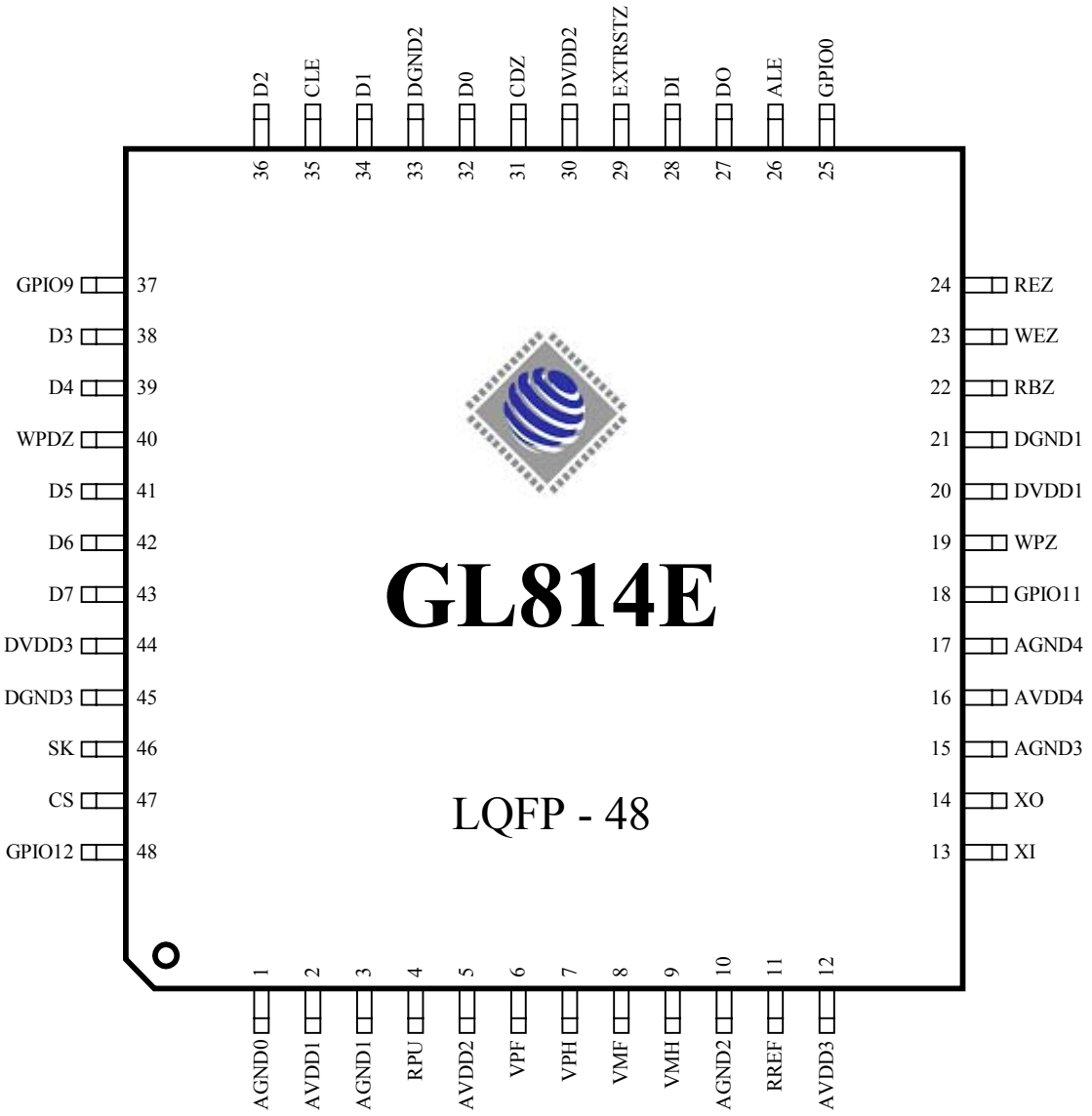


Figure 3.1 - Pinout Diagram

3.2 Pin List

Table 3.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AGND0	P	13	XI	I	25	GPIO0	B	37	GPIO9	B
2	AVDD1	P	14	XO	B	26	ALE	O	38	D3	B
3	AGND1	P	15	AGND3	P	27	DO	I/SO	39	D4	B
4	RPU	A	16	AVDD4	P	28	DI	O	40	WPDZ	B/I
5	AVDD2	P	17	AGND4	P	29	EXTRSTZ	I	41	D5	B
6	VPF	B	18	GPIO11	B	30	DVDD2	P	42	D6	B
7	VPH	B	19	WPZ	O	31	CDZ	B/I	43	D7	B
8	VMF	B	20	DVDD1	P	32	D0	B	44	DVDD3	P
9	VMH	B	21	DGND1	P	33	DGND2	P	45	DGND3	P
10	AGND2	P	22	RBZ	B/I	34	D1	B	46	SK	O
11	RREF	A	23	WEZ	O	35	CLE	O	47	CS	O
12	AVDD3	P	24	REZ	O	36	D2	B	48	GPIO12	B

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

Pin Name	Pin#	Type	Description
AGND0~4	1,3,10,15, 17	P	Analog GND #0~4
AVDD1~4	2,5,12,16	P	Analog VDD #1~4
RPU	4	A	USB resistor pull up
VPF	6	B	FS D+
VPH	7	B	HS D+
VMF	8	B	FS D-
VMH	9	B	HS D-
RREF	11	A	Reference resistor
XI	13	I	Crystal input
XO	14	B	Crystal output
GPIO0,9,11,12	25,37,18, 48	B	GPIO0, GPIO9, GPIO11, GPIO12
WPZ	19	O (pd)	WP#
DVDD1~3	20,30,44	P	Digital VDD #1~3
DGND1~3	21,33,45	P	Digital GND #1~3

RBZ	22	B/I (pu)	RDY/BSY#
WEZ	23	O	WE#
REZ	24	O	RE#
ALE	26	O (pd)	ALE
DO	27	I/SO (pd)	93C46 Data in
DI	28	O (pd)	93C46 Data out
EXTRSTZ	29	I (pu)	External reset
CDZ	31	B/I (pu)	CD#
D0~7	32,34,36, 38,39,41, 42,43	B	Data 0~7
CLE	35	O (pd)	CLE
WPDZ	40	B/I (pu)	Write Protect Detect
SK	46	O (pd)	93C46 Clock
CS	47	O (pd)	93C46 CS

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 4 BLOCK DIAGRAM

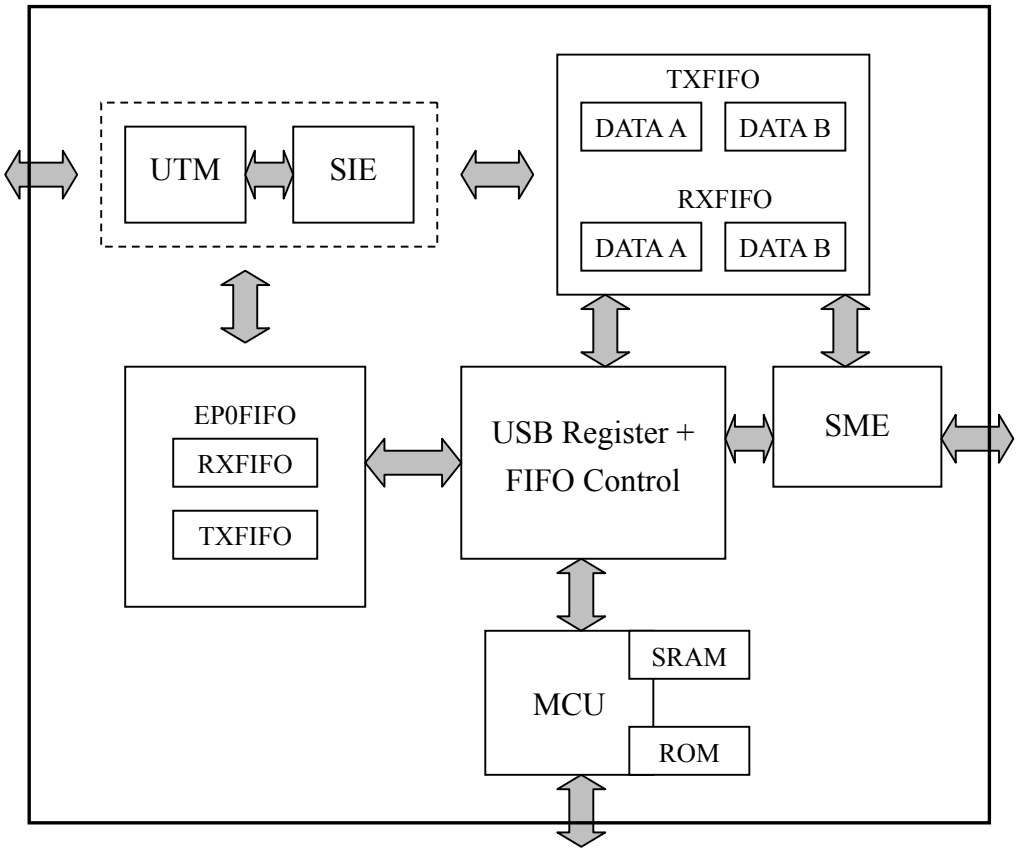


Figure 4.1 - Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0 FIFO

Endpoint 0 FIFO: The Control FIFO. It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

5.4 Bulk FIFO

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

5.4.1 TXFIFO:

- To ensure the continuous data transmission, TXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and two 16 bytes corresponding redundant areas. All can be directly accessed by MCU.
- Normally SIE popes data, SME pushes data for DATA A/B FIFOs, and redundant area is pushed by SME and popped by MCU.
- Supports MCU single byte access for SmartMedia ECC error correction.
- Supports transmit mode SIE won't transmit data filled in TXFIFO before MCU complete the data integrity checking.

5.4.2 RXFIFO:

- To ensure the continuous data transmission, RXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and 16 bytes single redundant area. All can be directly accessed by MCU.
- Normally SME popes data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by MCU and popped by SME.

5.5 SME

It is used to control the flash memory.

5.6 USB Registers / FIFO Control

It is a register space to store status information and to control the functions of GL814E by MCU.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Ambient Temperature under bias (T_A)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC}	12 MHz ± 100ppm

6.2 DC Characteristics

Table 6.2 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2.6		5	V
V_{IL}	Input Low Voltage		0.0		0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$				µA
V_{OH}	Output High Voltage		3.0			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output Current High					mA
I_{OL}	Output Current Low					mA
C_{IN}	Input Pin Capacitance				2.0	pF
I_{SUSP}	Suspend current	1.5K external pull-up included			390	µA
I_{CC}	Supply current	Connect to USB with MCU operating			120	mA

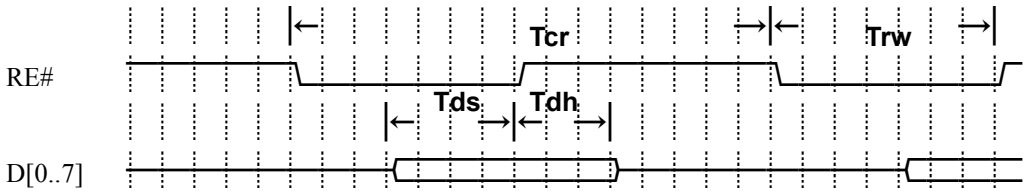
6.3 AC Characteristics

6.3.1 UTMI Transceiver

The GL814 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.3.2 NAND Flash

Read



Write

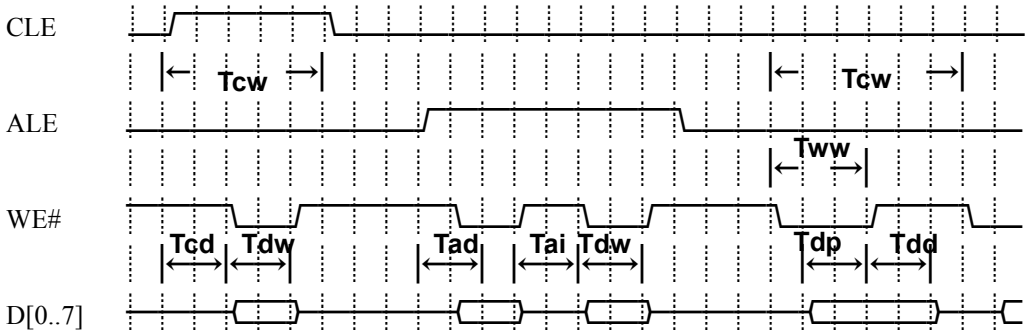
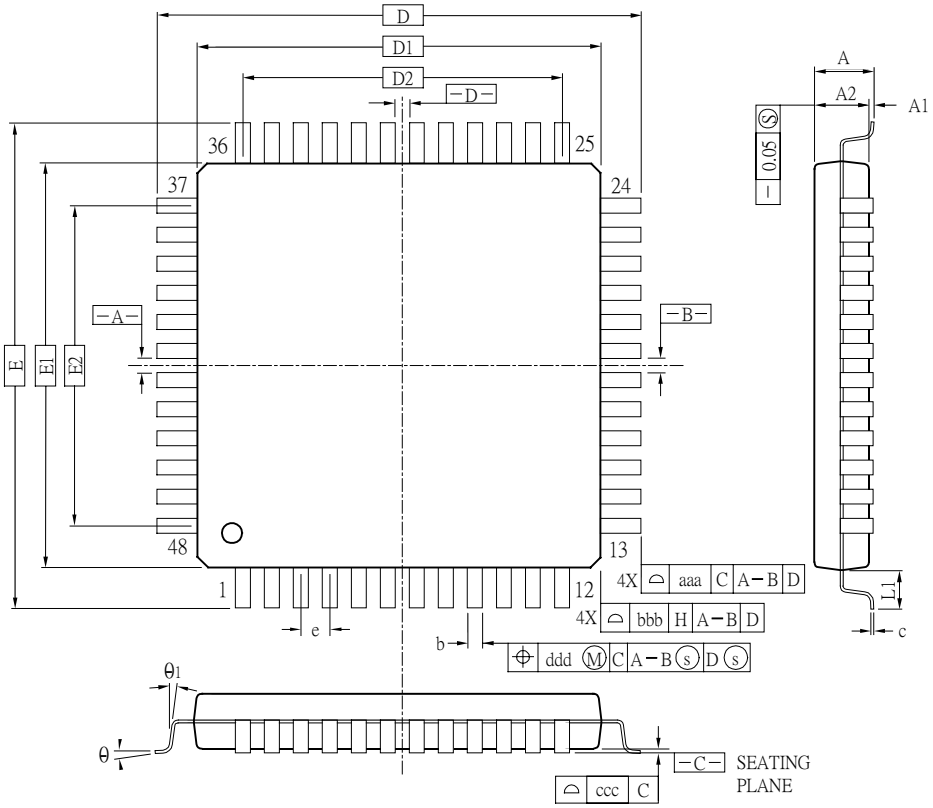
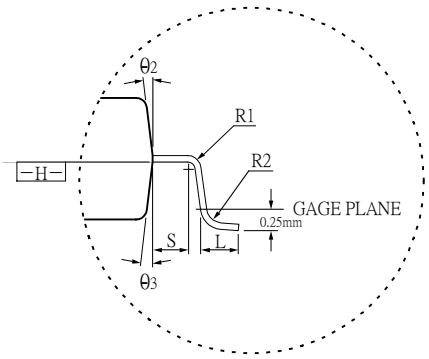


Figure 6.1 - Timing Diagram of SmartMedia

Parameter	Description	Min	Typ	Unit
Tcw	CLE active width	81		ns
Twc	Write data cycle time		50	
Tww	Write pulse width	31		
Tcd	CLE-to-command delay	16		
Tdw	Data width	31		
Tad	ALE-to-address delay	16		
Tai	Address data interval time	16		
Tdp	Data pre-output delay	20		
Tdd	Data delay time	10		
Tcr	Read data cycle time		50	
Trw	Read pulse width	30		
Tds	Data setup time	5		
Tdh	Data hold time	15		

CHAPTER 7 PACKAGE DIMENSION





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.1 - GL814E 48 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL814E	48-pin LQFP	

