Genesys Logic, Inc.

GL800USB -
USB2.0 UTMI Compliant Transceiver

Specification 1.2

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Contents

1. General Description

GL800USB is a high performance USB 2.0 Transceiver compliant with the UTMI (USB 2.0 Transceiver Macrocell Interface) Specification proposed by Intel. The UTMI specification defines a standard interface to USB 2.0 high-speed transceivers that enables common design across prototype and production implementations.

The GL800USB integrates high-speed, mixed-signal circuitry to serve as the interface between the high performance USB serial bus and the 16-bit SIE bus. The transceiver is controlled by input signals from the SIE bus, which is synchronized with the 30MHz clock output. The UTMI transceiver handles the low level USB protocol and signaling. This includes features such as: data serialization and deserialization, bit stuffing and clock recovery and synchronization. The primary focus of the UTMI transceiver is to shift the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

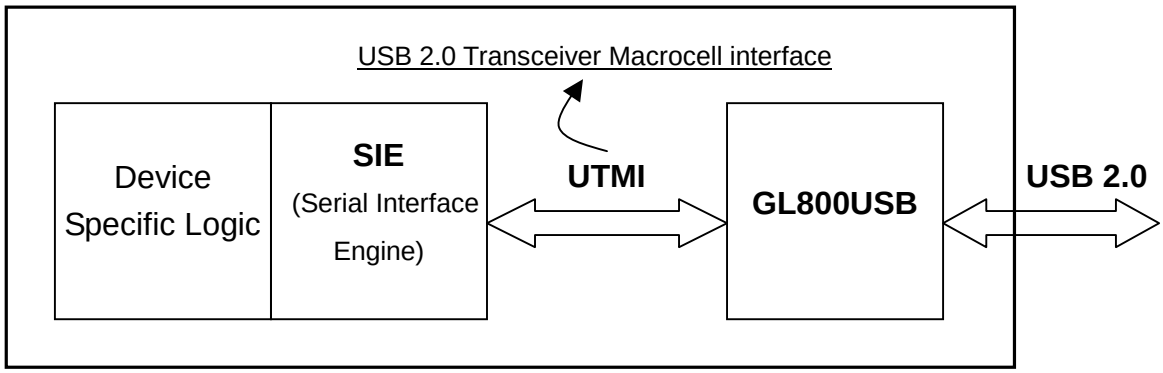
To eliminate the difficult high-speed, mixed-signal USB 2.0 logic design for system and peripheral developers, the GL800USB with standard UTMI and 40X improvement in data rate can be easily adapted for implementation of USB 2.0 high speed compliant design of widely applications, including scanners, printers, portable storage, external CD-ROM / CD-RW / DVD-ROM, flash card readers, and PC cameras.

2. Features

- Complies with Universal Serial Bus Specification Rev. 2.0.
- Complies with USB 2.0 Transceiver Macrocell Interface (UTMI) Specification.
- Supports 480 Mbit/s "High Speed" (HS) / 12 Mbit/s “Full Speed” (FS), FS Only serial data transmission rates.
- 16 bit Bi-directional Serial Interface Engine (SIE) bus
- SYNC/EOP generation and checking
- Supports “Chirp” for High Speed recognition
- Data and clock recovery from serial stream on the USB
- Bit-stuffing / unstuffing; Bit stuff error detection
- Holding registers to stage transmit and receive data
- Supports Reset and Suspend
- Supports USB 2.0 Test Mode
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks
- Available in 48 pin LQFP package (7 mm * 7mm)

3. System Configuration

3.1 System Diagram



3.2 System Description

3.2.1 GL800USB

The USB 2.0 UTMI Transceiver, which handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

3.2.2 Serial Interface Engine

The Serial Interface Engine can be further sub-divided into 2 types of sub-blocks; the SIE control logic and the Endpoint logic. The SIE control logic contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions. The Endpoint logic contains the endpoint specific logic: endpoint number recognition, FIFOs and FIFO control, etc.

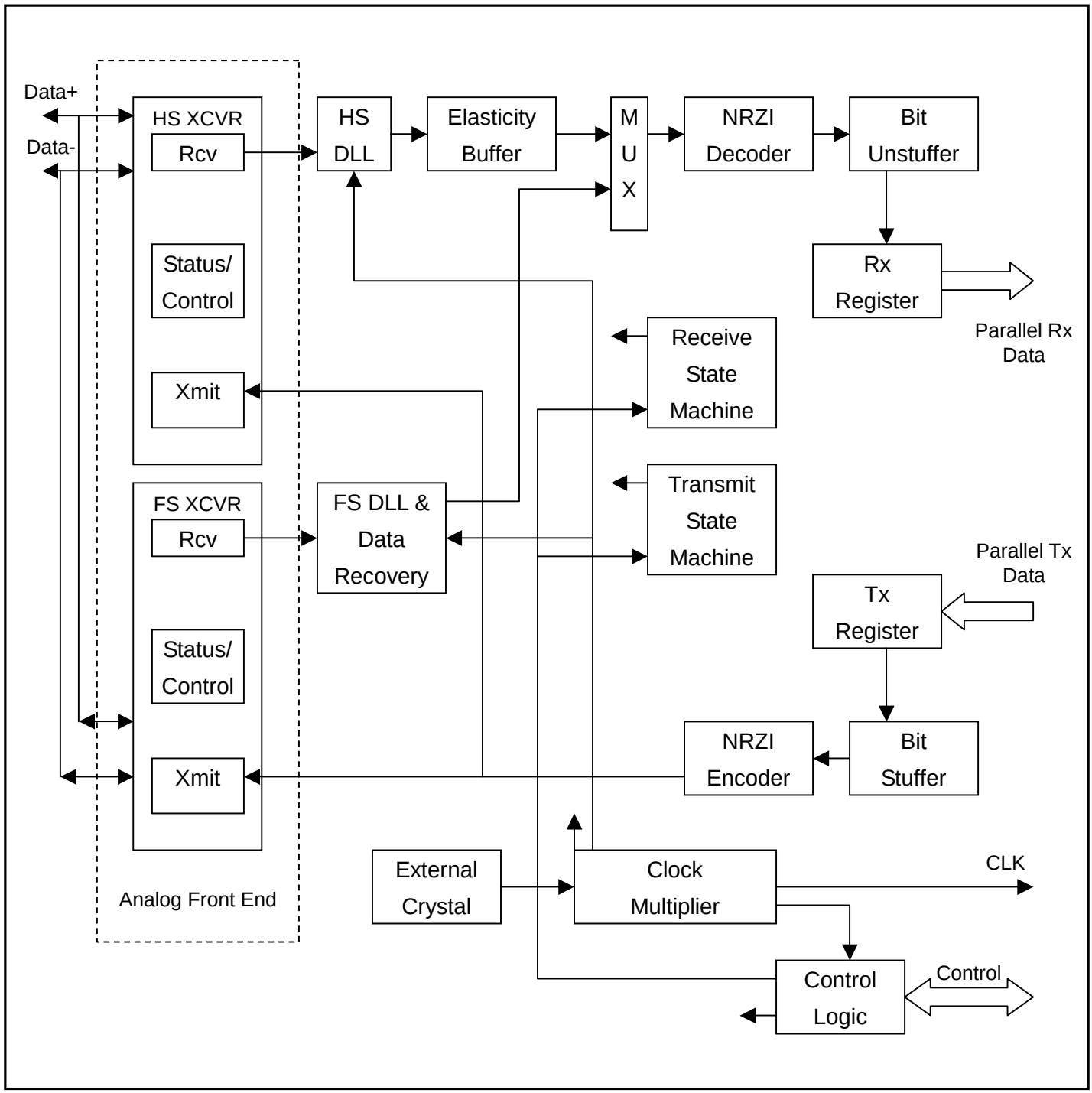
SIE logic module can be developed by peripheral vendors or purchased from IP vendors. The standardization of the UTMI allows multiple sources of SIE logic to connect with GL800USB to implement the USB 2.0 High-Speed design.

3.2.3 Device Specific Logic

This block is the glue that ties the USB interface to the specific application of the device.

4. Function Block

4.1 Block Diagram



4.2 Functional Overview

4.2.1 HS XCVR

HS XCVR contains the low-level analog circuitry required to physically interface USB 2.0 signaling to the USB DP/DM signal lines.

4.2.2 FS XCVR

FS XCVR includes the logic necessary to send and receive the FS data on USB.

4.2.3 Clock Multiplier

Clock Multiplier generates the internal clocks for the GL800USB USB 2.0 Transceiver and the CLKOUT signal. All data transfer signals are synchronized with the CLKOUT signal.

In HS mode there is one clock cycle per byte time. The frequency of clock does not change when the UTMI is switched between HS to FS modes. In FS mode there are 5 clock cycles per FS bit time, typically 40 clock cycles per FS byte time. If a received byte contains a stuffed bit then the byte boundary can be stretched to 45 clock cycles, and two stuffed bits would result in a 50 clock delay between bytes.

4.2.4 HS DLL (High Speed Delay Line PLL)

DLL extracts clock and data from the data received over the USB 2.0 interface for reception by the Receive Deserializer. The data output from the DLL is synchronous with the local clock.

4.2.5 Elasticity Buffer

Elasticity Buffer is used to compensate for difference between transmitting and receiving clocks. The USB specification defines a maximum clock error of +/- 500 ppm. When the error is calculated over the maximum packet size up to +/- 12 bits of drift can occur. The elasticity buffer is filled to a threshold prior to enabling the remainder of the down stream receive logic.

Overview and underflow conditions detected in the elasticity buffer can be reported with the **RXERR** signal.

4.2.6 Mux

The MUX block allows the data from the HS or FS receivers to be routed to the shared receive logic. The state of the Mux is determined by the **FSPEED** input.

4.2.7 NRZI Decoder

The NRZI Decoder is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates.

4.2.8 Bit Unstuffer

The Bit Unstuffer is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates. The bit unstuffer is a state machine, which strips a stuffed 0 bit from the data stream and detects bit stuff errors. In FS mode bit stuff errors asserts the **RXERR** signal. In HS mode bit stuff errors are used to generate the EOP signal so the **RXERR** signal is not asserted.

4.2.9 Rx Register

Rx Register is in charge of converting serial data received from the USB to parallel data.

4.2.10 Receive State Machine

The behavior of the Receive State Machine is described at Chapter 6, Function Description.

4.2.11 NRZI Encoder

The NRZI Encoder is compliant to standard USB 1.X specification, and it can operate at FS and HS data rates.

4.2.12 Bit Stuffer

Bit Stuffer is used by insert a zero after every six consecutive ones in the data stream before the data is NRZI encoded in order to ensure adequate signal transitions. Bit stuffing is enabled beginning with the SYNC Pattern and through the entire transmission. The data “one” that ends the SYNC Pattern is counted as the first one in a sequence.

In FS mode bit stuffing by the transmitter is always enforced, without exception. If required by the bit stuffing rules, a zero bit is inserted even after the last bit before the TXVLD signal is negated.

After 8 bits are stuffed into the USB data stream TXRDY is negated for one byte time to hold up the data stream on the Data bus.

4.2.13 Tx Register

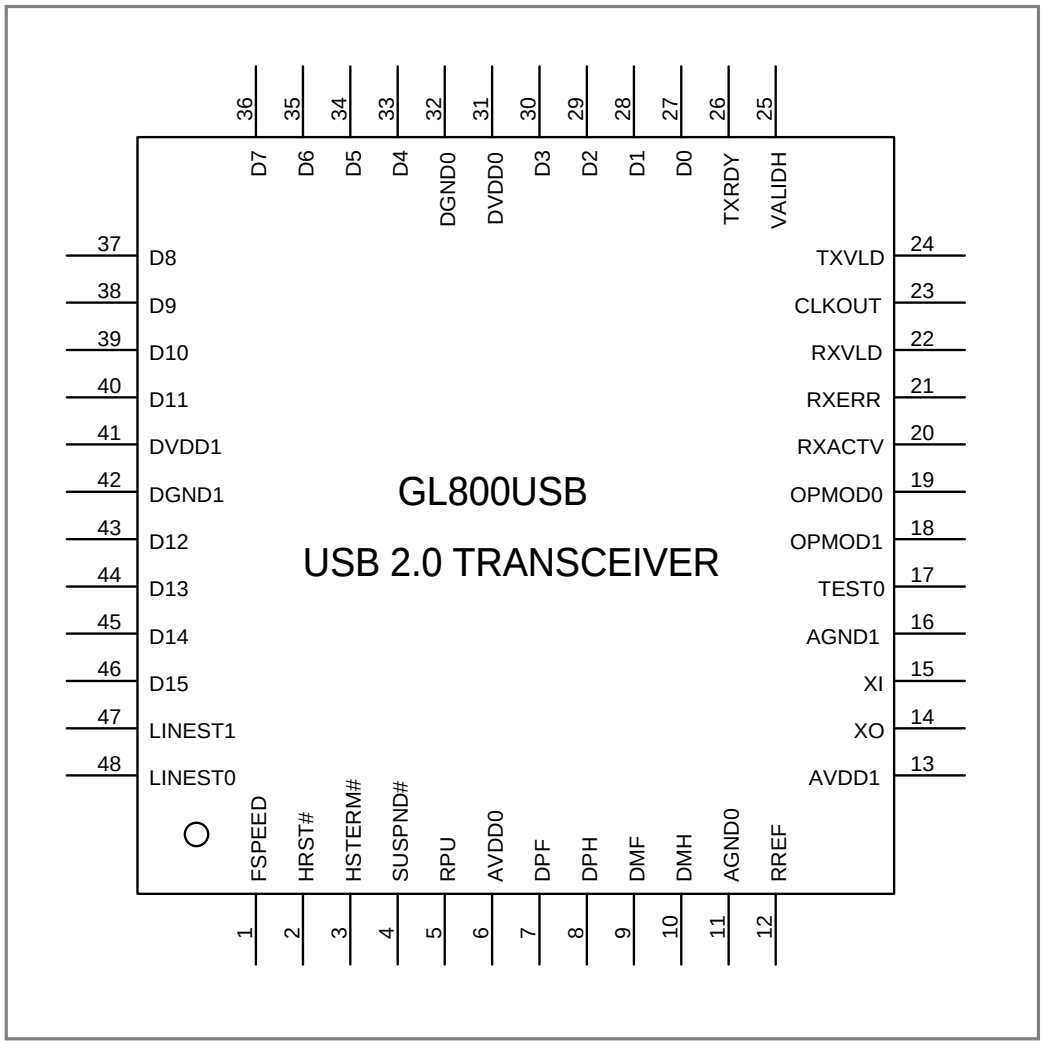
Tx Register is in charge of reading parallel data from the parallel application bus interface upon command and serializing for transmission over USB.

4.2.14 Transmit State Machine

The behavior of the Transmit State Machine is described at Chapter 6, Function Description.

5. Pinning Information

5.1 Pin Assignment



5.2 Pin Description

Pin #	Name	I/O	Pull Up/Down	Description
1	**FSPEED**	I	up	**Transceiver Select.** This signal selects between the FS and HS transceivers: 0: High Speed transceiver enabled 1: Full Speed transceiver enabled
2	**HRST#**	I	up	**Reset.** Chip reset Input, active low. This signal is used to reset all state machines in the GL800USB.
3	**HSTERM#**	I	up	**Termination Select**. HS termination enable, active low
4	**SUSPND#**	I	down	**Suspend** mode enable, active low. This signal places the GL800USB in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation. While suspended, HSTERM# must always be disabled (FS Mode) to ensure that the 1.5K pull-up on DP remains powered.
5	**RPU**	-		3.3V Pull up control for DPF
6	**AVCC0**	P		Positive analog supply (3.3V)
7	**DPF**	B		Positive USB differential data (Full Speed)
8	**DPH**	B		Positive USB differential data (High Speed)
9	**DMF**	B		Negative USB Differential Data (Full Speed)
10	**DMH**	B		Negative USB Differential Data (High Speed)
11	**AGND0**	P		Analog ground (0V)
12	**RREF**	-		510Ohm reference resistor input
13	**AVCC1**	P		Positive analog supply (3.3V)
14	**XO**	B		Crystal output
15	**XI**	I		12MHz crystal/oscillator input
16	**AGND1**	P		Analog ground (0V)
17	**TEST0**	I	down	Test mode enable
18	**OPMOD1**	I	up	**Operational mode.** These signals select between various operational modes: [1] [0] Description
19	**OPMOD0**	I	down	0 0 0: Normal Operation 0 1 1: Non-Driving 1 0 2: Disable Bit Stuffing and NRZI encoding 1 1 3: Reserved

Pin #	Name	I/O	Pull Up/Down	Description
20	**RXACTV**	O		**Receive Active**, active high. Indicates that the receive state machine has detected SYNC and is active. RXACTV is negated after a Bit Stuff Error or an EOP is detected. In HS mode, RXACTV must be negated no less than 3 and no more than 8 CLKs after an Idle state is detected on the USB. And RXACTV must be negated for at least 1 CLK between consecutive received packets. In FS/FS only modes, RXACTV must be negated no more than 2 CLKs after a FS Idle state is detected on the USB. And RXACTV must be negated for at least 4 CLKs between consecutive received packets.
21	**RXERR**	O		**Receive Error**, active high. 0: Indicates no error. 1: Indicates that a receive error has been detected. This output is clocked with the same timing as the Data lines and can occur at anytime during a transfer. If asserted, it will force the negation of RXVLD on the next rising edge of CLKOUT.
22	**RXVLD**	O		**Receive Data Valid**, active high. Indicates that the Data bus has valid data. The Rx Register is full and ready to be unloaded. The SIE is expected to latch the Data bus on the clock edge.
23	**CLKOUT**	O		**Clock.** This 30MHz clock output is used for clocking receive and transmit HS/FS 16-bit parallel data.
24	**TXVLD**	I		**Transmit Valid**, active high. Indicates that the Data bus is valid. The assertion of Transmit Valid initiates SYNC on the USB. The negation of Transmit Valid initiates EOP on the USB. In HS mode, the SYNC pattern must be asserted on the USB between 8 and 16 bit times after the assertion of TXVLD is detected by the Transmit State Machine. In FS/ FS only Modes, the SYNC pattern must be asserted on the USB no less than 1 CLK and no more than 5 CLKs after the assertion of TXVLD is detected by the Transmit State Machine.
25	**VALIDH**	B		**Transmit/Receive Valid High**, active high.

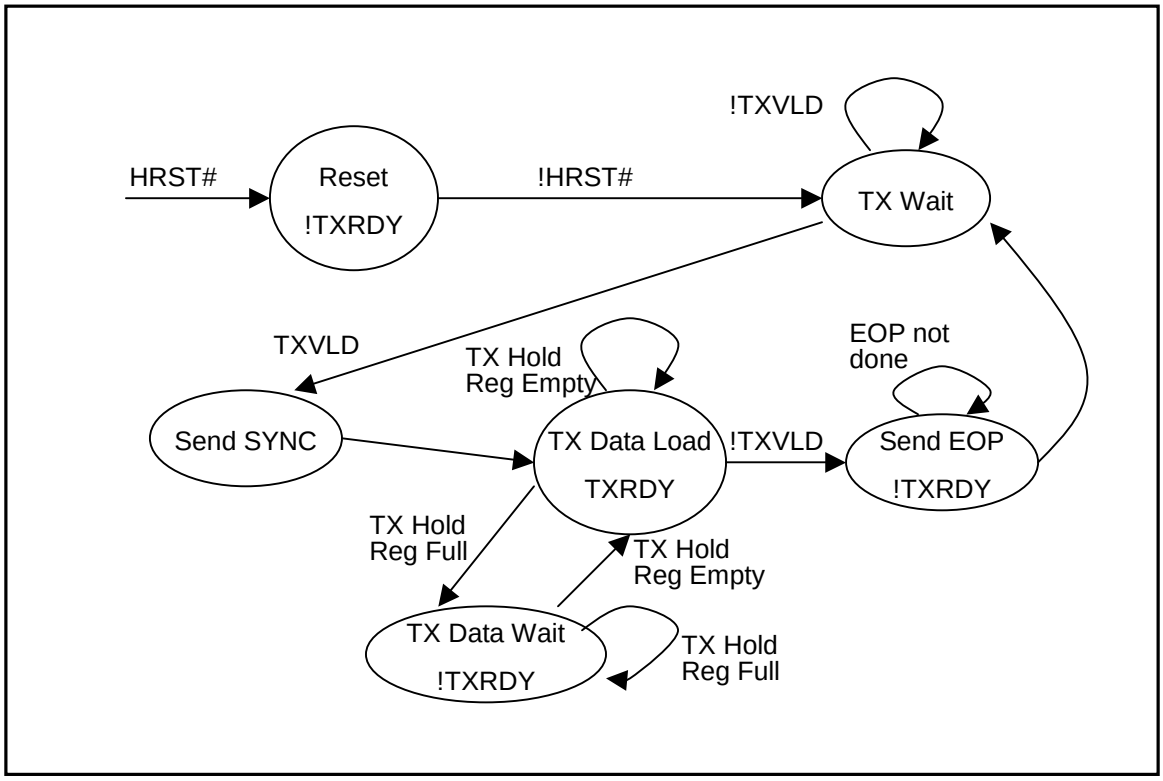
Pin #	Name	I/O	Pull Up/Down	Description
26	**TXRDY**	O		**Transmit data ready**, active high. If TXVLD is asserted, the SIE must always have data available for clocking in to the TX Register on the rising edge of CLKOUT. If TXVLD is true and TXRDY is asserted at the rising edge of CLKOUT, the GL800USB will load the data on the Data bus into the TX Register on the next rising edge of CLKOUT, at that time, SIE should immediately present the data for next transfer on the Data bus. If TXVLD is asserted and TXRDY is negated, the SIE must hold the previously asserted data on the Data bus. From the time TXVLD is negated, TXRDY is a don't care for the SIE.
27	**D 0**	B		Data bus 0
28	**D 1**	B		Data bus 1
29	**D 2**	B		Data bus 2
30	**D 3**	B		Data bus 3
31	**DVCC0**	P		Positive digital supply (3.3V)
32	**DGND0**	P		Digital ground (0V)
33	**D 4**	B		Data bus 4
34	**D 5**	B		Data bus 5
35	**D 6**	B		Data bus 6
36	**D 7**	B		Data bus 7
37	**D 8**	B		Data bus 8
38	**D 9**	B		Data bus 9
39	**D 10**	B		Data bus 10
40	**D 11**	B		Data bus 11
41	**DVCC1**	P		Positive digital supply (3.3V)
42	**DGND1**	P		Digital ground (0V)
43	**D 12**	B		Data bus 12
44	**D 13**	B		Data bus 13
45	**D 14**	B		Data bus 14
46	**D 15**	B		Data bus 15

<table>
<tr><th>Pin #</th><th>Name</th><th>I/O</th><th>Pull Up/Down</th><th>Description</th></tr>
<tr><td>47</td><td>LINEST1</td><td>O</td><td></td><td rowspan="2">Line State. These signals reflect the current state of the single ended receivers. They are combinatorial until a “usable” CLKOUT is available then they are synchronized to CLKOUT. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals:
DM DP Description
0 1 0: SE0
0 1 1: ‘J’ State
1 0 2: ‘K’ State
1 1 3: SE1</td></tr>
<tr><td>48</td><td>LINEST0</td><td>O</td><td></td></tr>
</table>

6. Functional Description

6.1 Transmit Operation

6.1.1 Transmit State Diagram

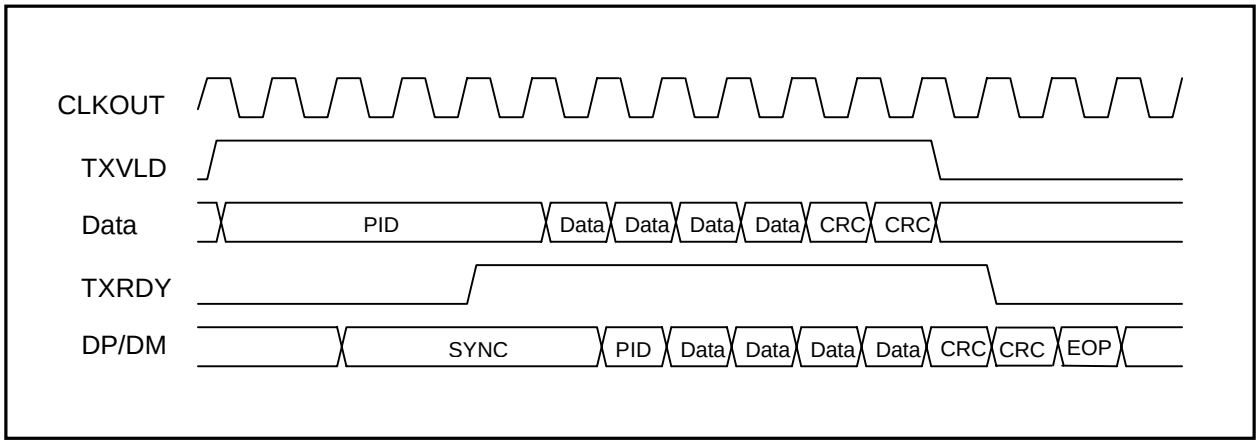


- Transmit must be asserted to enable any transmissions.
- The SIE asserts TXVLD to begin a transmission.
- The SIE negates TXVLD to end a transmission.
- After the SIE asserts TXVLD it can assume that the transmission has started when it detects TXRDY asserted.
- The SIE assumes that the UTM has consumed a data byte if TXRDY and TXVLD are asserted.
- The SIE must have valid packet information (PID) asserted on the Data bus coincident with the assertion of TXVLD. Depending on the UTM implementation, TXRDY may be asserted by the Transmit State Machine as soon as one CLK after the assertion of TXVLD.
- TXVLD and TXRDY are sampled on the rising edge of CLKOUT.
- The Transmit State Machine does not automatically generate Packet ID's (PIDs) or

CRC. When transmitting, the SIE is always expected to present a PID as the first byte of the data stream and if appropriate, CRC as the last bytes of the data stream.

- The SIE must use LINEST0/1 to verify a Bus Idle condition before asserting TXVLD in the TX Wait state.

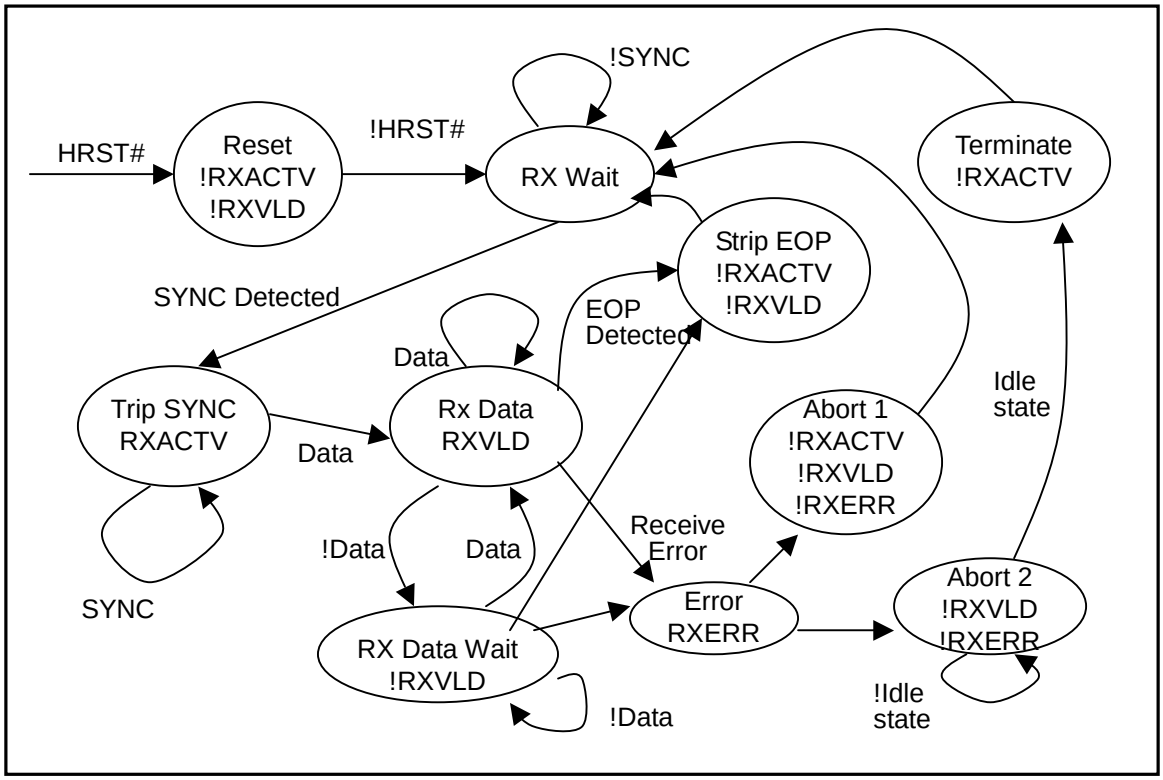
6.1.2 Transmit Timing for Data Packet



The SIE negates TXVLD to complete a packet. Once negated, the Transmit State Machine will never reassert TXRDY until after the EOP has been loaded into the Transmit Shift Register. Note that the UTM Transmit State Machine can be ready to start another package immediately, however the SIE must confirm to the minimum inter-packet delays identified in the USB 2.0 Specification.

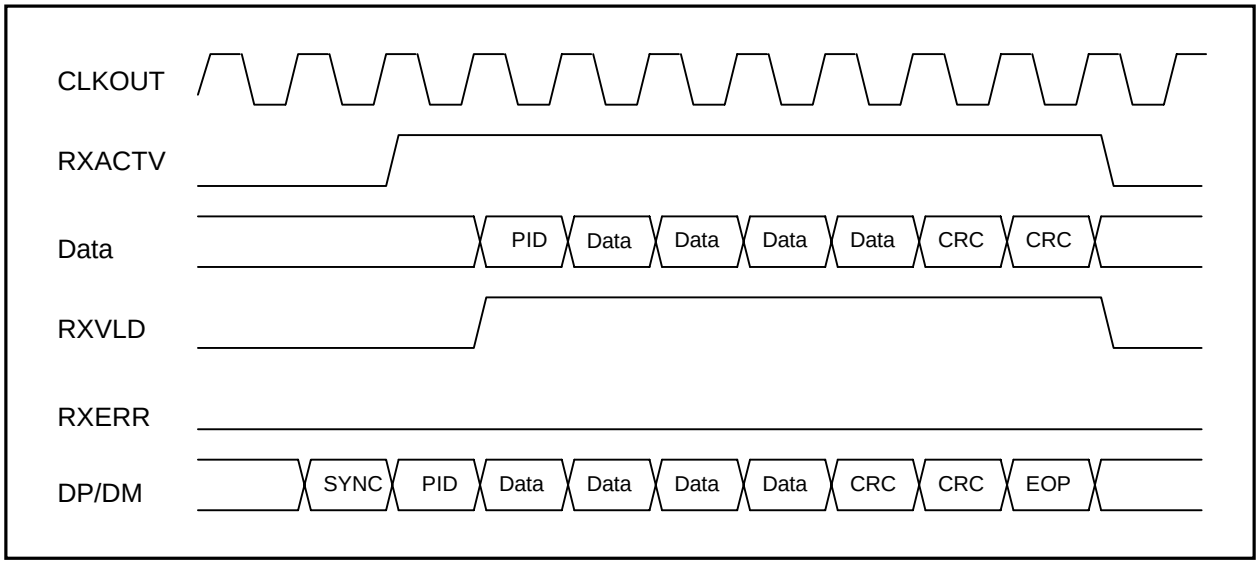
6.2 Receive Operation

6.2.1 Receive State Diagram



- RXACTV and RXVLD are sampled on the rising edge of CLKOUT.
- In the RX Wait state the receiver is always looking for SYNC.
- The Macrocell asserts RXACTV when SYNC is detected (Strip SYNC state).
- The Macrocell negates RXACTV when an EOP is detected (Strip EOP state).
- When RXACTV is asserted, RXVLD will be asserted if the RX Holding Register is full.
- RXVLD will be negated if the RX Holding Register was not loaded during the previous byte time. This will occur if 8 stuffed bits have been accumulated.
- The SIE must be ready to consume a data byte if RXACTV and RXVLD are asserted (RX Data state).
- In FS mode, if a bit stuff error is detected then the Receive State Machine will negate RXACTV and RXVLD, and return to the RXWait state.

6.2.2 Receive Timing for Data Packet (with CRC-16)



Note that the USB 2.0 transceiver does not decode Packet ID's (PIDs). They are passed to the SIE for decoding.

This timing example is in HS mode. When a HS/FS UTM is in FS mode there are approximately 40 clock cycles every byte time. The Receive State Machine assumes that the SIE captures the data on the data bus if RXACTV and RXVLD are asserted. In FS mode, RXVLD will only be asserted for one clock per byte time.

Note that the receive and transmit sections of the transceiver operate independently. The receiver will receive any packets on the USB. The transceiver does not identify whether the packet that it is receiving from the upstream or the downstream port. The SIE must ignore receive data while it is transmitting.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

Symbol	Description	Min	TYP	Max
VCC	DC supply voltage	3.0V	3.3V	3.6V
V_I	DC input voltage	2.8V	3.3V	3.8V
$V_{I/O}$	DC input voltage range for I/O	2.8V	3.3V	3.8V
$V_{AI/O}$	DC input voltage for USB D+/D- pins	2.8V	3.3V	3.8V
$V_{I/OZ}$	DC voltage applied to outputs in High Z state	2.8V	3.3V	3.8V
V_{ESD}	Static discharge voltage	4000V		
T_A	Ambient Temperature	0 ^oC		100 ^oC

7.2 DC Characteristics (Digital Pins)

Symbol	Description	Min	Typ	Max	Unit
P_D	Power Dissipation				MA
V_{DD}	Power Supply Voltage	3	3.3	3.6	V
I_O	DC output sink current excluding D+/D-/VCC/GND	8			MA
V_{IL}	LOW level input voltage			0.9	V
V_{IH}	HIGH level input voltage	2.0			V
V_{TLH}	LOW to HIGH threshold voltage	1.3	1.43	1.56	V
V_{THL}	HIGH to LOW threshold voltage	1.3	1.43	1.56	V
V_{HYS}	Hysteresis voltage	-	0	-	V
V_{OL}	LOW level output voltage when I_{OL}=8mA			0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4			V
I_{OLK}	Leakage current for pads with internal pull up or pull down resistor			46	μA
R_{DN}	Pad internal pull down resister (**Note 1**)	79K	105K	152K	Ohms
R_{UP}	Pad internal pull up resister (**Note 2**)	78K	104K	146K	Ohms

7.3 DC Characteristics (D+/D-)

Symbol		Description	Min	Typ	Max	Unit
HS	V_{DIFS}	Differential Receiver Input Sensitivity	0.15			V
	V_{CMFS}	Differential Receiver Common-Mode Voltage	0.8		2.5	V
	V_{ILSE}	Single-Ended Receiver Low Level Input Voltage			0.8	V
	V_{IHSE}	Single-Ended Receiver High Level Input Voltage	2.0			V
	V_{HYSSE}	Single-Ended Receiver Hysteresis Voltage	0.1	0.15	0.2	V
	V_{FSOL}	Low Level Output Volatge			0.3	V
	V_{FSOH}	High Level Output Voltage	2.8		3.6	V
	Z_{HSDRV}	Driver Output Impedance for HS and FS	40.5	45	49.5	Ohm
	Z_{INP}	Input Impedance	10			Mohm
FS	V_{DHS}	HS Differential Input Sensitivity	100			mV
	V_{CMHS}	HS Data Signaling Command Mode Voltage Range	-500		500	mV
	V_{HSSQ}	HS Squelch Detection Thershold(Differential)	150		100	mV
	V_{HSOL}	High Speed Low Level Output Voltage	-10		10	mV
	V_{HSOH}	High Speed High Level Output Voltage	360		440	mV
	V_{OLHS}	High Speed IDLE Level Output Voltage	-10		10	mV
	V_{CHIRPJ}	Chirp-J Output Voltage(Differential)	700		1100	mV
	V_{CHIRPK}	Chirp-K Output Voltage(Differential)	-900		-500	mV
C_{IN}		Transceiver capacitance			20	pF
I_{LO}		Hi-Z state data line leakage	-10		+10	μA

7.4 Switching Characteristics

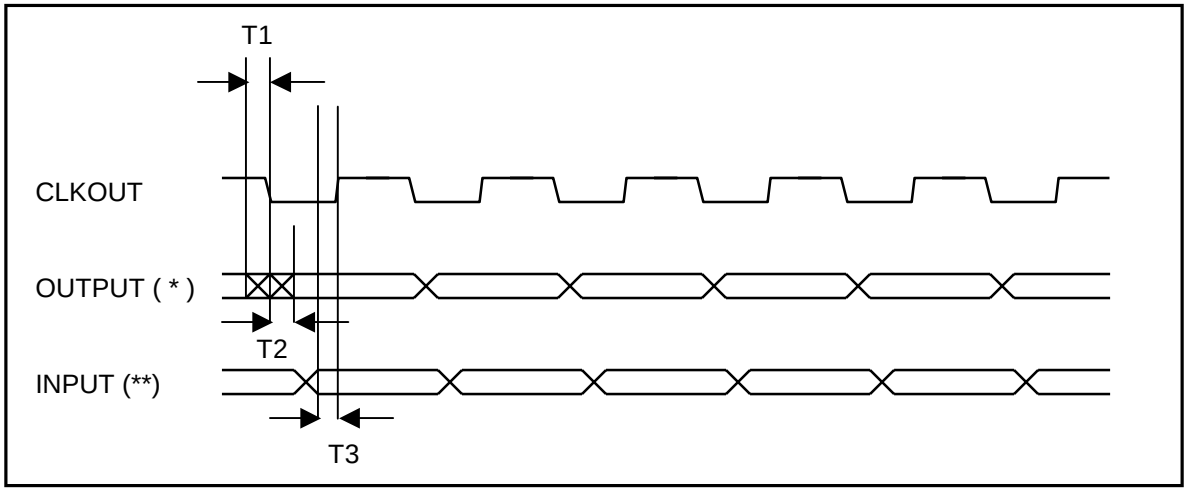
Symbol	Description	Min	Typ	Max	Unit
F_{X1}	X1 crystal frequency	11.97	12	12.03	MHz
T_{CYC}	X1 cycle time		83.3		ns
T_{X1L}	X1 clock LOW time	$0.45T_{cyc}$			ns
T_{X1H}	X1 clock HIGH time	$0.45T_{cyc}$			ns
T_{r30pf}	Output pad rise time from 10% to 90% swing with 30pF loading				ns
T_{f30pf}	Output pad fall time from 10% to 90% swing with 30pF loading				ns
T_{r50pf}	Output pad rise time from 10% to 90% swing with 50pF loading				ns
T_{f50pf}	Output pad fall time from 10% to 90% swing with 50pF loading				ns
T_{rUSB}	D+/D- rise time with 50pF loading	4		20	ns
T_{fUSB}	D+/D- fall time with 50pF loading	4		20	ns

7.5 Operating & Suspend Current

Symbol	Description	Min	Typ	Max	Unit
I_{FSTX}	FS Transmit Current			76	mA
I_{FSRX}	FS Receive Current			75	mA
I_{HSTX}	HS Transmit Current			96	mA
I_{HXRX}	HS Receive Current			95	mA
I_{SUS}	Operating Suspend Current			16	uA

7.6 Timing Chart

7.6.1 CLKOUT rising and falling edge vs. Input / Output signals

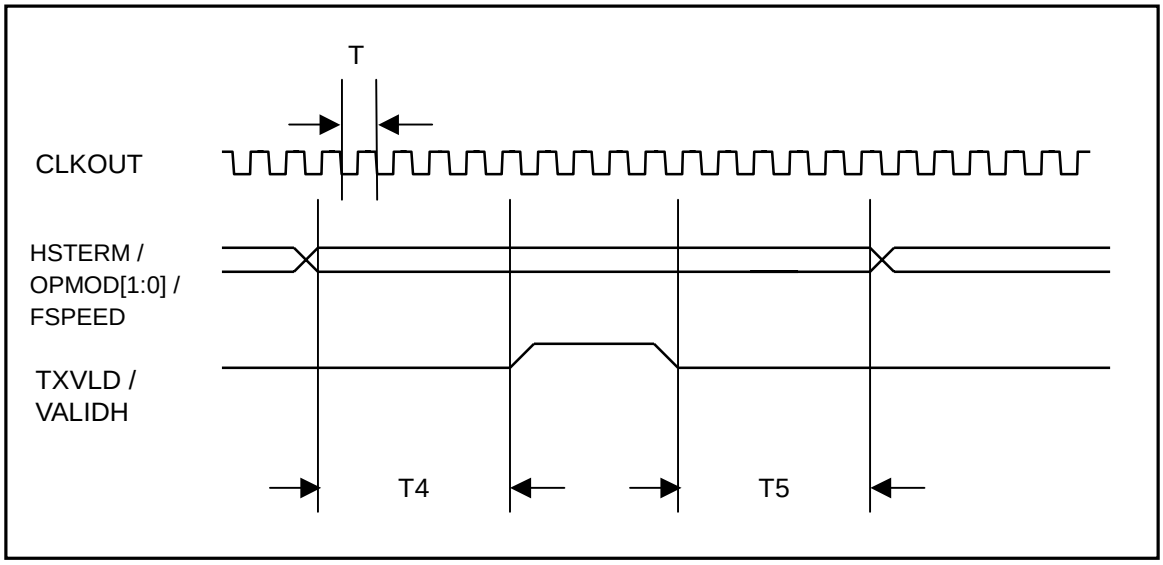


1. Output signals includes TXRDY, RXACTV, RXERR, RXVLD, LINEST[1:0], D[15:0]

** Input signals includes TXVLD, VALIDH

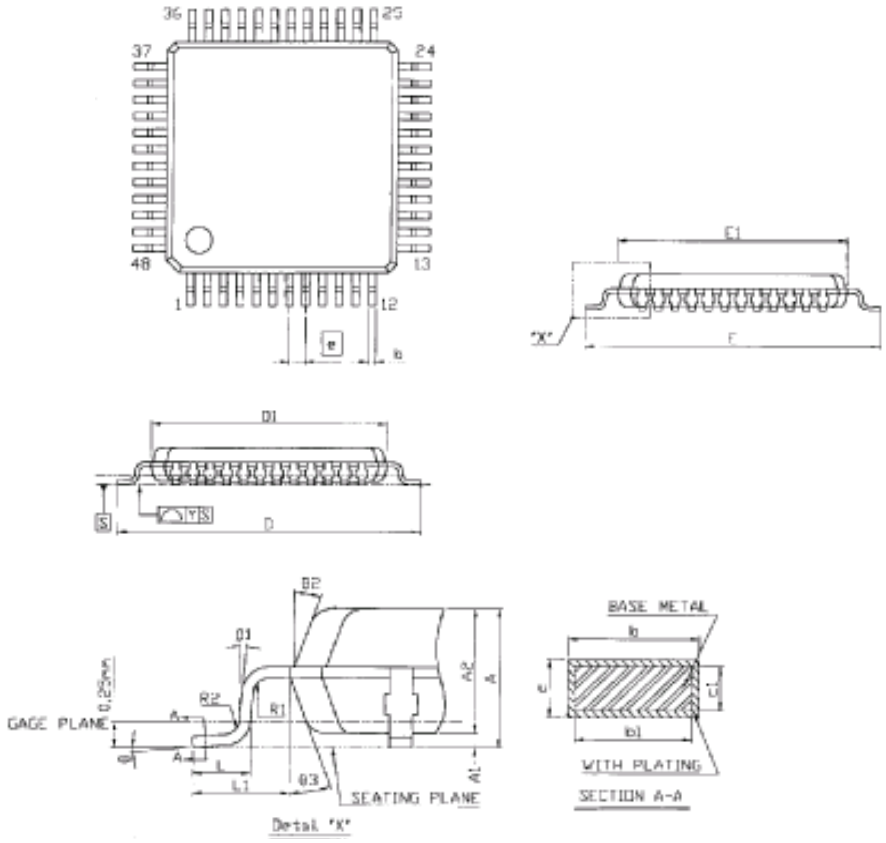
	Max	Min	Unit
T1	8		ns
T2	3		ns
T3		8	ns

7.6.2 Relationship between mode change and other input signals



	Max	Min
T5		4T
T6		4T

8. Package Dimension



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.50 BSC			20 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

Note:
1. REFER TO JEDEC MS-026 / BBC.
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4. ALL DIMENSIONS IN MILLIMETERS.

9. Revision History

Version	Description	Date
1.0	First draft	2001/05/30
1.1	1. Added Function Description of transmitting and receiving operations of UTMI transceiver. 2. Added Electrical Characteristics including timing chart. 3. Eliminated Application Circuit for different publication.	2001/08/02
1.2	1. Modify DC Characteristics of D+/D- 2. Added Operating & Suspend Current	2002/8/2
1.3	Update package information: 7mm * 7mm	2003/2/25

