Genesys Logic, Inc.

GL816

USB 2.0
Flash Card Reader Controller

Datasheet
Revision 1.31
Sep. 29, 2003

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Revision History

Revision	Date	Description
1.00	05/10/2002	First draft release
1.10	07/17/2002	Change the package from QFP128 to LQFT 128
1.20	09/20/2002	Add package information data
1.30	08/11/2002	Add chapter 8 Ordering Information
1.31	09/29/2003	Add disclaimer about X-D Picture license

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CHAPTER 1 GENERAL DESCRIPTION

The GL816 is a highly integrated, flexible application USB 2.0 Multi-Interface Flash Card Reader controller. It supports USB 2.0 high-speed transmission to PCMCIA, CompactFlash ™ (CF), Micro Drive, SmartMedia™ (SM), Secure Digital ™ (SD), Multi Media Card ™ (MMC), and MemoryStick ™ (MS) interface on one chip. Besides the flash card interface controller each, the GL816 integrates Genesys Logic own design USB 2.0 high-speed UTMI (**U**SB 2.0 **T**ransceiver **M**acrocell **I**nterface) transceiver. As a single chip solution for USB 2.0 multi flash card reader, the GL816 complies with Universal Serial Bus specification rev. 2.0, USB Storage Class specification ver.1.0, and flash card interface specification each.

The GL816 can support different kinds of multi-interface combinations. For the best performance consideration, the GL816 integrates high efficiency card interface hardware engine for data transfer, and the 48MHz feature-enhanced 8051 micro-controller. The GL816 also supports firmware upgrade via USB interface, and external flash read/ write for firmware upgrade and other applications. With the advanced mobile consideration in the IA application, the GL816 can support **Inter-Media** transfer, it means that the data transfer between different cards doesn't need the support of USB host in PC system.

The GL816 equips dedicated power control pins for different cards and power / busy indication. And the pin assignment design fits to card sockets to provide easier PCB layout. With 8 additional GPIOs, and firmware controllable CD, CE pins, the GL816 can be programmed to fit your various design in USB 2.0 high speed multi-interface flash card reader applications.

CHAPTER 2 FEATURES

- Supports PCMCIA, CompactFlash™ (CF), SmartMedia™ (SM), MemoryStick™ (MS), Secure Digital™ (SD) and Multi Media Card™ (MMC) interface on one chip.
- Complies with 480Mbps Universal Serial Bus specification rev. 2.0.
- Complies with USB Storage Class specification rev. 1.0. (Bulk only protocol).
- Operating System supported: Win XP/ 2000/ Me/ 98/ 98SE; Mac OS 9.x/ X.
- Supports 1 device address and up to 10 endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/ Interrupt (3), and 3 optional Bulk Read/ Write endpoints pair.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Integrated 8051 micro-controller with enhanced feature:
  - Supports 48MHz clock rate.
  - 12 clocks per instruction cycle.
  - Embedded 24KB Mask ROM and 2KB+256B SRAM.
  - Supports external 64KB ROM/ Flash for design flexibility.
- Supports firmware upgrade via USB interface.
- Supports external flash read/ write for firmware upgrade and other applications.
- Supports serial EEPROM 93C86 interface for the flexibility of vendor or firmware parameters, EEPROM size up to 2KB.
- High efficiency card interface hardware engine for data transfer.
- Shared pins between PCMCIA and SmartMedia™ interface.
- PCMCIA interface:
  - Supports address up to 16 bits, with fix and incremental mode.
  - Supports 8 / 16 bit data mode and different timing.
  - Supports WAIT# detection.
  - Supports multi signal level (3.3 / 5V).
  - Other control signals like CD1#, CD2#, CE1#, CE2# … etc.
- SmartMedia™ interface:
  - Supports address up to 4 bytes, 8 bit data width and different speed.
  - Supports different page size, and automatic append redundant area data (8/16 bytes).
  - Hardware ECC generation and verification.
  - Supports firmware correct page ECC error capability.
  - Supports automatic page copy (source page read + destination page write).
- MemoryStick™ interface:
  - Complies with MemoryStick interface specification.
  - Supports hardware BS/SDIO/SCLK signals.
  - Supports INS signal.
  - Supports automatic CRC16 generation and verification.
  - Supports hardware CMD timeout detection.
  - Supports different clock rate up to 24 MHz.
- Secure Digital™/ Multi Media Card™ interface:
  - Complies with Secure Digital / MMC interface specification.
  - Supports both SD / MMC mode access: CLK/CMD/DAT0/DAT1/DAT2/DAT3.
  - Command transmit and response receive can be enabled separately.
  - Automatic CRC7 generation for command and CRC7 verification for response on CMD.

  - Supports automatic CRC16 generation and verification on DAT3-0.
  - In addition to full packet transaction, optional single byte/ bit operation on both CMD and DAT line/ lines.
  - Data processing in block or byte.
  - Supports different clock rate from 375 KHz to 24 MHz.

- Dedicated power control pins for different cards and power / busy indication.
- Build-in power-on reset (POR) and low-voltage detector (LVD).
- 3.3 Volt operation.
- Pin assignment fits to card sockets to provide easier PCB layout.
- Supports 8 additional GPIOs and firmware controllable CD, CE pins.
- Available in 128-pin LQFP package.

CHAPTER 3 BLOCK DIAGRAM

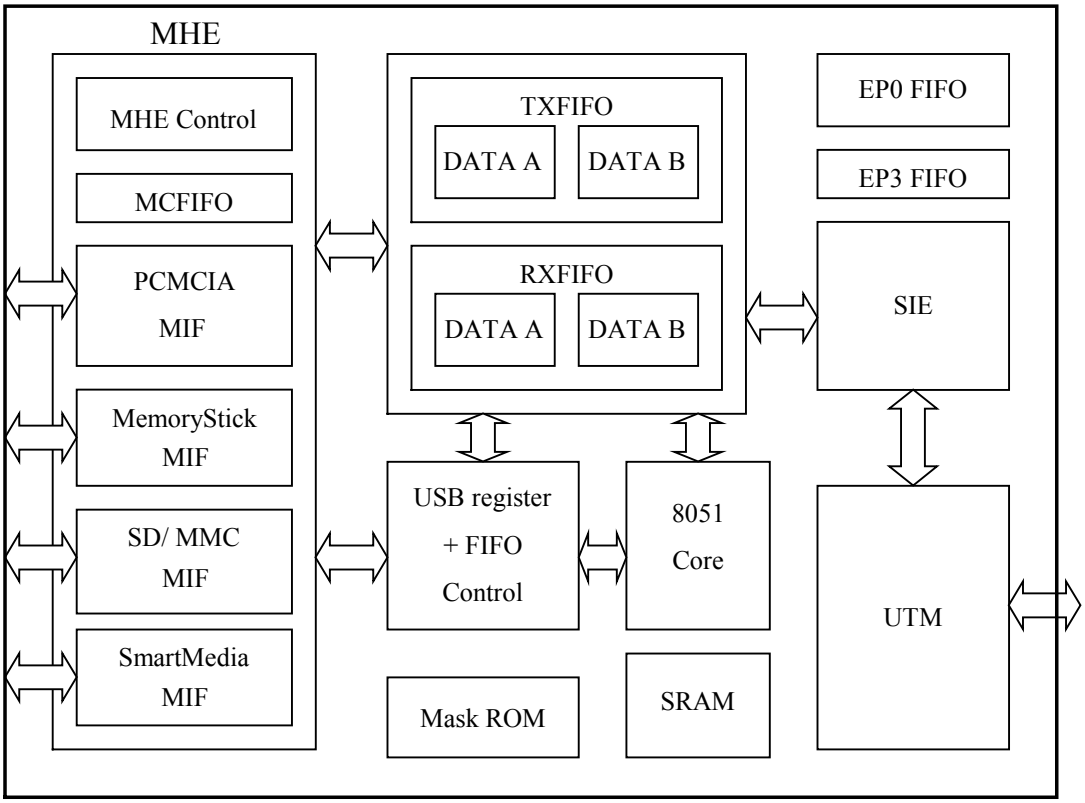


Figure 3.1 - Block Diagram

CHAPTER 4 PIN ASSIGNMENT

4.1 Pinouts

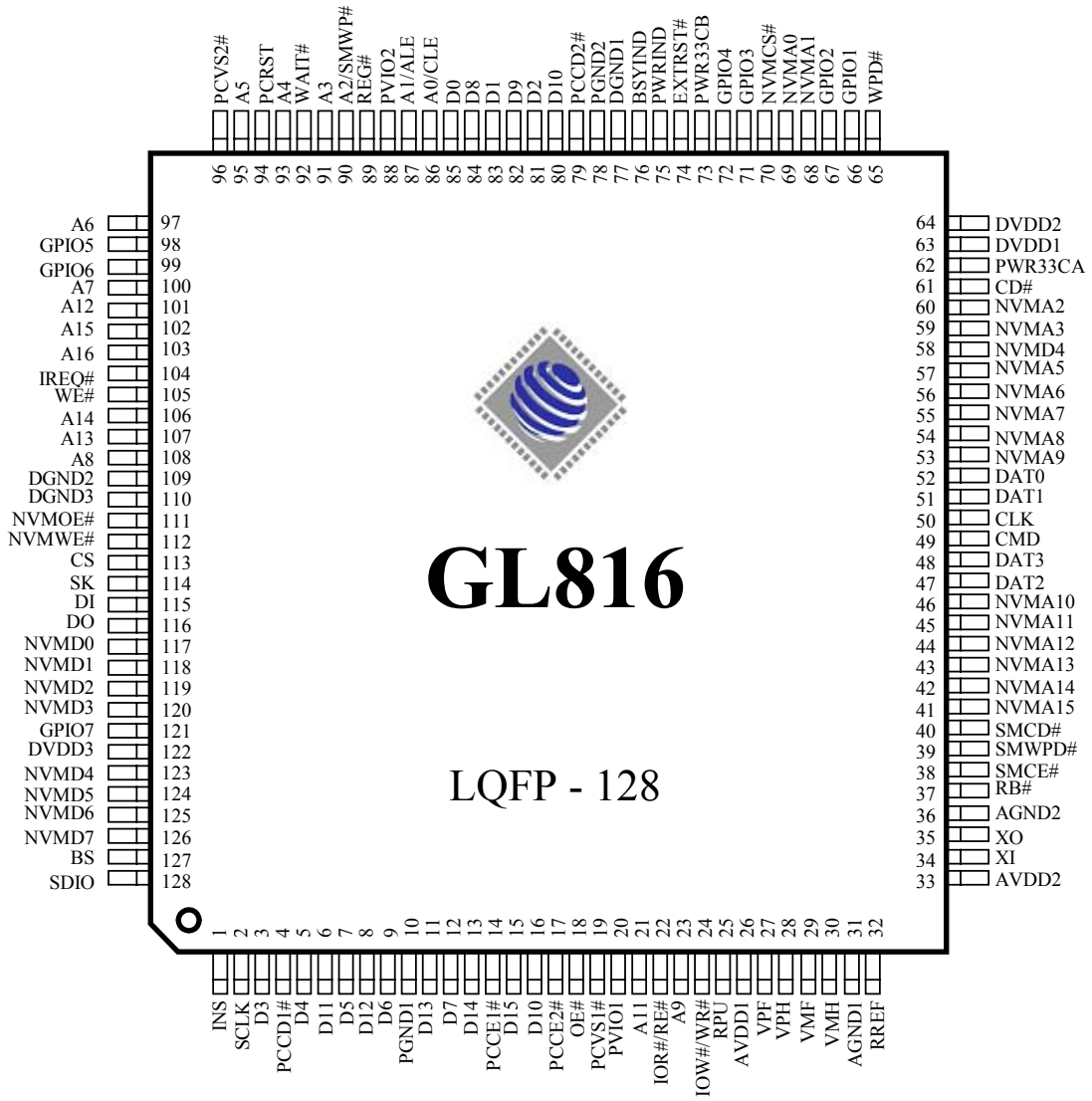


Figure 4.1 - Pinout Diagram

4.2 Pin List

Table 4.1 - Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	INS	B/I	33	AVDD2	P	65	WPD#	B/I	97	A6	O
2	SCLK	O	34	XI	I	66	GPIO1	B	98	GPIO5	B
3	D3	B	35	XO	B	67	GPIO2	B	99	GPIO6	B
4	PCCD1#	B/I	36	AGND2	P	68	NVMA1	O	100	A7	O
5	D4	B	37	RB#	B/I	69	NVMA0	O	101	A12	O
6	D11	B	38	SMCE#	B/O	70	NVMCS#	O	102	A15	O
7	D5	B	39	SMWPD#	B/I	71	GPIO3	B	103	A16	O
8	D12	B	40	SMCD#	B/I	72	GPIO4	B	104	IREQ#	B/I
9	D6	B	41	NVMA15	O	73	PWR33CB	O	105	WE#	O
10	PGND1	P	42	NVMA14	O	74	EXTRST#	I	106	A14	O
11	D13	B	43	NVMA13	O	75	PWRIND	O	107	A13	O
12	D7	B	44	NVMA12	O	76	BSYIND	O	108	A8	O
13	D14	B	45	NVMA11	O	77	DGND1	P	109	DGND2	P
14	PCCE1#	B/O	46	NVMA10	O	78	PGND2	P	110	DGND3	P
15	D15	B	47	DAT2	B/SO	79	PCCD2#	B/I	111	NVMOE#	O
16	A10	O	48	DAT3	B/SO	80	D10	B	112	NVMWE#	O
17	PCCE2	B/O	49	CMD	B/SO	81	D2	B	113	CS	O
18	OE#	O	50	CLK	O	82	D9	B	114	SK	O
19	PCVS1#	B/I	51	DAT1	B/SO	83	D1	B	115	DI	O
20	PVIO1	P	52	DAT0	B/SO	84	D8	B	116	DO	I/SO
21	A11	O	53	NVMA9	O	85	D0	B	117	NVMD0	B
22	IOR#/RE#	O	54	NVMA8	O	86	A0/CLE	O	118	NVMD1	B
23	A9	O	55	NVMA7	O	87	A1/ALE	O	119	NVMD2	B
24	IOW#/WR#	O	56	NVMA6	O	88	PVIO2	P	120	NVMD3	B
25	RPU	A	57	NVMA5	O	89	REG#	B/O	121	GPIO7	B
26	AVDD1	P	58	NVMA4	O	90	A2/SMWP#	O	122	DVDD3	P
27	VPF	B	59	NVMA3	O	91	A3	O	123	NVMD4	B
28	VPH	B	60	NVMA2	O	92	WAIT#	I/SO	124	NVMD5	B
29	VMF	B	61	CD#	B/I	93	A4	O	125	NVMD6	B
30	VMH	B	62	PWR33CA	O	94	PCRST	B	126	NVMD7	B
31	AGND1	P	63	DVDD1	P	95	A5	O	127	BS	O
32	RREF	A	64	DVDD2	P	96	PCVS2#	B/I	128	SDIO	B

4.3 Pin Descriptions

Table 4.2 - Pin Descriptions

USB Interface			
Pin Name	**Pin#**	**Type**	**Description**
RPU	25	A	USB resistor pull up
VPF	27	B	FS D+
VPH	28	B	HS D+
VMF	29	B	FS D-
VMH	30	B	HS D-
RREF	32	A	Reference resistor
XI	34	I	Crystal input
XO	35	B	Crystal output
NVMA15~0	41~46, 53~60, 68,69	O	Ext. flash address 15~0
NVMCS#	70	O (pu)	Ext. flash CS#
EXTRST#	74	I (pu)	External reset
PWRIND	75	O (pd)	Power indicator
BSYIND	76	O (pd)	Busy indicator
NVMOE#	111	O	Ext. flash OE#
NVMWE#	112	O	Ext. flash WE#
NVMD0~7	117~120, 123~126	B (pd)	Ext. flash Data 0~7

Memory Interface			
Pin Name	**Pin#**	**Type**	**Description**
INS	1	B/I (pu)	Memory Stick INS
SCLK	2	O	Memory Stick SCLK
D3	3	B	PCMCIA data 3 / SmartMedia data 3
PCCD1#	4	B/I	PCMCIA CD1#
D4	5	B	PCMCIA data 4 / SmartMedia data 4
D11	6	B	PCMCIA data 11
D5	7	B	PCMCIA data 5 / SmartMedia data 5
D12	8	B	PCMCIA data 12

D6	9	B	PCMCIA data 6 / SmartMedia data 6
D13	11	B	PCMCIA data 13
D7	12	B	PCMCIA data 7 / SmartMedia data 7
D14	13	B	PCMCIA data14
PCCE1#	14	B/O (pu)	PCMCIA CE1#
D15	15	B	PCMCIA data 15
A10	16	O	PCMCIA address 10
PCCE2#	17	B/O (pu)	PCMCIA CE2#
OE#	18	O	PCMCIA OE#
PCVS1#	19	B/I	PCMCIA VS1# ATAPI DMARQ
A11	21	O	PCMCIA address 11
IOR#/RE#	22	O	PCMCIA IOR# / SmartMedia RE#
A9	23	O	PCMCIA address 9
IOW#/WR#	24	O	PCMCIAIOW# / SmartMedia RE#
RB#	37	B/I (pu)	SmartMedia RDY/BSY#
SMCE#	38	B/O (pu)	SmartMedia CE#
SMWPD#	39	B/I (pu)	SmartMedia Write Protect Detect
SMCD#	40	B/I (pu)	SmartMedia CD#
DAT2	47	B/SO (pu)	SD DAT2
DAT3	48	B/SO (pu)	SD DAT3
CMD	49	B/SO (pu)	CD/MMC CMD
CLK	50	O	SD/MMC CLK
DAT1	51	B/SO (pu)	SD DAT1
DAT0	52	B/SO (pu)	SD/MMC DAT0
CD#	61	B/I (pu)	SD/MMC CD #
PWR33CA	62	O (pd)	PCMCIA 3.3V power control
WPD#	65	B/I (pu)	SD/MMC Write Protect Detect
PWR33CB	73	O	Card 3.3V power control
PCCD2#	79	B/I	PCMCIA CD2#
D10	80	B	PCMCIA data 10
D2	81	B	PCMCIA data 2 / SmartMedia data 2

D9	82	B	PCMCIA data 9
D1	83	B	PCMCIA data 1 / SmartMedia data 1
D8	84	B	PCMCIA data 8
D0	85	B	PCMCIA data 0 / SmartMedia data 0
A0/CLE	86	O	PCMCIA address 0 / SmartMedia CLE
A1/ALE	87	O	PCMCIA address 1 / SmartMedia ALE
REG#	89	B/O (pu)	PCMCIA REG#
A2/SMWP#	90	O	PCMCIA address 2 / SmartMedia WP#
A3	91	O	PCMCIA address 3
WAIT#	92	I/SO (pu)	PCMCIA WAIT#
A4	93	O	PCMCIA address 4
PCRST	94	B (pd)	PCMCIA reset
A5	95	O	PCMCIA address 5
PCVS2#	96	B/I (pu)	PCMCIA VS2#
A6	97	O	PCMCIA address 6
A7	100	O	PCMCIA address 7
A12	101	O	PCMCIA address 12 / ATAPI DMACK#
A15	102	O	PCMCIA address 15
A16	103	O	PCMCIA address 16
IREQ#	104	B/I (pu)	PCMCIA IREQ#
WE#	105	O	PCMCIA WE#
A14	106	O	PCMCIA address 6
A13	107	O	PCMCIA address 6
A8	108	O	PCMCIA address 6
BS	127	O	MemoryStick BS
SDIO	128	O (pd)	MemoryStick SDIO

EEPROM Interface			
Pin Name	**Pin#**	**Type**	**Description**
CS	113	O	93C86 CS
SK	114	O	93C86 Clock
DI	115	O	93C86 Data in
DO	116	I/SO	93C86 Data ouot

Miscellaneous Interface			
Pin Name	**Pin#**	**Type**	**Description**
GPIO1	66	B (odpu)	GPIO1
GPIO2	67	B (odpu)	GPIO2
GPIO3	71	B (odpu)	GPIO3
GPIO4	72	B (odpu)	GPIO4
GPIO5	98	B (odpu)	GPIO5
GPIO6	99	B (odpu)	GPIO6
GPIO7	121	B (odpu)	GPIO7

Power / Ground			
Pin Name	**Pin#**	**Type**	**Description**
PGND1	10	P	Pad GND #1
PVIO1	20	P	Power (5 / 3.3V) for pin 3-24
AVDD1	26	P	Analog VDD #1
AGND1	31	P	Analog GND #1
AVDD2	33	P	Analog VDD #2
AGND2	36	P	Analog GND #2
DVDD1	63	P	Digital VDD #1
DVDD2	64	P	Digital VDD #2
DGND1	77	P	Digital GND #1
PGND2	78	P	Pad GND #2
PVIO2	88	P	Power (3.3 / 5V) for pin 79-108
DGND2	109	P	Digital GND #2
DGND3	110	P	Digital GND #3
DVDD3	122	P	Digital VDD #3

Notation:

Type	**O**	Output
	I	Input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull up
	pd	Internal pull down
	odpu	Open drain with internal pull up

CHAPTER 5 FUNCTIONAL DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0 FIFO

It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

5.4 EP3 FIFO

It's an 8-byte FIFO for endpoint 3.

5.5 Bulk FIFO

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

TXFIFO:

1. To ensure the continuous data transmission, TXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and two 16 bytes corresponding redundant areas. All can be directly accessed by 8051 μC.
2. Normally SIE popes data, MHE pushes data for DATA A/B FIFOs, and redundant area is pushed by MHE when SmartMedia MIF is enabled and popped by uC.
3. Supports uC single byte access for SmartMedia ECC error correction.
4. At transmit mode SIE won't transmit data filled in TXFIFO before uC complete the data integrity checking.

RXFIFO:

1. To ensure the continuous data transmission, RXFIFO includes 512 bytes DATA-A FIFO, 512 bytes DATA-B FIFO, and 16 bytes single redundant area. All can be directly accessed by 8051 μC.
2. Normally MHE popes data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by uC and popped by MHE when SmartMedia MIF is enabled.

Buffer Mode:

1. Buffer mode is enabled by firmware and is used to copy data block from source to destination in same card for SmartMedia or MemoryStick applications.
2. Under Buffer mode, firmware can enable MIF to read source data block to TXFIFO, check the data integrity, then enable MIF to write data in TXFIFO to destination data block space on memory card.
3. For SmartMedia application, the redundant data write to destination data block space is from redundant area of RXFIFO.

5.6 MHE (Media Hardware Engine)

The Media Hardware Engine contains 4 MIF (Media Interface), MHE control and MCFIFO.

1. **MIF (Media Interface):** There are PCMCIA MIF, SmartMedia MIF, MemoryStick MIF, and Secure Digital/ Multi Media Card MIF in MHE.
2. **MCFIFO (Media Control FIFO):** It's a 64-byte FIFO that shared by MemoryStick and SD/ MMC MIF. In MemoryStick application, the MCFIFO is used for register read and write function; In SD/ MMC application, it is used for command and response.
3. **SMAFIFO (SmartMedia™ Address FIFO):** It's a 4-byte FIFO for SmartMedia address only.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Absolute Maximum Ratings

Parameter	Value
Ambient Temperature under bias (T_A)	0°C to 70°C
Supply Voltage	+3.0V to +3.6V
Ground Voltage	0V
F_{OSC}	12 MHz ± 100ppm

6.2 DC Characteristics

Table 6.2 - DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		3.0		3.6	V
V_{IH}	Input High Voltage		2.6		5	V
V_{IL}	Input Low Voltage		0.0		0.7	V
I_I	Input Leakage current	$0 < V_{IN} < V_{CC}$				µA
V_{OH}	Output High Voltage		3.0			V
V_{OL}	Output Low Voltage				0.2	V
I_{OH}	Output Current High					mA
I_{OL}	Output Current Low					mA
C_{IN}	Input Pin Capacitance				2.0	pF
I_{SUSP}	Suspend current	1.5K external pull-up included				µA
I_{CC}	Supply current	Connect to USB with 8051 operating				mA

6.3 AC Characteristics

6.3.1 UTMI Transceiver

The GL816 is fully compatible with Universal Serial Bus specification rev. 2.0 and USB 2.0 Transceiver Macercell Interface (UTMI) specification rev. 1.01. Please refer to the specifications for more information.

6.3.2 External Flash

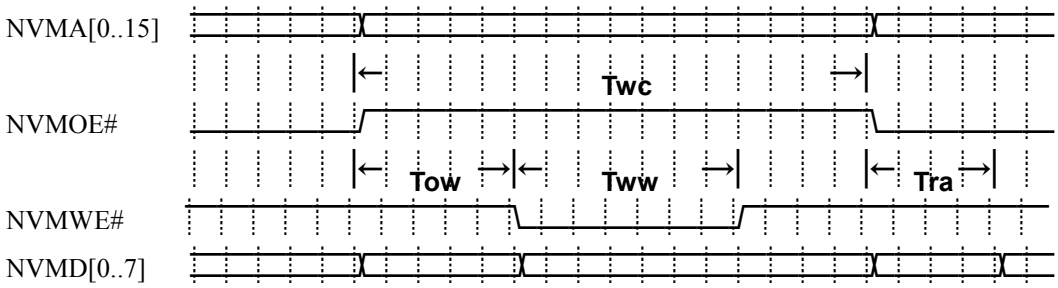
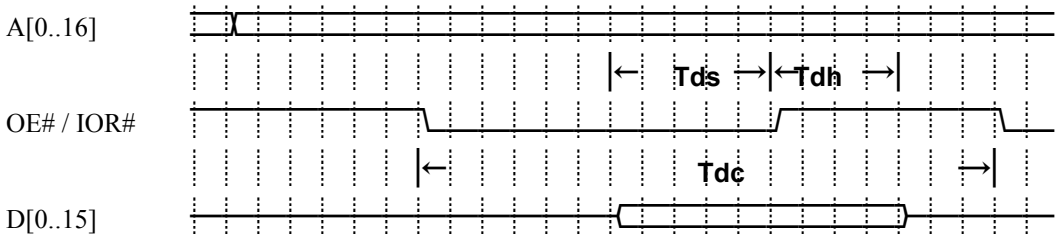


Figure 6.1 - Timing Diagram of External Flash

Parameter	Description	Min	Typ	Max	Unit
T_{WC}	Write data cycle time		102.5		ns
T_{WW}	Write pulse width		41.6		
T_{OW}	OE# to WE# time		38.6		
T_{RA}	Read Access time			90	

6.3.3 PCMCIA

Read



Write

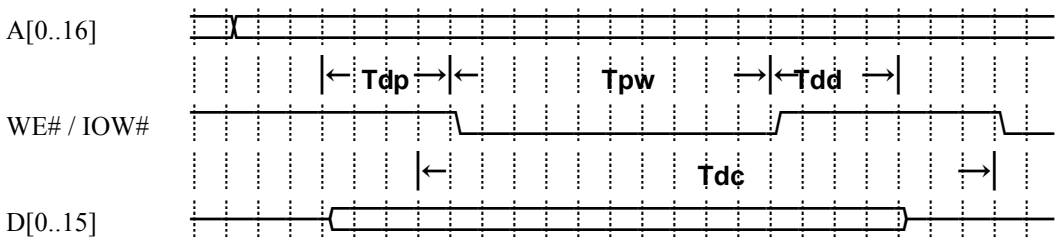
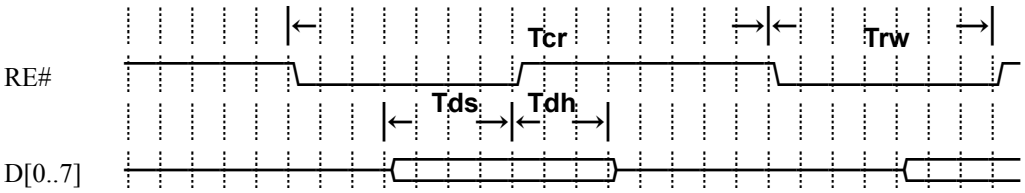


Figure 6.2 - Timing Diagram of PCMCIA

Parameter	Description	Mode	Min	Typ	Max	Unit
Tds	Data setup time (read)	0, 1		88.3		ns
		2, 3		38.3		
Tdh	Data hold time (read)	0, 1		2		
		2, 3		2		
Tdc	Access cycle time (read/write)	0		666.4		
		1		416.5		
		2		222.1		
		3		166.5		
Tpw	Control pulse width (read/write)	0		333.2		
		1		166.6		
		2		133.2		
		3		66.6		
Tdp	Data pre-output time (write)	0, 1		26.6		
		2, 3		1.6		
Tdd	Data delay time (write)	0, 1		41.6		
		2, 3		16.6		

6.3.4 SmartMedia

Read



Write

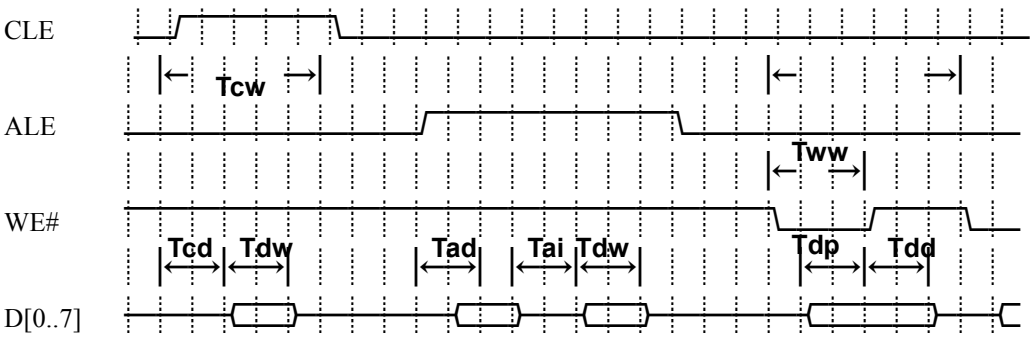


Figure 6.3 - Timing Diagram of SmartMedia

Parameter	Description	Mode	Min	Typ	Max	Unit
Tcw	CLE active width	Normal		165		ns
		Slow		198		
Twc	Write data cycle time	Normal		100		
		Slow		166		
Tww	Write pulse width	Normal		66		
		Slow		100		
Tcd	CLE-to-command delay			33.3		
Tdw	Data width	Normal		67		
		Slow		100		
Tad	ALE-to-address delay			33.3		
Tai	Address data interval time			33.3		
Tdp	Data pre-output delay			33.3		
Tdd	Data delay time			33.3		
Tcr	Read data cycle time	Normal		133.3		
		Slow		166.6		
Trw	Read pulse width			100		
Tds	Data setup time			40		
Tdh	Data hold time			2		

6.3.5 Memory Stick

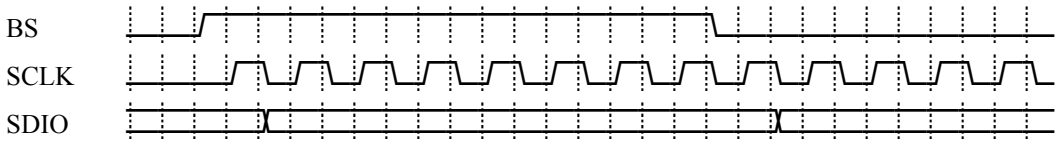


Figure 6.4 - Timing Diagram of MemoryStick

Parameter	Description	Mode	Typ	Unit	Remark
Fck	SCLK frequency	0	1.5M	Hz	
		1	6M		
		2	15M		
		3	24M		

6.3.6 Secure Digital / MultiMedia Card

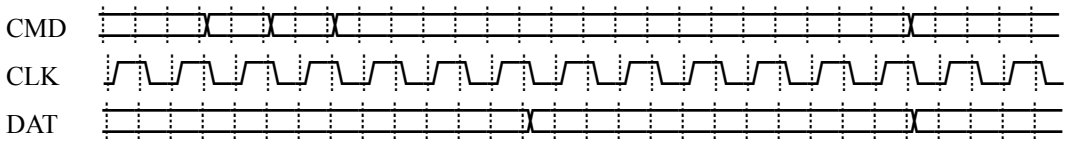
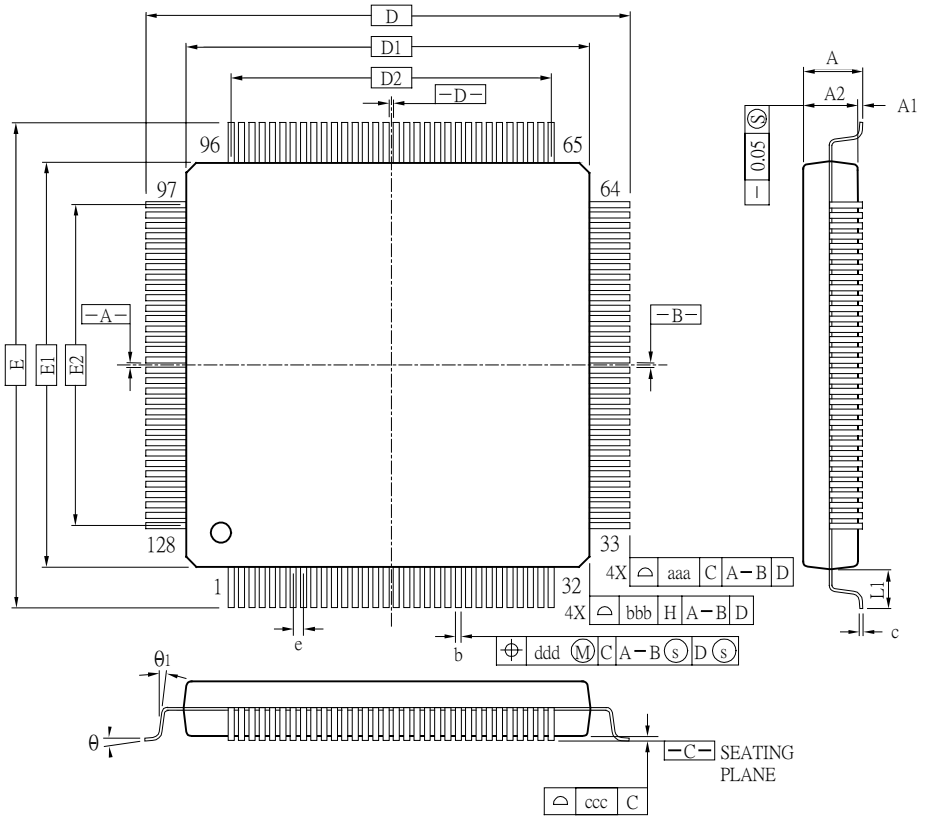
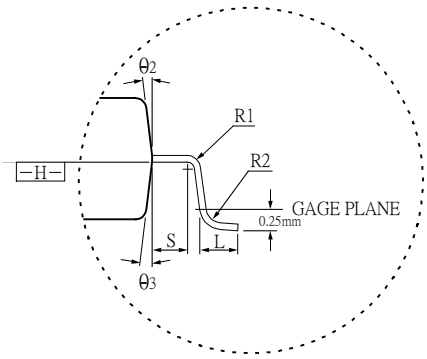


Figure 6.5 - Timing Diagram of SD / MMC Interface

Parameter	Description	Mode	Typ	Unit	Remark
Fck	CLK frequency	0	375K	Hz	
		1	6M		
		2	15M		
		3	24M		

CHAPTER 7 PACKAGE DIMENSION





NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	16.00 BASIC			0.630 BASIC		
E	16.00 BASIC			0.630 BASIC		
D1	14.00 BASIC			0.551 BASIC		
E1	14.00 BASIC			0.551 BASIC		
D2	12.40 BASIC			0.488 BASIC		
E2	12.40 BASIC			0.488 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BASIC			0.016 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Figure 7.1 - GL816 128 Pin LQFP Package

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Status
GL816	128-pin LQFP	

