TEXAS INSTRUMENTS

GS20 0.18-μm CMOS Standard Cell/Gate Array

Version 1.1

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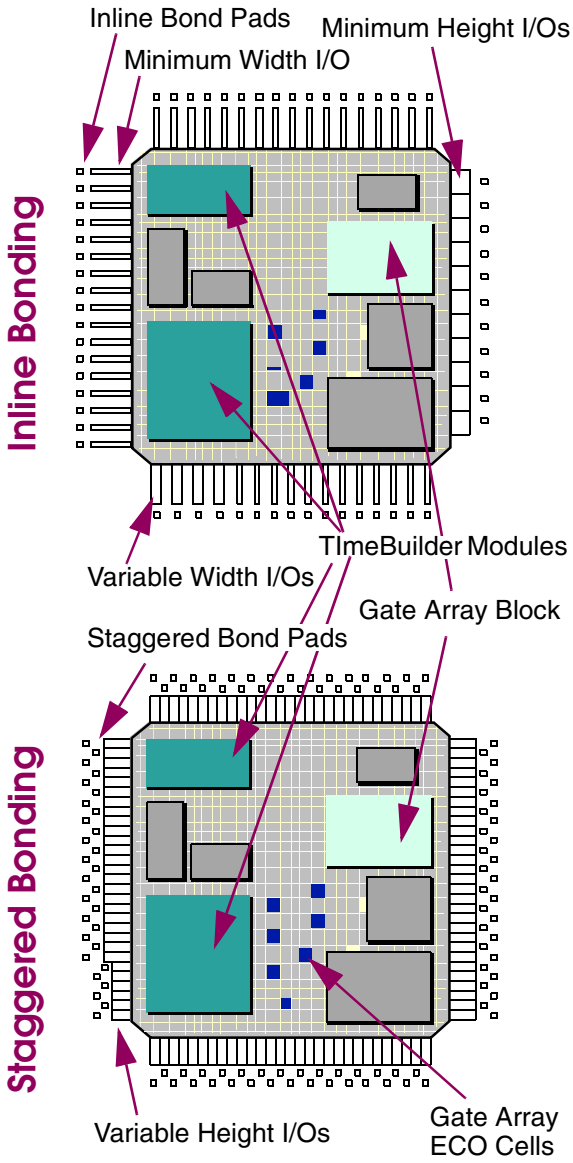
GS20 0.18-µm CMOS Standard Cell/Gate Array

Overview

- **0.18-µm Leff process** with Shallow Trench Isolation (STI)
- **4 and 5 levels of metal**
- **Density:** 36,000 gates/mm^2 at 50K gates (QLM)
- **3 million random logic gates** plus 3 million equivalent gates in TImeBuilder™ modules and memory
- **Power supply:** 1.1/1.4/1.8 V cores
  I/Os: 1.4/2.5/3.3 V (selected combinations)
  5 V-tolerant, failsafe
- **Power dissipation:** 0.025 µW/MHz/gate for 1.8 V core
- **Multi-gigabit** serial link transceiver technology
- **More than 450 core cells**
- **Over 250 peripheral macros,** including LVCMOS, PCI, differential, level-shifting I/Os, ATA, PCML, CML, DPECL, LVDS, HSTL, SSTL, TTL, TLV, oscillators
- **Extensive module selection**, including TMS 320 digital signal processors (DSPs), ARM™ 32-bit RISC microcontrollers, JADE embedded MIPS® processor and analog functions
- **Memory compilers** including single-port, two-port, dual-port, three-port, ROM, CAM, and register file, synthesizable memories
- **TI ExSRAM** extremely high-density SRAM (>3 Mb of memory on a die)
- **Electrically-readable** die ID
- **Spare gate-array cells and gate-array blocks** for fast metal-level ECO
- **Packages:** TQFP, JEDEC metric QFP with and without heat spreader, EIAJ QFP, MicroStar™ BGA, plastic BGA, Super BGA, Generic BGA, PowerPad



Major Product Characteristics

Nominal core voltage	I/O voltage	Typical gate delay NA210, FO = 2	Typical design power dissipation
1.8 V	1.8, 2.5, 2.75, 3.3, 5.0	75 ps	0.025 µW/MHz/gate
1.4 V	1.4, 1.8, 2.5, 2.75, 3.3	119 ps	0.010 µW/MHz/gate
1.1 V	1.1, 1.4, 1.8, 2.5, 2.75, 3.3	159 ps	0.008 µW/MHz/gate

Features and Benefits

Features	Benefits
High-density product	Reduces die size and power
High-performance macros	Designed to meet telecom and networking needs
Five-level metal for power	Provides high-power design support
Four-level metal	Reduces die size and power
Low-power macros	Reduces chip power
Clock tree synthesis	Flexible, low-power clock strategy. Support for high number of clocks. Allows gated clock domains for power reduction.
Variety of analog cells	System integration
Dense memories	Reduces die size
Core integration (DSP, microcontroller)	System integration
VHDL, Verilog™, QuickSim II™ signoff flows	Reduces cycle time and improves accuracy
1.1-, 1.4-, and 1.8-V core libraries	Speed/power trade-offs
Automated spare gate/cell insertion of programmable base cells and all-level cells in the core	Flexibility in making top-level changes late in the design cycle
Synopsys™ Power Compiler™ support	Power reduction
Static timing analysis (STA) signoff	Comprehensive verification and less QC effort at design hand-off

Description

The GS20 ASIC product family is the first to use the new Texas Instruments TImeCell™ Architecture, which combines on the same silicon the cost-efficiency of standard cells with the fast time-to-market of gate arrays. Texas Instruments (TI™) provides a full range of product options to address the challenges of producing ultra high density, low power devices that take advantage of system integration. These options include:

- **4 and 5 levels of metal** with full Chemical Mechanical Polishing (CMP) planarization and fully stacked Tungsten vias
- **A wide variety of core macros**, including cells designed especially to meet high-performance requirements
- **A full range of inputs/outputs** (I/Os) in many specifications and voltages, including LVDS, HSTL, CML, 5-V I/Os, and SSTL
- **A broad selection of memory compilers**, including synthesizable RAMs for more area efficiency in small RAM configurations
- **Fully characterized libraries** that enable accurate modeling
- **TImePilot™ design system**, which offers a multi-EDA-vendor strategy that supports industry standards. This system, combined with enhancements in the design flow, simplifies and speeds the design process. See Table 8 on page 18 for a list of supported CAD tools.
- **TImeBuilder module library** containing modules for processors and peripherals (including TMS320C54X DSP; ARM 32-bit RISC, MIPS 32- and 64-bit, and NEC v850 microcontrollers); mixed signal (analog-to-digital converters, digital-to-analog converters); communications (including UART, USART, 10/100 Ethernet MAC, single-channel HDLC); and interface (such as IrDA, 32-bit/33 MHz PCI bus, USB controller).
- **A wide range of package options** for flexibility in cost-effectiveness, density and performance. These include thin quad flat pack (TQFP), JEDEC metric QFP with heat spreader, EIAJ QFP, MicroStar™ BGA, Plastic BGA, Super BGA, PowerPad, and Generic BGA. For more details, see Table 7 on page 13.
- **Clock tree synthesis (CTS)** design flow that provides automatic synthesis of clock trees in physical design to meet designers' skew and insertion delay goals. The TI CTS flow supports more than 200 clock domains and clock gating for low power, and consistently achieves less than 50 ps clock skew.
- **Complete STA signoff methodology** enables comprehensive verification and minimizes gate-level simulation efforts at design hand-off. The Synopsys PrimeTime™-based signoff flow is supported with delay fault test generation capability using Sunrise™ tools.
- **SubChip™** design capabilities that support reuse
- **Sprinkled gate array cells** and gate array blocks for fast metal-level design changes

Core and I/O Macro Summary

This summary of core and I/O macros lists the selections available from the library.

Performance Equations

Every timing path through each GS20 family core and I/O macro is characterized at multiple voltage, temperature, process, input slew, and output load points. No global derating with respect to voltage, temperature, or process is used with the GS20 family. The characterized data coupled with nonlinear delay modeling allows SPICE-like accuracy for a large range of operating conditions.

Library Description

The GS20 family macro library has been optimized for use with synthesis and power optimization tools. Data from over 200 synthesized designs was analyzed to determine high-usage macros. In addition, a team of TI engineers worked closely with leading synthesis vendors to determine an optimal cell set. As a result, the GS20 family library features:

- A rich set of Boolean functions
- A wide variety of gates with inverting inputs
- Multiple-drive-strength gates
- Compact flip-flops and latches with Q only or QZ only
- Low-power combinational cells
- Minimized internal transistors in multistage macros
- Ultra-high-performance flip-flop and core macros
- Negative-edge flip-flops

A summary of core functions is shown in Table 1 on page 5.

Table 1: GS20 Family Core Macro Library Summary

Function	Number of macros
Datapath	11
AND/NAND/OR/NOR	76
Exclusive-OR/Exclusive-NOR	6
Inverters	12
Buffers	15
Boolean functions	63
Multiplexers	19
D-type flip-flops	51
Latches	21
Scan flip-flops/latches	78
PMT functions and JTAG	5
Clock generators	8
Analog functions	17
Special functions/miscellaneous	21
Total	**403**

Analog functions include an 8-bit analog-to-digital converter (pipeline), a 10-bit successive approximation register (SAR), an analog clock squarer, a 10-bit digital-to-analog converter, and a low frequency analog differential receiver/comparator. The special function macros include two electrically-readable die ID fuse array macros.

Gate Array Macros

The GS20 macro library also includes gate array cells for ECO as shown in Table 2 and gate array block cells as shown in Table 3.

Table 2: Gate-Array Cells for ECO

Function	Number of macros
AND	2
Buffers	8
D-type flip-flops	2
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NANDs	8
NORs	9
ORs	1
Special functions/miscellaneous	3
Total	**44**

Table 3: Gate Array Block Cells

Function	Number of macros
AND	2
OR	1
Buffers	8
D-type flip-flops	2
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NANDs	9
NORs	9
Scan flip-flops	3
Clock-tree synthesis	13
Special functions/miscellaneous	3
Total	**61**

High-Performance Macros

High-speed applications, such as synchronous digital hierarchy (SDH) and asynchronous transfer mode (ATM), require correct alignment between the data and clock signals. To ensure this data synchronization, the GS20 family provides a set of macros to build systems capable of phase alignment and digital clock recovery. These high-performance macros include:

- DLP52 bit-phase aligner, CK812B clock generator (750 MHz), and S8P20 serial-to-parallel converter, DLP53 digital clock recovery
- CK813B clock repeater - up to 750 MHz

Key product features include operating range exceeding 750 MHz, tolerance to input jitter and pulse distortion up to 30%, data out retime to system clock, and high test coverage.

The phase alignment function (DLP52, clock macro, and serial-to-parallel converter) resynchronizes off-chip data to an on-chip clock when the relationship between the two is unknown or changing over time. The phase alignment function tracks this variation and maintains data integrity in the receiving function.

The clock recovery function (CK812B, CK813B, S8P21) recovers the clock from the input data stream. The digital clock recovery (DCR) mechanism dynamically creates a clock to match the original reference clock associated with the data. The phase and the exact frequency of DATAIN may be unknown. The target frequency exceeds 750 MHz.

Other high-performance macros include:

- CML - up to 750 MHz
- GaAs - up to 750 MHz
- LVDS - up to 750 MHz
- Oscillators up to 100 MHz

I/O Macros

The GS20 product provides 1.1, 1.4, 1.8, 2.5, 2.75, 3.3, and 5 V I/Os. Low-voltage CMOS (LVCMOS), PCI, and differential buffers are available. Most output buffers are available in three noise performance options: high performance, low noise, and ultra-low noise. To minimize system noise and power pins, select the lowest noise output that the application allows. Ultra-low-noise I/Os typically require only one-fifth the number of power pins that high-performance I/Os require.

The user creates a bidirectional macro by selecting inputs and outputs and combining the functions in the netlist. Pullup and pulldown macros can also be added to I/Os in the same manner. I/O macros include:

- 1.1, 1.4, 1.8, 2.5, 2.75, 3.3, and 5-V-tolerant and failsafe I/Os
- LVCMOS, TTL, PCI, ATA
- CML, GaAs, TLV, LVDS, HSTL, SSTL, PCML, DPECL, SSTL
- High performance, low noise, ultra-low noise, ultra-low power, failsafe, and 5 V-tolerant options
- 1/1mA - 12/24mA output drivers

Table 4: I/O Specifications

Type	Maximum Frequency	Signal Swing	Signal Type
TTL/LVCMOS	200 MHz	3 V	single
CML	750 MHz	400 mV	differential
GaAs	400/622 MHz	800 mV	single & differential
TLV	250 MHz	800 mV	single & differential
LVDS	750 MHz	400 mV	differential
HSTL	400 MHz	1.5 V	single & differential
PCI	33 MHz	3 V	single
PCML	400 MHz	400 mV	single & differential
DPECL	800 MHz	800 mV	differential
ATA-66	17.3 MHz	3.3 V	single
SCSI	20 MHz	2.85 V	single
SCSI	40MHz	400 mV	differential
SSTL	125 MHz	2.5 V	single

Memories

The GS20 family supports synchronous single-port, two-port, dual-port, and three-port memory compilers as well as ROM, CAM and asynchronous two-port compilers. These dense memories allow the user to specify the exact word and bit counts for each memory to meet the application's need. All memories can have synchronous operation, zero dc power and zero hold times.

Table 5: Memories Summary

Description	Max Bits	Min Bits	Max Words	Max Bits/ Word	Functionality
1-port Clocked RAM area optimized	128K	32	2K	128	Single edge
1-port CRAM density optimized with redundancy	1M	32	32K	128	Single edge
1-port CRAM density optimized with bit-write and redundancy	1M	32	32K	128	Single edge
1-port CRAM speed optimized with redundancy	1M	4K	64K	144	Single edge
1-port CRAM speed optimized with bit-write and redundancy	1M	4K	64K	144	Single edge
1-port CRAM with multi-strobe, bit write, and redundancy	128K	512	4K	32	Single edge
2-port CRAM (1R/1W)	128K	256	8K	128	Single edge
2-port CRAM (1R/1W) area optimized	9K	4	512	72	Single edge
2-port register file (1R/1W)	8K	8	256	32	Sync write Async read
2-port SRAM (1R/1W)	32K	4	2K	64	Asynchronous
3-port CRAM (1R/2W)	147K	32	4096	128	Single edge
3-port CRAM (2R/1W)	147K	32	4096	128	Single edge
Dual-port CRAM	128K	64	4K	128	Single edge
ROM via2, density optimized	1M	64	64K	128	Single edge
ROM via2, speed optimized	1M	64	64K	128	Single edge
ROM moat, density optimized	1M	64	64K	64	Single edge
ROM moat, speed optimized	1M	64	64K	64	Single edge
CAM	128K	512	1024	128	

Single-Port Clocked SRAM Compiler

The single-port clocked SRAM compiler creates speed-optimized RAM blocks based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor. Contact the TI Customer Design Center for complete details.

Single-Port Clocked SRAM Compiler With Word-Write, Bit-Write and Multistrobe

In addition to the single-port clocked SRAM, TI also offers single-port memories with both word-write and bit-write capability. The bit-write capability enables you to update individual bits in the single port without changing the rest of the word. Multistrobe allows data to be read and/or written on up to three strobes.

Dual-Port Clocked SRAM Compiler

The dual-port clocked SRAM compiler creates area- and speed-optimized RAM based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor. Contact the TI Customer Design Center for complete details.

Synthesizable Memories

For maximum flexibility, GS20 offers a number of memory options for use as “soft,” or synthesizable, memories. This compiler generates RTL (based on your specifications) as well as constraints for synthesis. Design Compiler™ is then used to synthesize these memories to either flip-flop or latch-based implementation with support for multiple test methodologies. The compiler options are:

- 1-port CRAM area optimized
- 1-port CRAM speed optimized
- 2-port asynchronous RAM
- 2-port CRAM
- Dual-port RAM

TImeBuilder Modules

The GS20 family supports a wide variety of TImeBuilder modules targeted to integrate complex functionality onto a single die. Digital signal processor cores and microcontrollers are available for integration, among others.

Table 6: TImeBuilder Modules

Processors and Peripherals	Communications
ARM9TDMI	UART
ARM7TDMI	USART
MIPS 32- and 64-bit processor	Single-channel HDLC
NECv850	Multiple-channel HDLC
TMS320C54X	10/100 Ethernet MAC
ARM7 system bus controller	6-port 10/100 MAC with buffer memory
ARM7 peripheral bus bridge	Reed Solomon encoder/decoder
Multi-channel DMA controller	1GHz low-jitter digital clock recovery
Interrupt controller	650 MHz bit-phase aligner
Watchdog timer	622 Mb/s Serdes
16-bit timer	
Clock manager	
Configurable memory controller	
Serial port— SPI/uWire	
Mixed Signal	**Interface**
Analog-to-digital converters	IrDA
Digital-to-analog converters	I2C master/slave
	IEEE 1394 link core
	IEEE 1284 parallel port
	PCI core
	USB controller
	RAMBUS

Analog Cells

Analog cells include:

- Clock squarer with low power mode (dual gate only)
- Analog comparator
- Analog threshold cell
- Eight-bit analog-to-digital with 30 MHz minimum
- 10-bit successive approximation register (SAR) analog-to-digital converter
- 8-bit R-2R analog-to-digital converter
- 10-bit digital-to-analog video-band with 45 MHz operating frequency
- 10-bit digital-to-analog converter with 100 MHz operating frequency
- Analog phase-locked loop, 33-250 MHz, jitter <3%, three-pin implementation
- Analog phase-locked loop, 200-600 MHz, jitter <3%, three-pin implementation
- Analog phase-locked loop, 10-350 MHz, jitter <10%, three-pin implementation
- Analog input and output switches

Packaging

GS20 uses the package types shown below.

Table 7: Supported Packages

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)	Supports Staggered Bond
Thin Quad Flatpack (TQFP)	32	VF	7x 7x1.4	0.80	
	48	PFB	7x 7x1.4	0.50	
	52	PAH	10x10x1.0	0.65	
	64	PAG	10x10x1.0	0.50	
	80	PET	10x10x1.0	0.40	✓
	80	PFC	12x12x1.0	0.50	✓
	100	PZT	14x14x1.0	0.50	✓
	128	PDT	14x14x1.0	0.40	✓
	128	PEU	14x20x1.4	0.50	
	144	PGE	20x20x1.4	0.50	✓
	160	PBL	20x20x1.4	0.40	✓
	176	PBL	20x20x1.4	0.40	✓
	176	PGF	24x24x1.4	0.50	✓
	208	PDV	28x28x1.4	0.50	
	216	PDQ	24x24x1.4	0.40	✓
EIAJ QFP (EQFP)	80	PH	14x20x2.7	0.80	
	100	PJ	14x20x2.7	0.65	
	128	PGJ	14x20x2.0	0.50	
JEDEC metric QFP (JMQFP)	120	PBM	28x28x3.5	0.80	
	144	PCM	28x28x3.5	0.65	
	160	PCM	28x28x3.5	0.65	
	208	PPM	28x28x3.5	0.50	
	240	PGC	32x32x3.8	0.50	

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)	Supports Staggered Bond
	120	PBE	28x28x3.5	0.80	
JMQFP	144	PCE	28x28x3.5	0.65	
with Heat Spreader/ Slug	160	PCE	28x28x3.5	0.65	
(JMQFPHS)	208	PPE	28x28x3.5	0.50	
	240	PGV	32x32x3.8	0.50	
	64	GGV	8x 8x1.4	0.80	✓
	79	GHB	8x 8x1.4	0.8	✓
	80	GGM	10x10x1.4	0.80	✓
	100	GGM	10x10x1.4	0.80	✓
MicroStar Ball Grid Array	100	GGT	11x11x1.4	0.80	✓
(BGA)	100	GGB	12x12x1.4	0.80	✓
	128	GGB	12x12x1.4	0.80	✓
	144	GGU	12x12x1.4	0.80	✓
	176	GGW	15x15x1.4	0.80	✓
	196	GHC	15x15x1.4	1.00	✓
	208	GGW	15x15x1.4	0.80	✓
	240	GGW	15x15x1.4	0.80	✓
Plastic BGA	256	GFN	27x27	1.27	
(PBGA)	352	GFT	35x35	1.27	
PBGA-Thermal Ball	272	GFN	27x27	1.27	
(PBGA-TB)	388	GFW	35x35	1.27	
	256	GGN	27x27	1.27	
Super BGA	352	GGP	35x35	1.27	
(SBGA)	432	GGQ	40x40	1.27	
	520	GGR	40x40	1.27	
PowerPAD	52	PGP	10x10x1.0	0.65	

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)	Supports Staggered Bond
PowerPAD	64	PAP	10x10x1.0	0.50	
	80	PFP	12x12x1.0	0.50	
	100	PZP	14x14x1.0	0.50	
	128	PNP	14x14x1.0	0.40	
	144	PRP	20x20x1.4	0.50	
	176	PTP	24x24x1.4	0.50	
	208	PYP	28x28x1.4	0.50	
Generic BGA (GBGA)	672	GKP	40x40	1.27	✓
	792	GKQ	40x40	1.0	✓
	896	GKQ	40x40	1.0	✓

TImePilot Design Flow and CAD Tools

Fully characterized libraries account for the effects of voltage, temperature, process, load, and input rise and fall times. Hierarchical design viewing and editing, floorplanning, and timing analysis allow the designer to achieve the accurate representation of silicon through forward annotation of timing to the layout software. This design approach, shown in Figure 1 on page 17, gives designers full advantage of the high-performance characteristics that submicron CMOS technology offers.

The TI approach to open CAD enables easy interaction with other systems. Signoff quality libraries for all supported simulators, test vector verification software, and design rule checking software enable the customer to verify the design completely before handoff to TI, significantly shortening design cycle time and eliminating correlation issues. Cadence Leapfrog, Synopsys VSS, and Mentor Graphics QuickHDL simulation libraries conform to IEEE Std. 1076.4-1995–VITAL 95. Tools and libraries in the TImePilot design environment are supported on both Sun™ and HP™ workstations.

TImePilot uses the Avant! Planet ™ floorplanner. TI has added several features to the floorplanning flow, including a sequencer that steps users through all floorplanning-related tasks. Other features include:

- Gate-level floorplanning
- SubChips
- Clock tree synthesis
- Team design
- Delay calculation
- Global routing
- Planet placer
- Milky Way database
- Path timing-driven placement
- Power routing
- Rules-driven placement
- Floorplan checks
- Wide-wire support
- Advanced Routing Option (ARO) support
- ECO

The primary aim of the design flow is to offer state-of-the art design tools and a highly productive environment to support designers in achieving error-free designs in the shortest time. The flow is also designed to comprehend the effects of deep submicron technology by accurately estimating interconnection lengths and resistance-capacitance (RC) effects, and by providing close correlation between floorplanning and synthesis and pre- to postlayout delays.

Figure 1: Design Flow Overview

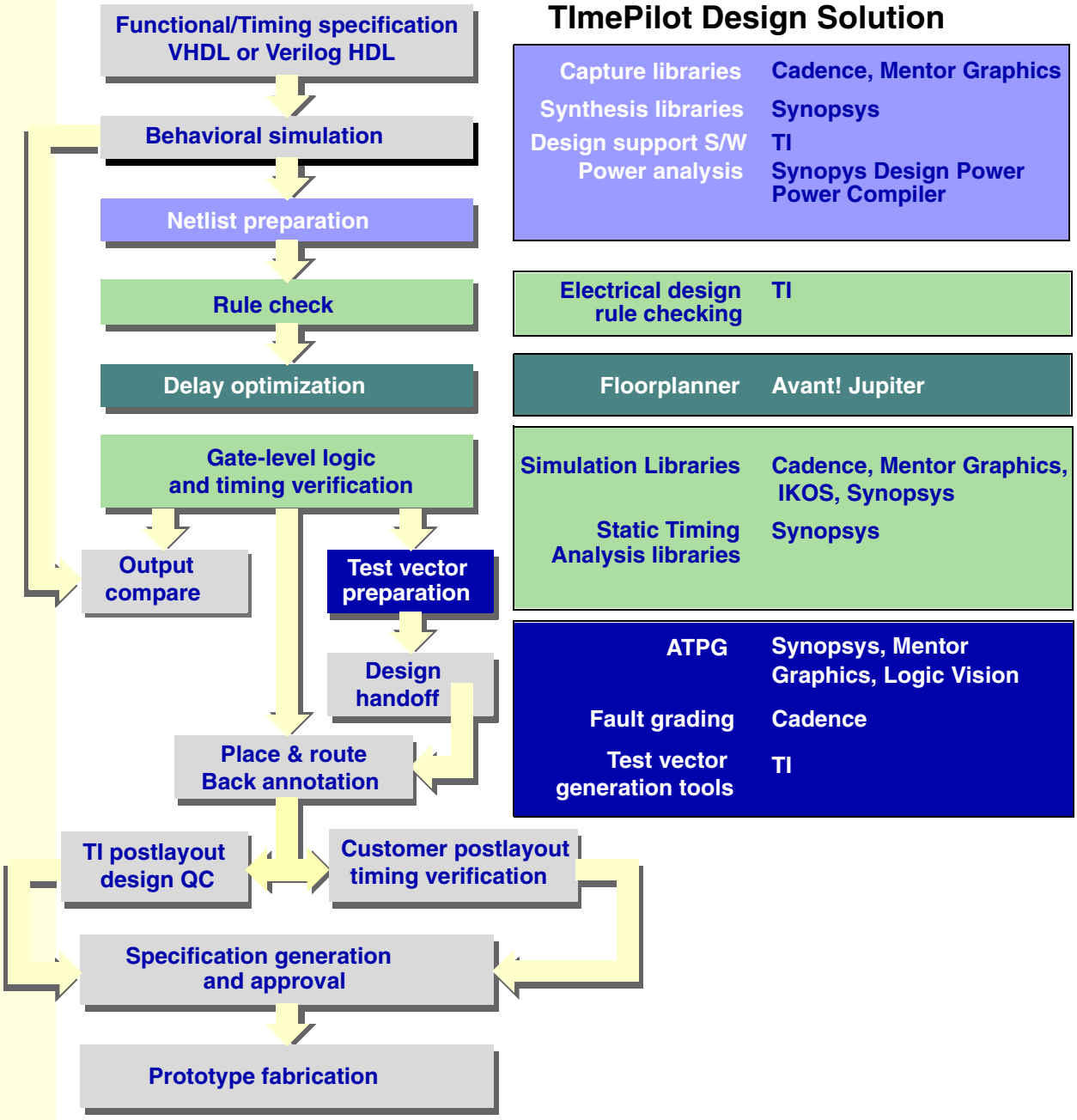


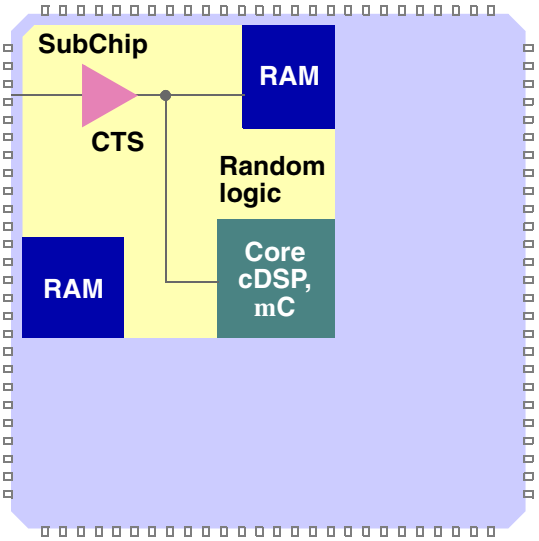
Table 8: TImePilot and GS20 CAD Tool Support

Platform/Tool	Options
Hardware platforms and operating systems	Sun SPARCStation™ 10/20/Ultra2/4/Enterprise (Solaris 2.5.1/2.6)
	HP9000 OS 10.20
Architectural synthesis	Synopsys Behavioral Compiler
Limited synthesis	Synopsys ECO Compiler
Logic synthesis	Synopsys DC Professional/Expert
Formal verification	Chrysalis Design VERIFYer™, Synopsys Formality™
Capture	Mentor Graphics™ Design Architect™
RAM compilation	Web-based ACE toolkit
Floorplanning	Avant! Jupiter™
Simulation	QuickSim II, ModelSim™, Verilog-XL™, Cadence Leapfrog™ for VHDL, IKOS Voyager-CS/NSIM™, Synopsys VSS™, Synopsys/Viewlogic VCS™
Datapath	Synopsys DesignWare™
Static Timing Analysis (STA) signoff	Synopsys Primetime™
Logic design rule checking	Detector™
Test vector verification	SimOut™
Test vector generation	TDLGEN ™
Test vector rule checking	TDLCHKR™
Automatic place and route	Avant! Apollo™
Test synthesis and ATPG	Synopsys Test Compiler/Test Compiler Plus™, Synopsys/ Viewlogic Sunrise™, Mentor Graphics FastScan™, Flex-Text™, DFT Advisor™, LogicVision ICRAMBIST™/MEM-BIST™
Fault grading	Mentor Graphics QuickGrade II™/QuickFault II™, Cadence Verifault™
Evaluation	Paragon™
Power	Synopsys DesignPower™, PowerCompiler™

Design Reuse

A SubChip is a design module that undergoes placement and routing as a discrete block that can be reused as a component of a larger design, as illustrated in Figure 9. When reused, the placement and routing of the SubChip stay the same so that its previous functionality and timing are preserved. This capability allows for independent optimization of design modules and provides increased designer productivity through module reuse.

Figure 2: SubChip Components



A SubChip can include:

- TImeBuilder modules
- Clock tree synthesis (CTS)
- Random logic
- Cores
- Analog cells
- Other SubChips

Some benefits of SubChips include:

- They are user- or TI-defined functions with known postlayout timing, area, and power that can be used in prelayout chip designs and simulations.
- Multiple instances can be placed in a design and will have identical timing.
- SubChips can be used by multiple designs.
- Complex designs can be implemented and/or easily modified by the designer without the difficult modeling or characterization associated with a complex hard macro design.

Clock Tree Synthesis (CTS)

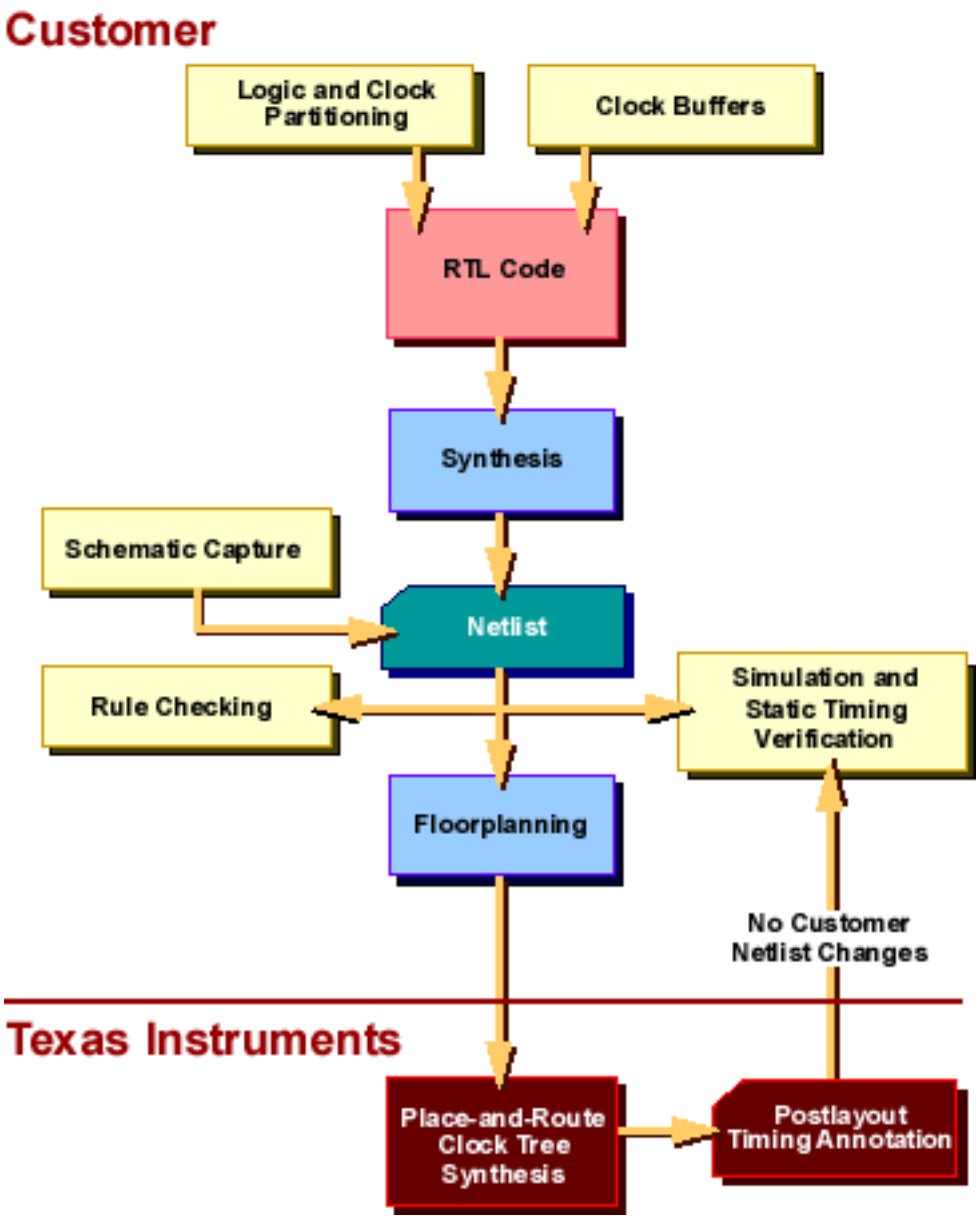
Clock tree synthesis (CTS), shown in Figure 3 on page 21, is the primary method of clock distribution for GS20 family standard cell designs. The key capabilities of the CTS flow are:

- Insertion delay, skew, and power management
- Capability to handle more than 200 clocks
- Gated clock support for lower power
- Ability to balance multiple clocks together
- Easy to use in design flow
- Good prelayout to postlayout correlation
- Layout-centered approach for lowest skew and delay
- No customer netlist modifications
- Balancing into a SubChip
- One CTS macro
- Automatic clock buffer selection

With clock tree synthesis, the customer instantiates a single CTS buffer per clock tree. The CTS buffer is expanded at layout into a multistage clock tree. The configuration of the clock tree is optimized for size, delay, and power in accordance with the requirements of the application, and the clock tree is placed according to the location of its loads.

The postlayout timing of the clock tree is back annotated to the customer's original netlist. The insertion delay is annotated as CTS buffer gate delay, and the clock skew is annotated to the input pin of the individual loads. Clock tree balancing and tuning are accomplished automatically by insertion of tuning buffers and loads at the root of the clock tree.

Figure 3: Clock Tree Synthesis Flow



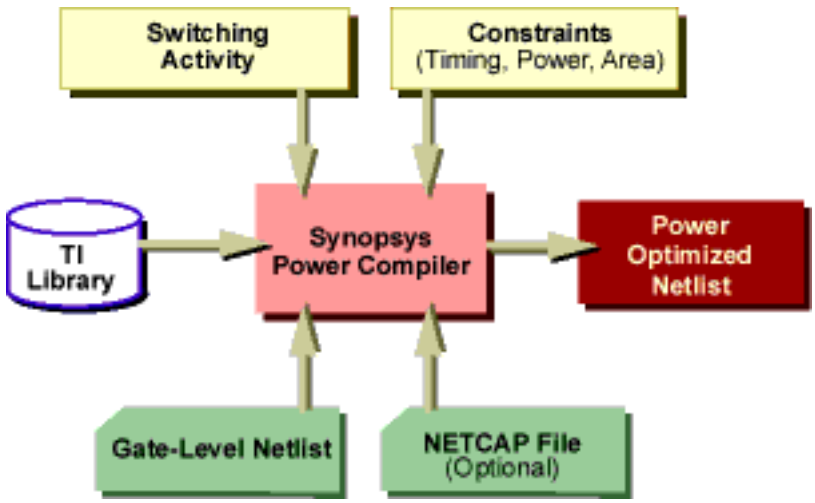
Power Analysis and Optimization

To achieve a low system power, the GS20 family provides:

- Support for Synopsys Power Compiler and DesignPower
- 1.1-V, 1.4-V, and 1.8-V libraries
- Core macros optimized for low power
- Optimized library for efficient synthesis, lowering net count and gate count to reduce power
- Full support for gated clock methodologies, which reduce switching activity through clock tree synthesis and clock balancing capabilities.
- Low-power and ultra-low-power I/Os
- TImeBuilder modules that draw zero dc current

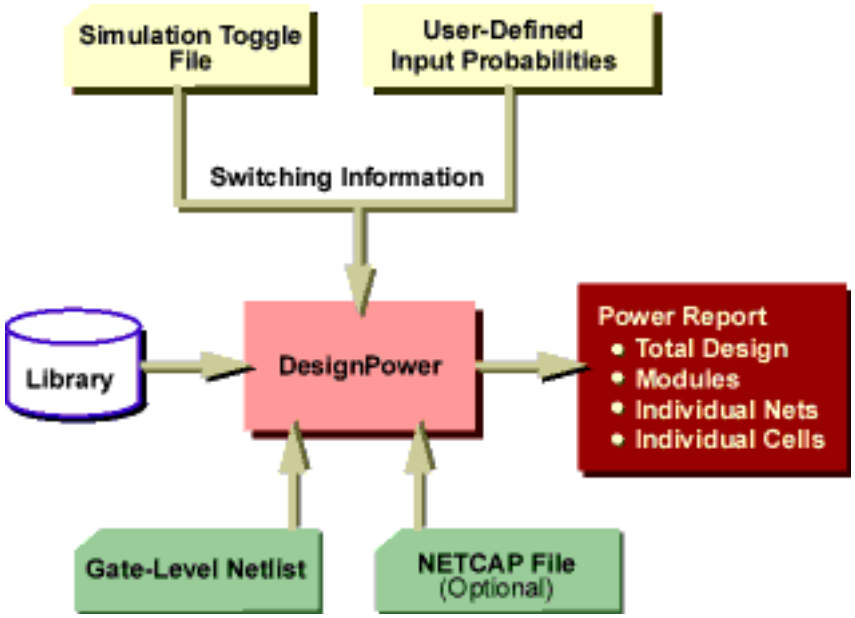
To optimize gate-level power, the GS20 family fully supports the Synopsys power optimization tool, Power Compiler. A design flow using Power Compiler is shown in Figure 3.

Figure 4: Design Flow Using Power Compiler



To analyze how much power is actually dissipated in a specific netlist, the GS20 family supports the Synopsys power analysis tool, DesignPower. A design flow using DesignPower is shown in Figure 4.

Figure 5: Power Estimation Using Synopsys DesignPower



GS20 Operating Conditions

Table 9: Recommended Operating Conditions

Parameter			MIN	NOM	MAX	Units
General	V_{DD}	Core and primary-I/O supply voltage	1.0	1.1	1.2	V
			1.26	1.4	1.54	
			1.65	1.8	1.95	
	V_{DDS}	Secondary-I/O supply voltage	2.3	2.5	2.7	V
			2.5	2.75	3	
		commercial	2.7	3.3	3.6	
		industrial	3	3.3	3.6	
			4.5	5	5.5	
	T_A	Operating free-air temperature range	-40		85	°C
	T_J	Junction temperature range	-40		125	°C
		for 10-year life	-40		105	
CML	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
	V_{REF}	Reference voltage		V_{DDS}		
	V_{Term}	Termination voltage	3.0	3.3	3.6	
GaAs	V_I	Input voltage	-2		-0.7	V
	V_O	Output voltage	-2		-0.7	
	V_{REF}	Reference voltage		-1.32		
	V_{Term}	Termination voltage		-2		
ATA-66	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
TLV	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
	V_{REF}	Reference voltage		0.5 V_{DDS}		
	V_{Term}	Termination voltage		0.5 V_{DDS}		

Parameter			MIN	NOM	MAX	Units
LVDS	V_I	Input voltage	0		2	V
	V_O	Output voltage	0.935		1.465	
	V_{Term}	Termination voltage		1.2		
GTL+	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
	V_{REF}	Reference voltage		0.667 V_{DDS}		
GTL++	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
	V_{REF}	Reference voltage		1		
	V_{Term}	Termination voltage		0.5 V_{DDS}		
HSTL	V_I	Input voltage	-0.3		V_{HSTL} +0.3	V
	V_O	Output voltage	0		V_{HSTL}	
	V_{HSTL}	Independent supply voltage for HSTL macros		1.5		
	V_{REF}	Reference voltage		0.5 V_{HSTL}		
	V_{Term}	Termination voltage		0.5 V_{HSTL}		
PCML	V_I	Input voltage	-0.3		V_{DDS}	V
	V_O	Output voltage	0		V_{DDS}	
	V_{REF}	Reference voltage		1.3 or 2		
	V_{Term}	Termination voltage		1.5 or 2.2		
DPECL	V_I	Input voltage	V_{Term}		V_{DDS}-0.7	V
	V_O	Output voltage	V_{Term}		V_{DDS}-0.7	
	V_{Term}	Termination voltage	V_{DDS}-1.9	V_{DDS}-2	V_{DDS}-2.1	
SSTL_2	V_I	Input voltage	-0.3		V_{DDO} +0.3	V
	V_O	Output voltage	0		V_{DDO}	V
	V_{REF}	Reference voltage		0.5 V_{DDO}		V
	V_{TT}	Termination voltage		0.5 V_{DDO}		V