TEXAS INSTRUMENTS

GS30TR 0.15-μm CMOS Standard Cell/Gate Array

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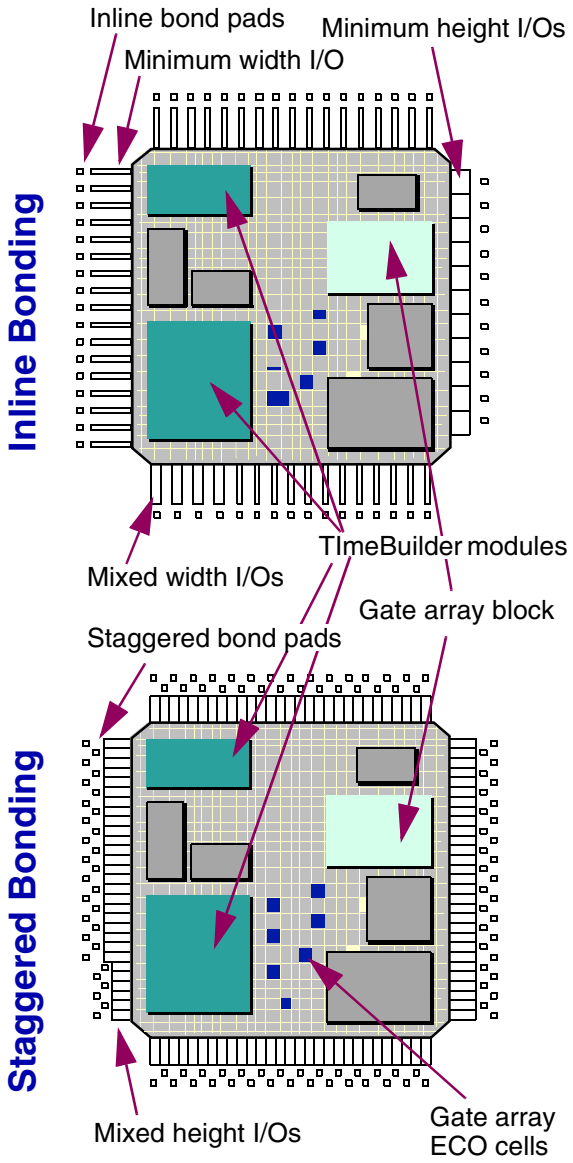
TEXAS INSTRUMENTS

GS30TR 0.15-µm CMOS Standard Cell/Gate Array

High-Performance ASIC

- **Designed for optimum speed and integration**
- **Over 500 cells optimized for performance**
- **Core cell architecture optimized for speed**
- **Over 250 peripheral macros,** including many high-performance I/Os, LVCMOS, differential, level-shifting I/Os, CML, DPECL, GaAs, LVDS, SSTL, TTL, TLV, oscillators
- **0.15-µm Leff process** (0.18-µm drawn) with Shallow Trench Isolation (STI)
- **5 levels of metal**
- **Density:** 45,000 gates/mm^2 at 50K gates
- **Over 20 million raw gates capacity**
- **Power supply:** 1.65 to 1.95 V cores I/Os: 1.8/2.5/3.3 V (selected combinations), 5 V-tolerant, failsafe
- **Power dissipation:** 0.0375 µW/MHz/gate for 1.8 V core
- **Multi-gigabit** serial link transceiver technology
- **Extensive module selection**, including TMS 320 digital signal processors (DSPs), ARM™ 32-bit RISC microcontrollers, MIPS® JADE™ and Opal™ embedded processors, and analog functions
- **Memory compilers** including single-port, two-port, dual-port, three-port, ROM, CAM, register file, and synthesizable memories
- **TI ExSRAM** extremely high-density SRAM (>3 Mb of memory on a die)
- **Electrically-readable die ID**
- **Spare gate-array cells** for fast metal-level ECO
- **Packages:** TQFP, plastic BGA, Generic BGA, flip-chip



Features and Benefits

TImeCell™ Architecture-- Faster to Market at a Price You Can Afford

GS30TR uses Texas Instruments TImeCell™ Architecture, the first to combine on the same silicon the cost-efficiency of standard cells with the fast time-to-market of gate arrays. TImeCell's powerful combination of the two ASIC technologies gives designers the flexibility they need to build multimillion-gate, single-chip systems. Designers no longer have to choose between the greater density and lower per-unit costs of standard cells and the rapid turnaround and flexibility of gate arrays.

Today, most complex ASICs are developed by taking an already proven design and adding new functionality. TImeCell allows designers to pack the proven sections of their designs into ultra-dense standard cell logic, while creating new logic functions in gate arrays. Using this approach reduces layout and prototype fab cycle time by more than 50 percent over standard cell and allows design changes up until the last minute.

Up to 80 percent of today's single-chip platform ASICs contain lower-risk logic implemented as reusable custom blocks, gate-level netlists, or RTL code. The remaining 20 percent consists of new, unproven logic used to differentiate the design from previous generation s or other product family members. For the lower-risk logic, designers want the density, performance and power advantages of standard cell. For the new logic, designers want the time-to-market advantages of gate array to help manage the inherent risk of unproven logic. TImeCell gives the best of both worlds.

While giving designers more flexibility at the silicon level, TImeCell also enables a whole new design approach. Designers can combine sections of customized logic with a variety of system-level blocks such as DSP cores, RISC cores, peripherals and application modules. TI has supported embedded processors in ASICs since 1991, and now our TImeBuilder™ Module Library provides a broad range of systems-on-a-chip intellectual property (IP), with the design and verification methodology and support to make integration easy.

GS30 Product Family-- Support for a Wide Range of Applications

TI provides a full range of products to address the challenges of producing high performance, ultra-dense and low-power devices that take advantage of system integration.

Product	Technology	Focus	Applications
GS30	0.15 µm L_{eff}	High density, low power	General
GS30TR	0.15 µm L_{eff}	High performance	Telecommunications, networking
GS30KA	0.13 µm L_{eff}	Ultra-high performance	Processors, wireless base stations, networking

High-Performance Design Optimization

GS30TR is designed to offer high performance and opportunity for more integration. To achieve maximum performance, the GS30TR family provides:

- Cell architecture created for maximum performance
- Synchronizer flip-flops for simulation across clock domains
- 5LM and high-performance packaging for heat dissipation/handling
- Synopsys library variable optimization for high-performance design
- Design of high-performance macros for maximum performance return
- Wide variety of high-performance I/Os
- Macros designed for telecommunications and networking applications, including clock generators and APLLs

TImePilot software provides high-performance design methodology, including support for early testcase layouts and timing-driven routing.

Some key GS30TR characteristics are:

Nominal core voltage	1.8 V
I/O voltages	1.8, 2.5, 3.3, 5.0-tolerant and -failsafe
Typical gate delay NA210, FO = 7	59 ps
Typical design power dissipation	0.0375 µW/MHz/gate

System-Level Integration-- The Advantage of Experience and Leadership

The GS30 product family is positioned to take advantage of TI's decade of experience in system-level integration and systems-on-a-chip design. TI brings a wealth of capabilities to this field:

- World's leading Digital Signal Processor (DSP) supplier
- A world-leading supplier of embedded RISC cores, including the ARM and MIPS processor families
- World's leading supplier of analog and data transmission solutions, including the IEEE 1394, Universal Serial Bus (USB) and Ethernet
- TI's unique SLI Architect tools that allow complete processor subsystems (the processor and all support peripherals) to be quickly assembled and verified
- Full support for hardware/software coverification
- Advanced process technologies
- Superior design support and manufacturing— "no excuses" ramp to production

The TImeBuilder™ library and methodology (see page 13) gives you easy access to all of the modules and tools you need for the fast and successful integration of processors within your ASIC. TI offers a complete SLI solution; processors, IP modules, software boot code, example software drivers and a complete coverification environement.

Advanced Technology

- **5-level metal** with full Chemical Mechanical Polishing (CMP) planarization, fully stacked Tungsten vias, and STI

Extensive Library for High Performance and Integration

- **Core macros designed to meet high-performance requirements**
- **A full range of inputs/outputs** (I/Os) in many specifications and voltages for speed and power trade-offs, including LVDS, HSTL, CML, 5-V-tolerant I/Os and SSTL
- **TImeBuilder module library and methodology and analog cells** for easy system-level integration
- **Memory compilers**, including synthesizable RAMs for more area efficiency in small RAM configurations
- **Fully characterized libraries** for accurate modeling
- **Sprinkled gate array cells** for fast metal-level design changes late in the design cycle

Proven Methodology

- **TImePilot™ design system**, which offers a multi-EDA-vendor strategy based on industry standards. This system, combined with enhancements in the design flow, simplifies and speeds the design process to help you achieve timing closure. An easy-to-use Design Sequencer steps you through the floorplanning process (built around a vendor-supplied floorplanner) and all of its associated design steps. See Table 7 on page 18 for a list of supported CAD tools.
- **Clock tree synthesis (CTS)** design flow that provides automatic synthesis of clock trees in physical design to meet designers' skew and insertion delay goals. The TI CTS flow supports more than 200 clock domains and clock gating for low power, and consistently achieves less than 50 ps clock skew.
- **Complete STA signoff methodology** enables comprehensive verification and minimizes gate-level simulation efforts at design hand-off. The Synopsys PrimeTime™-based signoff flow is supported with delay fault test generation capability using Sunrise™ tools.
- **SubChip™** design capabilities that support hierarchical design
- **VHDL and Verilog™ signoff flows** for reduced cycle time and improved accuracy
- **Synopsys™ Power Compiler™ support** for power reduction

Packaging for Performance

- **Package options** include thin quad flat pack (TQFP), Plastic BGA, Generic BGA and flip-chip. For more details, see Table 6 on page 15.

Macro Library

The GS30TR macro library includes a wide variety of cells tuned for high performance, and, like all GS30 family libraries, fully characterized for accurate modeling.

Performance Equations

Every timing path through each GS30 family core and I/O macro is characterized at multiple voltage, temperature, process, input slew, and output load points. No global derating with respect to voltage, temperature, or process is used with the GS30 family. The characterized data coupled with nonlinear delay modeling allows SPICE-like accuracy for a large range of operating conditions.

Library Description

The GS30 family macro library has been optimized for use with synthesis and power optimization tools. Data from over 200 synthesized designs, focusing on telecommunications and networking designs, was analyzed to determine high-usage macros. In addition, a team of TI engineers worked closely with leading synthesis vendors to determine an optimal cell set. As a result, the GS30TR library features:

- Ultra-high-performance core and I/O macros
- A rich set of Boolean functions
- A wide variety of gates with inverting inputs
- Multiple-drive-strength gates
- Minimized internal transistors in multistage macros
- Compact flip-flops and latches with Q and QZ
- Negative-edge flip-flops

The most frequently-used GS30TR cells are optimized for highest performance at:

Load	Standard Load	Slew
Low	5 - 10	0.5 ns
Medium	10 - 20	0.7 ns
High	20 - 40	0.9 ns

Core Macros

A summary of core functions is shown in Table 1.

Table 1: GS30TR Family Core Macros

Function	Number of macros
Datapath	13
AND/NAND/OR/NOR	75
Exclusive-OR/Exclusive-NOR	17
Inverters	15
Buffers	18
Boolean functions	62
Multiplexers	18
D-type flip-flops	37
Latches	4
Scan flip-flops/latches	37
Clock generators	8
Clock-tree synthesis buffers	20
Special functions/miscellaneous	20
Total	**336**

The GS30TR core library contains synchronizer flip-flop models that prevent setup-hold violations during cross-clock domain simulation. These flip-flops:

- Are based on the design of existing DTN10 and TDN10 flip-flops
- Have no setup-hold timing checks on the D pin
- Are tagged as “don’t touch” for Synopsys (as they must be hand-instantiated)

Gate Array Macros

The goal of performing an Engineering Change Order (ECO) is to make necessary changes to a design with minimal changes to the die. The TImePilot floorplanning flow lets you add, delete and swap core cells.

A summary of the GS30TR macro library gate array cells available for ECO are shown in Table 2.

Table 2: Gate-Array Cells for ECO

Function	Number of macros
AND	2
Buffers	8
D-type flip-flops	2
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NANDs	8
NORs	8
ORs	1
Scan flip-flops	2
Special functions/miscellaneous	3
Total	**45**

High-Performance Macros

High-speed applications, such as synchronous digital hierarchy (SDH) and asynchronous transfer mode (ATM), require correct alignment between the data and clock signals. To ensure this data synchronization, the GS30 family provides a set of macros to build systems capable of phase alignment and digital clock recovery. These high-performance macros include:

- Many I/Os, most up to 750 MHz, including CML, DEPCL, GaAs, LVDS, SSTL, TLV, HSTL
- CK814A clock generator with integrated PLL (750 MHz)
- S8P21 serial-to-parallel converter and P8S20 parallel-to-serial converter
- DLP53 digital clock recovery

Key product features include operating range exceeding 750 MHz, tolerance to input jitter and pulse distortion up to 30 percent, data out retime to system clock, and high test coverage.

The phase alignment function (clock macro and serial-to-parallel converter) resynchronizes off-chip data to an on-chip clock when the relationship between the two is unknown or changing over time. The phase alignment function tracks this variation and maintains data integrity in the receiving function.

I/O Macros

GS30TR provides 1.8, 2.75, 3.3, 5-V-tolerant and 5-V-failsafe I/Os. Most output buffers are available in three noise performance options: high performance, low noise and ultra-low noise. To minimize system noise and power pins, select the lowest noise output that the application allows. Ultra-low-noise I/Os typically require only one-fifth the number of power pins that high-performance I/Os require.

The user creates a bidirectional macro by selecting inputs and outputs and combining the functions in the netlist. You can add pullup and pulldown macros to I/Os in the same manner. I/O macros include:

- LVCMOS, TTL
- CML, GaAs, TLV, LVDS, HSTL, SSTL, PCML, DPECL
- Low noise, ultra-low noise, failsafe, and 5 V-tolerant options
- 2/2mA - 12/24mA output drivers

Table 3: I/O Specifications

Type	Maximum Frequency	Signal Swing	Signal Type
TTL	200 MHz	3.3 V	single
LVCMOS	200 MHz	varies by V_{DDS}	single
CML	800 MHz	400 - 800 mV	differential
GaAs	800 MHz	600 - 800 mV	differential
TLV	250 MHz	800 mV	single & differential
LVDS	800 MHz	250 - 600 mV	differential
HSTL	400 MHz	1.8 V	single & differential
SSTL_2	200 MHz	2.5 V	single
DPECL	800 MHz	600 - 800 mV	differential

Memories

GS30TR supports synchronous single-port, two-port, dual-port, and three-port memory compilers and ROM, CAM and asynchronous two-port compilers. These dense memories let you specify the exact word and bit counts for each memory to meet the application's need. All memories can have synchronous operation, zero dc power and zero hold times.

Table 4: Memories Summary

Description	Min Bits	Max Bits	Max Words	Max Bits/ Word	Functionality
2-port SRAM (1W/1R)	4	32K	2K	64	Asynchronous
1-port Clocked RAM, density optimized, word write/bit write	2K	1Mbit	32K	128	Single edge
1-port Clocked ROM, via2, fast/dense	32	1Mbit	64K	64	Single edge
Dual-port CRAM, bit write	64	128K	4K	128	Single edge
1-port ROM, speed optimized	64	1Mbit	64K	128	Asynchronous
1-port CRAM, speed optimized, bit write	4K	1Mbit	64K	144	Single edge
1-port CRAM, multistrobe, page mode, low power	1K	128K	4K	64	Single edge
2-port CRAM (1W/1R), small, word write/bit write	4	9K	512	72	Single edge
2-port register file (1W/1R), bit write	2	32K	512	256	Synchronous write/asynchronous read
1-port CRAM, area optimized, word write/bit write	32	128K	2K	128	Single edge
1-port CROM, moat program, fast/dense	32	1Mbit	64K	64	Single edge
3-port CRAM (1W/2R)	32	144K	4K	128	Single edge
3-port CRAM (2W/1R)	32	144K	4K	128	Single edge
CAM compiler	512	128K	1K	128	Synchronous
2-port CRAM (1W/1R), large, WE pin	256	128K	8K	128	Single edge
Dual-port RAM, large bit count, very fast, bit write	64	256K	8K	32	Single edge
Dual-port RAM, simultaneous access capability, redundancy	64	128K	4K	32	Single edge

Single-Port Clocked SRAM Compiler

The single-port clocked SRAM compiler creates speed-optimized RAM blocks based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor. Contact the TI Customer Design Center for complete details.

Single-Port Clocked SRAM Compiler With Word-Write, Bit-Write and Multistrobe

In addition to the single-port clocked SRAM, TI also offers single-port memories with both word-write and bit-write capability. The bit-write capability enables you to update individual bits in the single port without changing the rest of the word. Multistrobe allows data to be read and/or written on up to three strobes.

Dual-Port Clocked SRAM Compiler

The dual-port clocked SRAM compiler creates area- and speed-optimized RAM based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor.

Synthesizable Memories

For maximum flexibility, GS30TR offers a number of memory options for use as “soft,” or synthesizable, memories. This compiler generates RTL (based on your specifications) as well as constraints for synthesis. Synopsys Design Compiler™ is then used to synthesize these memories to either flip-flop or latch-based implementation with support for multiple test methodologies. The compiler options are:

- 1-port CRAM area optimized
- 1-port CRAM speed optimized
- 2-port asynchronous RAM
- 2-port CRAM
- Dual-port RAM

TImeBuilder Modules

Texas Instruments has more than a decade of experience with complex integration and reuse for a wide variety of application-oriented markets. This experience gives TI a practical understanding of the challenges of integration; leadership in key integration areas gives TI the ability to offer unique solutions. TI is the world leader in digital signal processor (DSP) solutions, the world-leading supplier of data transmission peripherals, the world-leader in analog, and the world-leading supplier of ARM RISC processors (and also offers MIPS and NEC processors).

GS30TR supports a wide variety of TImeBuilder modules for integrating complex functionality onto a single die. TImeBuilder gives you access to DSP technology from the company who invented it, and the ability to easily integrate it with a wide selection of core modules, including the ARM and MIPS Jade. Our DSPs, USB controller, DMA controller and bus bridges all contain logic to support easy access to the ARM Processor Interface (API).

Table 5: TImeBuilder Modules

Processors	
TMS320C54X Digital Signal Processor	ARM 7 32-bit RISC processor
MIPS 32-bit Opal RISC processor	ARM 9 32-bit RISC processor
MIPS 64-bit RISC processor	ARC 32-bit RISC processor
NEC V850 32-bit RISC processor	
Processor Peripherals	
SDRAM controller	Multi-master arbiter
Multi-channel DMA controller	16-bit timer
Interrupt controller	Watchdog timer
Peripheral bus controller	Serial port SPI/uWire
Mixed Signal	
Analog-to-digital converters	Digital PLLs
Digital-to-analog converters	Analog PLLs
Data Communications	
10/100 Ethernet MAC	I2C master/slave
10/100 Ethernet PHY	IEEE 1394 link core
33 MHz 32-bit PCI	IEEE 1284 parallel port
66 MHz 32-bit PCI	USB hub
UART	USB function controller
USART	Reed Solomon encoder/decoder
Single-channel HDLC	2.5 Gbps serial link
Multiple channel HDLC	RAMBUS (direct)
IrDA	

Analog Cells

Analog cells include:

- Clock squarer with low power mode (dual gate only)
- Analog regulators
- Analog phase-locked loop, 50 - 500 MHz, zero-pin implementation
- Analog input and output switches

Special Functions

GS30TR special functions cells include cells designed for telecommunications applications, voltage regulators and electrically readable die ID.

Telecommunication Cells

These special cells include:

- Digital clock recovery with an integrated APLL
- Clock generator
- 8b serial-to-parallel and parallel-to-serial interface
- 10b serial-to-parallel and parallel-to-serial interface

Voltage Regulators

These feature:

- 3.3 V to 1.8 V regulator with bandgap reference
- No external pass device is required
- Three pins: 3 V, 1.8 V, powerdown (NZ), PG
- Three components: REG00 (I/O, pass device and control), CAP00 (core, bypass capacitor) and VR000 (core, bandgap reference)
- 50mA units, 100mV internal ripple (use one I/O and one bypass cap for each 50mA current; all connect to a single VR000 bandgap reference)

Electrically Readable Die ID

This cell function contains a unique identifier for each die fabricated. You can access the 64-bit identifier in software directly from the ASIC or through the JTAG TAP controller during test. The TImePilot test flow supports either muxed or clocked scan methodology.

Packaging

GS30TR supports the package types shown below.

Table 6: Supported Packages

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)	Supports Staggered Bond
Thin Quad Flatpack (TQFP)	32	VF	7x 7x1.4	0.80	✷
	48	PFB	7x 7x1.4	0.50	✷
	52	PAH	10x10x1.0	0.65	
	64	PAG	10x10x1.0	0.50	
	80	PET	10x10x1.0	0.40	✷
	80	PFC	12x12x1.0	0.50	✷
	100	PZT	14x14x1.0	0.50	
	128	PDT	14x14x1.0	0.40	
	144	PGE	20x20x1.4	0.50	✷
	160	PBL	20x20x1.4	0.40	✷
	176	PBL	20x20x1.4	0.40	✷
	176	PGF	24x24x1.4	0.50	✷
	208	PDV	24x24x1.4	0.50	✷
	216	PDQ	24x24x1.4	0.40	✷
Plastic BGA (PBGA)	256	GFN	27x27	1.27	✷
	352	GFT	35x35	1.27	✷
Plastic BGA, thermal ball (PBGA- TB)	272	GFN	27x27	1.27	✷
	388	GFW	35x35	1.27	
Generic BGA (GBGA)	672	GKP	40x40x1.7	1.27	
	792	GKQ	40x40x1.7	1.00	
	896	GKQ	40x40x1.7	1.00	

GS30TR will support flip-chip packages up to 1672 pins. Flip chip use is limited by the available packages and die size; it requires N+1 metal layers.

TImePilot Design Flow and CAD Tools

Fully characterized libraries account for the effects of voltage, temperature, process, load, and input rise and fall times. Hierarchical design viewing and editing, floorplanning, and timing analysis allow the designer to achieve the accurate representation of silicon through forward annotation of timing to the layout software. This design approach, shown in Figure 1 on page 17, gives designers full advantage of the high-performance characteristics that submicron CMOS technology offers.

The TI approach to open CAD enables easy interaction with other systems. Signoff quality libraries for all supported simulators, test vector verification software, and design-rule-checking software enable the customer to verify the design completely before handoff to TI, significantly shortening design cycle time and eliminating correlation issues. Synopsys VSS, and Model Technology ModelSim™ simulation libraries conform to IEEE Std. 1076.4-1995–VITAL 95. Tools and libraries in the TImePilot design environment are supported on both Sun™ and HP™ workstations.

TImePilot uses the Avant! Planet™ floorplanner. TI has added several features to the floorplanning flow, including a sequencer that steps users through all floorplanning-related tasks. Many traditional place-and-route features are now available in the floorplanner to help achieve first-pass timing convergence. Other features include:

- Gate-level floorplanning
- SubChips for reuse (see “Design Reuse” on page 19)
- Clock tree synthesis, a flexible, low power strategy for clock distribution (see “Clock Tree Synthesis (CTS)” on page 20
- Team design
- Path timing-driven placement
- Rules-driven placement
- Floorplan checks
- Wide-wire support for power management
- ECO

The primary aim of the design flow is to offer state-of-the art design tools and a highly productive environment to enable designers to achieve error-free designs in the shortest time that meets timing goals. The flow is also designed to comprehend the effects of deep submicron technology by accurately estimating interconnection lengths and resistance-capacitance (RC) effects, and by providing close correlation between floorplanning and synthesis and pre- to postlayout delays.

Figure 1: Design Flow Overview

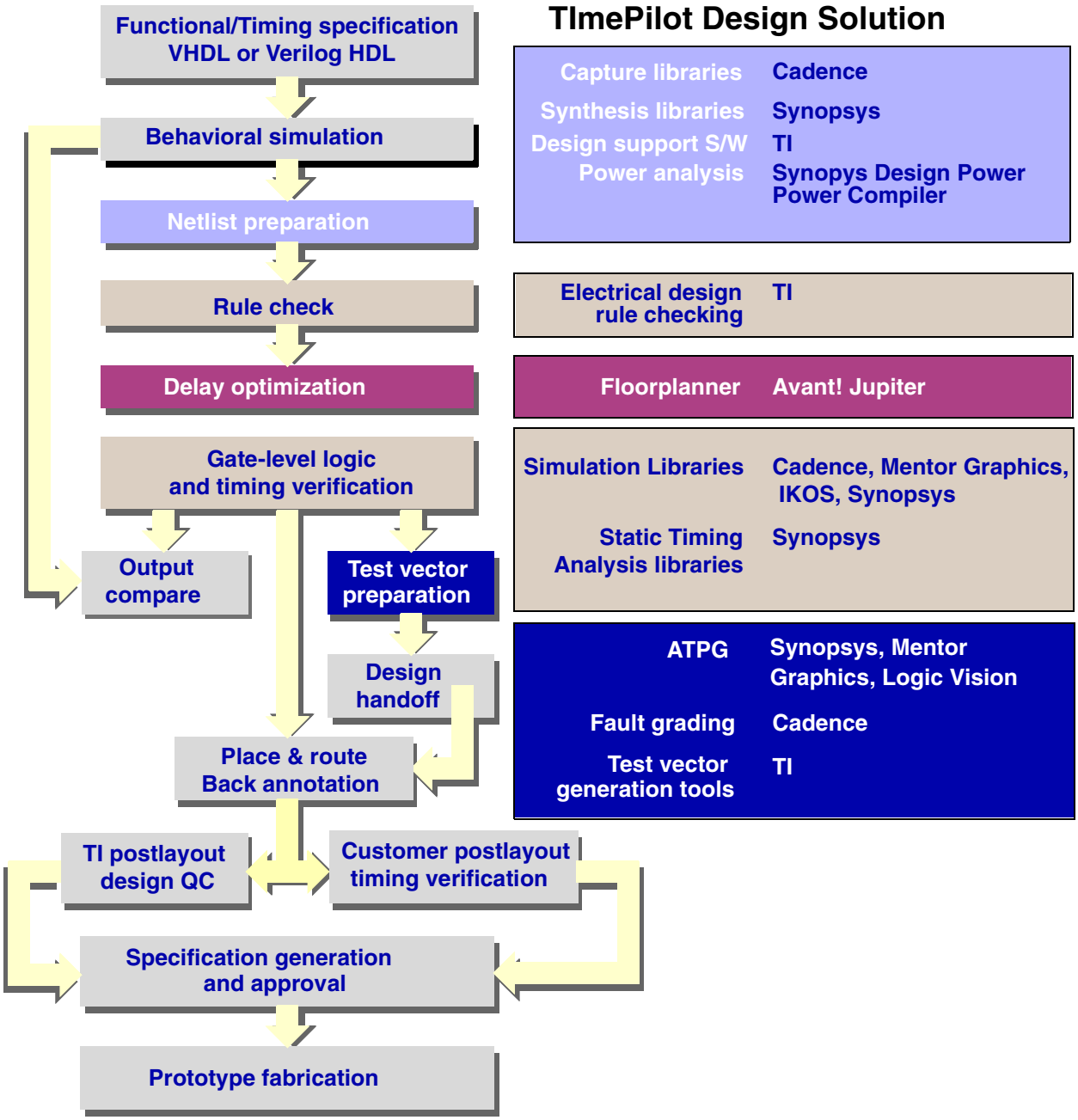


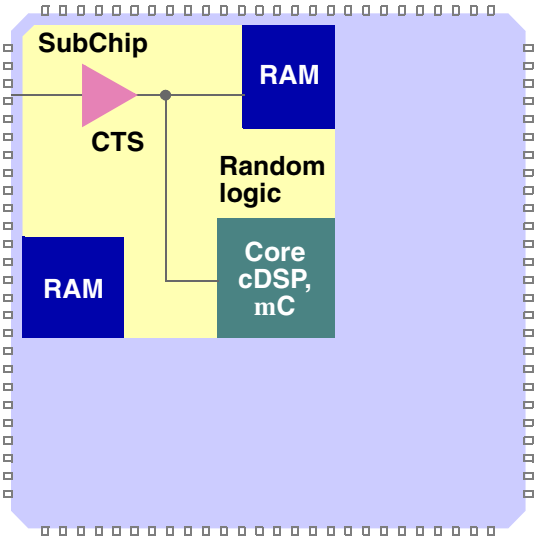
Table 7: TImePilot CAD Tool Support

Platform/Tool	Options
Hardware platforms and operating systems	Sun ULTRAsparc™ platforms (Solaris 2.5.1/2.6) HP9000 (HP-UX™ 10.20)
Architectural synthesis	Synopsys Behavioral Compiler
Limited synthesis	Synopsys ECO Compiler
Logic synthesis	Synopsys DC Professional/Expert
Formal verification	Chrysalis Design VERIFYer™, Synopsys Formality™
RAM compilation	Web-based ACE toolkit
Floorplanning	Avant! Jupiter™
Simulation	ModelSim™, Verilog-XL™, NC Verilog, IKOS Voyager-CS/ NSIM™, Synopsys VSS™, Synopsys/Viewlogic VCS™
Datapath	Synopsys DesignWare™
Static Timing Analysis (STA) signoff	Synopsys Primetime™
Logic design rule checking	Detector™
Test vector verification	SimOut™
Test vector generation	TDLGEN ™
Test vector rule checking	TDLCHKR™
Automatic place and route	Avant! Apollo™
Test synthesis and ATPG	Synopsys Test Compiler/Test Compiler Plus™, Synopsys/ Viewlogic Sunrise™, Mentor Graphics FastScan™, Flex-Text™, DFT Advisor™, LogicVision ICRAMBIST™/MEM-BIST™
Fault grading	Cadence Verifault™
Evaluation	Paragon™
Power	Synopsys DesignPower™, PowerCompiler™

Design Reuse

A SubChip is a design module that undergoes placement and routing as a discrete block that can be reused as a component of a larger design, as illustrated in Figure 9. When reused, the placement and routing of the SubChip stay the same so that its previous functionality and timing are preserved. This capability allows for independent optimization of design modules and provides increased designer productivity through module reuse. SubChips can be used on multiple designs.

Figure 2: SubChip Components



A SubChip can include:

- TImeBuilder modules
- Clock tree synthesis (CTS)
- Random logic
- Cores
- Analog cells
- Other SubChips

Some benefits of SubChips include:

- They are user- or TI-defined functions with known postlayout timing, area, and power that can be used in prelayout chip designs and simulations.
- Multiple instances can be placed in a design and will have identical timing.
- SubChips can be used by multiple designs.
- Complex designs can be implemented and/or easily modified by the designer without the difficult modeling or characterization associated with a complex hard macro design.

Clock Tree Synthesis (CTS)

Clock tree synthesis (CTS), shown in Figure 3 on page 21, is the primary method of clock distribution for GS30 product family designs. The key capabilities of the CTS flow are:

- Insertion delay, skew, and power management
- Capability to handle more than 200 clocks
- Gated clock support for lower power
- Ability to balance multiple clocks together
- Easy to use in design flow
- Good prelayout to postlayout correlation
- Layout-centered approach for lowest skew and delay
- No customer netlist modifications
- Balancing into a SubChip
- One CTS macro
- Automatic clock buffer selection

With clock tree synthesis, the customer instantiates a single CTS buffer per clock tree. The CTS buffer is expanded at layout into a multistage clock tree. The configuration of the clock tree is optimized for size, delay, and power in accordance with the requirements of the application, and the clock tree is placed according to the location of its loads.

The postlayout timing of the clock tree is back annotated to the customer's original netlist. The insertion delay is annotated as CTS buffer gate delay, and the clock skew is annotated to the input pin of the individual loads. Clock tree balancing and tuning are accomplished automatically by insertion of tuning buffers and loads at the root of the clock tree.

Figure 3: Clock Tree Synthesis Flow