TEXAS INSTRUMENTS

GS40 0.11-μm CMOS Standard Cell/Gate Array

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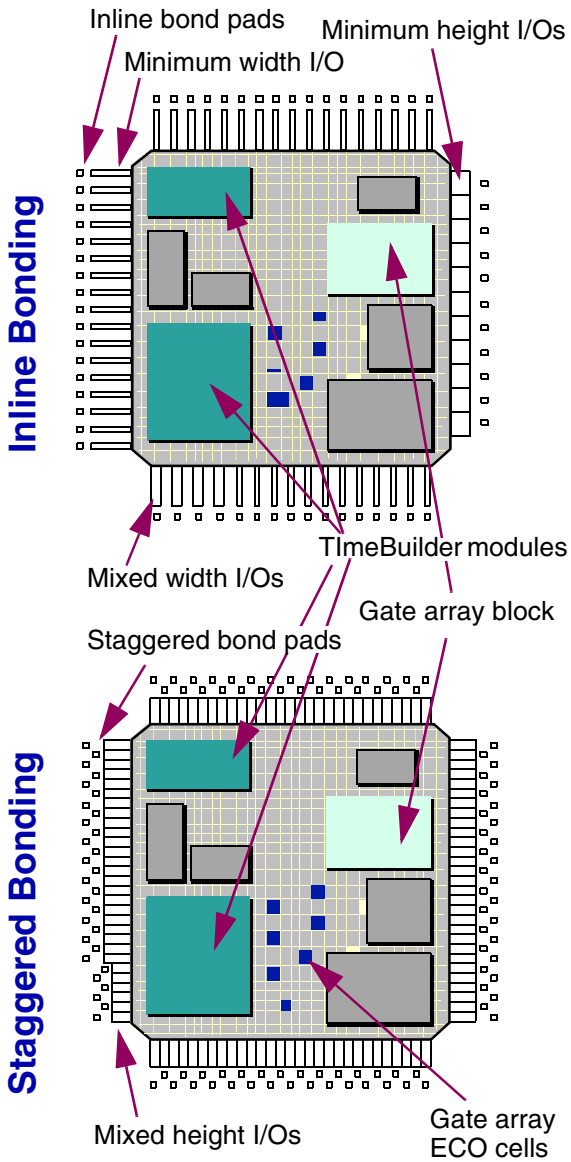
GS40 0.11-µm CMOS Standard Cell/Gate Array

Preliminary

High-Density, Low-Power ASIC

- **0.11-µm Ldrawn process** (0.08-µm L_{eff}) with Shallow Trench Isolation (STI)
- **Copper metal system with low-k dielectric**
- **5 and 6 levels of metal**
- **Density:** 156,000 gates/mm^2
- **Power supply:** 1.1/1.3/1.5 V cores I/Os: 1.8/2.5/2.75/3.3 V (selected combinations)
- **Power dissipation:** 11 nW/MHz/gate for 1.5-V core
- **Over 150 peripheral macros,** including LVCMOS, level-shifting I/Os, PCI, USB, oscillators
- **More than 300 core cells**
- **Extensive module selection**, including TMS 320 digital signal processors (DSPs), ARM™ 32-bit RISC microcontrollers, MIPS® Jade and Opal embedded processors, and analog functions
- **Memory compilers** including single-port (up to 450 Kbits/mm^2 at 1Mbit sizes), two-port, dual-port, ROM, and register file
- **TI ExSRAM** extremely high-density SRAM (>32 Mb of memory on a die)
- **Electrically-readable die ID**
- **Spare gate-array cells and gate-array blocks** for fast metal-level changes
- **Packages:** Flip-chip support to 1,672 pins, TQFP, MicroStar™ BGA (chip scale), plastic BGA, PowerPad



Features and Benefits

GS40 uses Texas Instruments TImeCell™ Architecture, which combines on the same silicon the cost-efficiency of standard cells with the fast time-to-market of gate arrays. TI provides a full range of product options to address the challenges of producing ultra-dense, low-power devices that take advantage of system integration.

The GS40 product family is positioned to take advantage of TI's world leadership in areas key to system-level integration and systems-on-a-chip design:

- World's leading supplier of embedded ARM™ and MIPS™ cores, including the ARM 7 and ARM 9 families of RISC processors, and MIPS Jade™ and Opal™ processors
- World's leading Digital Signal Processor (DSP) supplier
- Easy integration of DSP, ARM and MIPS cores with standard cell, gate-array logic and memories
- World's leading supplier of analog and data transmission solutions, including the IEEE 1394 link core, the Universal Serial Bus (USB) function controller, and the Universal Asynchronous Receiver/Transmitter (UART), 622 Mb/s Serdes transceiver core
- Proven design methodology with integrated hardware/software coverification
- Advanced 0.11-micron L_{drawn} process technology
- Superior design support and manufacturing— "no excuses" ramp to production

GS40 offers higher density and reduced die size, power and cost, or opportunity for more integration. Some key characteristics are shown in the table below (power dissipation numbers are preliminary).

Nominal core voltage	I/O voltage	Typical gate delay NA210, FO = 2	Typical design power dissipation
1.5 V	1.8, 2.5, 2.75, 3.3	40 ps	11 nW/MHz/gate
1.3 V	1.8, 2.5, 2.75, 3.3	100 ps	8.2 nW/MHz/gate
1.1 V	1.8, 2.5, 2.75, 3.3	150 ps	3.1 nW/MHz/gate

Advanced Technology

- **5- or 6- level metal**, with full Chemical Mechanical Polishing (CMP) planarization and fully stacked Tungsten vias.

Extensive Library for Density, Low Power, Value and Integration

- **Over 300 core macros**, including cells designed especially to meet high-performance requirements
- **A full range of inputs/outputs** (I/Os) in many specifications and voltages for speed and power trade-offs, including LVCMOS, PCI and USB
- **TImeBuilder module library and methodology and analog cells** for easy system-level integration
- **Memory compilers**, including synthesizable RAMs for more area efficiency in small RAM configurations
- **Fully characterized libraries** for accurate modeling
- **Sprinkled gate array cells** and gate array blocks for fast metal-level design changes late in the design cycle

Proven Methodology

- **TImePilot™ design system**, which offers a multi-vendor EDA strategy based on industry standards. This system, combined with enhancements in the design flow, simplifies and speeds the design process to help you achieve timing closure. An easy-to-use Design Sequencer steps you through the floorplanning process (built around a vendor-supplied floorplanner) and all of its associated design steps. See Table 7 on page 16 for a list of supported CAD tools.
- **Clock tree synthesis (CTS)** design flow that provides automatic synthesis of clock trees in physical design to meet designers' skew and insertion delay goals. The TI CTS flow supports more than 200 clock domains and clock gating for low power, and consistently achieves less than 50 ps clock skew.
- **Complete STA signoff methodology** enables comprehensive verification and minimizes gate-level simulation efforts at design hand-off. The Synopsys PrimeTime™-based signoff flow is supported with delay fault test generation capability using Sunrise™ tools.
- **SubChip™** design capabilities that support hierarchical design
- **VHDL and Verilog™ signoff flows** for reduced cycle time and improved accuracy
- **Synopsys™ Power Compiler™ support** for power reduction

Packaging for Value, Density and Performance

- **Package options** include thin quad flat pack (TQFP), MicroStar™ BGA, Plastic BGA, and PowerPad. For more details, see Table 6 on page 12.

Core and I/O Macro Summary

This summary of core and I/O macros lists the selections available from the library.

Performance Equations

Every timing path through each GS40 family core and I/O macro is characterized at multiple voltage, temperature, process, input slew, and output load points. No global derating with respect to voltage, temperature, or process is used with the GS40 family. The characterized data coupled with nonlinear delay modeling allows SPICE-like accuracy for a large range of operating conditions.

Library Description

The GS40 family macro library has been optimized for use with synthesis and power optimization tools. As a result, the GS40 family library features:

- A rich set of Boolean functions
- A wide variety of gates with inverting inputs
- Multiple-drive-strength gates
- Compact flip-flops and latches with Q only or QZ only
- Low-power combinational cells
- Minimized internal transistors in multistage macros
- Ultra-high-performance flip-flop and core macros
- Negative-edge flip-flops

A summary of core functions is shown in Table 1 on page 5.

Table 1: GS40 Family Core Macro Library Summary

Function	Number of macros
AND/NAND/OR/NOR	181
Exclusive-OR/Exclusive-NOR	23
Inverters	31
Buffers	13
Boolean functions	117
Multiplexers	39
D-type flip-flops	122
Latches	21
Clock macros	5
Clock-tree synthesis macros	47
Special functions/miscellaneous	16
Total	**615**

Analog functions include an 8-bit analog-to-digital converter (pipeline), a 10-bit successive approximation register (SAR), an analog clock squarer, a 10-bit digital-to-analog converter, a 3.3- to 1.5-V voltage regulator, high-frequency PLLs and a DPLL. The special function macros include electrically-readable die ID fuse-array macros.

Gate Array Macros

The GS40 macro library also includes gate array cells for ECO as shown in Table 2.

Table 2: Gate-Array Cells for ECO

Function	Number of macros
AND	2
OR	1
Buffers	8
D-type flip-flops	4
Exclusive-OR	1
Exclusive-NOR	2
Inverters	4
Latches	2
Multiplexers	2
NAND	8
NOR	8
Special functions/miscellaneous	7
Total	**49**

I/O Macros

GS40 provides 1.8, 2.5, 2.75, 3.3, and 3.3 V I/Os. Low-voltage CMOS (LVCMOS), PCI, and differential buffers are available. Most output buffers are available in two noise performance options: low noise and ultra-low noise. To minimize system noise and power pins, select the lowest noise output that the application allows. Ultra-low-noise I/Os typically require only one-fifth the number of power pins that high-performance I/Os require.

The user creates a bidirectional macro by selecting inputs and outputs and combining the functions in the netlist. You can add pullup and pulldown macros to I/Os in the same manner. I/O macros include:

- LVCMOS
- PCI, USB
- Low noise, ultra-low noise, ultra-low power, and failsafe options
- 1/1mA - 8/8 mA output drivers

Table 3: I/O Specifications

Type	Maximum Frequency	Signal Swing	Signal Type
LVCMOS	250 MHz	varies by V_{DDS}	single
PCI	66 MHz	3 V	single

Memories

GS40 supports synchronous single-port, two-port, and dual-port memory compilers and ROM, CAM and asynchronous two-port compilers. These dense memories let you specify the exact word and bit counts for each memory to meet the application's need. All memories can have synchronous operation, zero dc power and zero hold times.

Table 4: Memories Summary

Description	Max Bits	Min Bits	Max Words	Max Bits/ Word	Functionality
2-port SRAM (1W/1R)	32K	4	2K	64	Asynchronous
1-port Clocked RAM, density optimized, bit write	1Mbit	2K	32K	128	Single edge
1-port CRAM, density optimized, bit write, testability	2Mbit	2K	64K	64K	Single edge
1-port CROM, fast, via2 program	1Mbit	32	64K	64	Single edge
Dual-port CRAM, bit write	128K	64	4K	128	Single edge
1-port CRAM, multistrobe, page mode, low power	128K	1K	4K	64	Single edge
1-port CRAM, multistrobe, page mode, low power, testability	128K	512	4K	64	Single edge
2-port register file (1W/1R), bit write	32K	2	512	256	Single edge
1-port CRAM, area optimized, bit write	128K	32	2K	128	Single edge
1-port CROM, moat program	1Mbit	32	64K	64	Single edge
2-port CRAM (1W/1R), large, WE pin	128K	256	8K	128	Single edge

Single-Port Clocked SRAM Compiler

The single-port clocked SRAM compiler creates speed-optimized RAM blocks based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor. Contact the TI Customer Design Center for complete details.

Single-Port Clocked SRAM Compiler With Word-Write, Bit-Write and Multistrobe

In addition to the single-port clocked SRAM, TI also offers single-port memories with both word-write and bit-write capability. The bit-write capability enables you to update individual bits in the single port without changing the rest of the word. Multistrobe allows data to be read and/or written on up to three strobes.

Dual-Port Clocked SRAM Compiler

The dual-port clocked SRAM compiler creates area- and speed-optimized RAM based on user specifications. It creates data sheets, logic and layout models for simulation, testing, and layout based on the required number of words, number of bits per word, and the column multiplex factor.

Synthesizable Memories

For maximum flexibility, GS40 offers a number of memory options for use as “soft,” or synthesizable, memories. This compiler generates RTL (based on your specifications) as well as constraints for synthesis. Synopsys Design Compiler™ is then used to synthesize these memories to either flip-flop or latch-based implementation with support for multiple test methodologies. The compiler options, which are ideal for small RAM configurations, are:

- 1-port CRAM area optimized
- 2-port asynchronous RAM
- 2-port CRAM
- Dual-port RAM

TImeBuilder Modules

Texas Instruments has more than a decade of experience with complex integration and reuse for a wide variety of application-oriented markets. This experience gives TI a practical understanding of the challenges of integration; leadership in key integration areas gives TI the ability to offer unique solutions. TI is the world leader in digital signal processor (DSP) solutions, the world-leading supplier of data transmission peripherals, the world-leader in analog, and the world-leading supplier of ARM RISC processors (and also offers MIPS and NEC processors).

GS40 supports a wide variety of TImeBuilder modules for integrating complex functionality onto a single die. TImeBuilder gives you access to DSP technology from the company who invented it, and the ability to easily integrate it with a wide selection of core modules, including the ARM and MIPS Jade.

Table 5: TImeBuilder Modules

Processors and Peripherals	
TMS320C54X Digital Signal Processor	External memory controller (SDRAM, EDO, SRAM, ROM, flash)
ARM7TDMI	
ARM946	Multi-channel DMA controller
ARM966	Interrupt controller
ARM10	General-purpose timer
MIPS4kc Jade	Watchdog timer
MIPS4kp Jade Lite	Real-time clock (RTC)
MIPS4km	TMS320C54x standard peripherals
MIPS5k Opal	(McBSP, HPI)
ARC 32-bit RISC	
NECv850	
Bus Structures	
VBUS	Bus bridges, arbiters, controllers
AMBA (AHB, APB)	Processor-to-processor interface
Digital IP Functions	
10/100 Ethernet MAC	2.5 Gbps Serdes serial link
10/100 Ethernet PHY	Viterbi encoder/decoder
PCI controller (32-bit, 33/66 MHz)	RAMBUS (direct)
UART	General-purpose I/O (GPIO)
USART	1284 parallel interface
IrDA	1394 link core
Single-channel HDLC	IPSEC encryption
Multi-channel HDLC	DOCSIS MAC
I^2C master/slave	DOCSIS PHY
USB function and host controllers	NTSC/PAL encoder
Reed-Solomon encoder/decoder	

Analog IP Functions	
Analog-to-digital converters	Analog PLLs
Digital-to-analog converters	Voltage regulators
Digital PLLs	

Analog Cells

Analog cells include:

- Clock squarer with low power mode (dual gate only)
- Analog regulators
- Analog phase-locked loops, 100 - 750 MHz with zero-pin implementation and 150 - 1200 MHz with dedicated power and ground pins
- Analog input and output switches

Packaging

GS40 supports the package types shown below.

Table 6: Supported Packages

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
Thin Quad Flatpack (TQFP)	32	VF	7x 7x1.4	0.80
	48	PFB	7x 7x1.4	0.50
	52	PAH	10x10x1.0	0.65
	64	PAG	10x10x1.0	0.50
	80	PET	10x10x1.0	0.40
	80	PFC	12x12x1.0	0.50
	100	PZT	14x14x1.0	0.50
	128	PDT	14x14x1.0	0.40
	144	PGE	20x20x1.4	0.5
	176	PBL	20x20x1.4	0.5
	176	PGF	24x24x1.4	0.50
	208	PDV	24x24x1.4	0.50
	216	PDQ	24x24x1.4	0.40
MicroStar Ball Grid Array (USTARBGA)	64	GGV	8x 8x1.4	0.80
	80	GGM	10x10x1.4	0.80
	100	GGM	10x10x1.4	0.80
	100	GGB	12x12x1.4	0.80
	132	XXX	12x12x1.4	0.80
	144	GGU	12x12x1.4	0.80
	176	GGW	15x15x1.4	0.80
	196	GHC	15x15x1.4	1.00
	208	GGW	15x15x1.4	0.80
	240	GGW	15x15x1.4	0.80
	257	GHK	15x15x1.4	0.80
	257	GZG	16x16x1.4	0.80
	256	GFN	27x27	1.27
(STARBGA)	352	GHF	35x35x1.7	1.27
	432	GGZ	40x40x1.7	1.27
	520	GHM	40.x40x1.7	1.27
	600	GJM	40x40x1.7	1.27

Package	Pins	TI Suffix Code	Body Size (mm)	Lead Spacing (mm)
Plastic BGA	272	GFN	27x27	1.27
(PBGA)	352	GFT	35x35	1.27
	388	GFW	35x35	1.27
PowerPAD	64	PAP	10x10x1.0	0.50
	80	PFP	12x12x1.0	0.50
	100	PZP	14x14x1.0	0.50
	208	PYP	28x28x1.4	0.50
	216	RBP	24x24x1.4	0.40
	256	PFK	28x28x1.4	0.40

TImePilot Design Flow and CAD Tools

Fully characterized libraries account for the effects of voltage, temperature, process, load, and input rise and fall times. Hierarchical design viewing and editing, floorplanning, and timing analysis allow the designer to achieve the accurate representation of silicon through forward annotation of timing to the layout software. This design approach, shown in Figure 1 on page 15, gives designers full advantage of the high-performance characteristics that submicron CMOS technology offers.

The TI approach to open CAD enables easy interaction with other systems. Signoff quality libraries for all supported simulators, test vector verification software, and design-rule-checking software enable the customer to verify the design completely before handoff to TI, significantly shortening design cycle time and eliminating correlation issues. Synopsys VSS and Model Technology ModelSim™ simulation libraries conform to IEEE Std. 1076.4-1995–VITAL 95. Tools and libraries in the TImePilot design environment are supported on both Sun™ and HP™ workstations.

TImePilot uses the Avant! Jupiter™ floorplanner. TI has added several features to the floorplanning flow, including a sequencer that steps users through all floorplanning-related tasks. Many traditional place-and-route features are now available in the floorplanner to help achieve first-pass timing convergence. Other features include:

- Gate-level floorplanning
- SubChips for reuse (see “Design Reuse” on page 17)
- Clock tree synthesis, a flexible, low-power strategy for clock distribution (see “Clock Tree Synthesis (CTS)” on page 18
- Team design
- Path timing-driven placement
- Rules-driven placement
- Floorplan checks
- Wide-wire support for power management
- ECO

The primary aim of the design flow is to offer state-of-the art design tools and a highly productive environment to enable designers to achieve error-free designs in the shortest time that meets timing goals. The flow is also designed to comprehend the effects of deep submicron technology by accurately estimating interconnection lengths and resistance-capacitance (RC) effects, and by providing close correlation between floorplanning and synthesis and pre- to postlayout delays.

Figure 1: Design Flow Overview

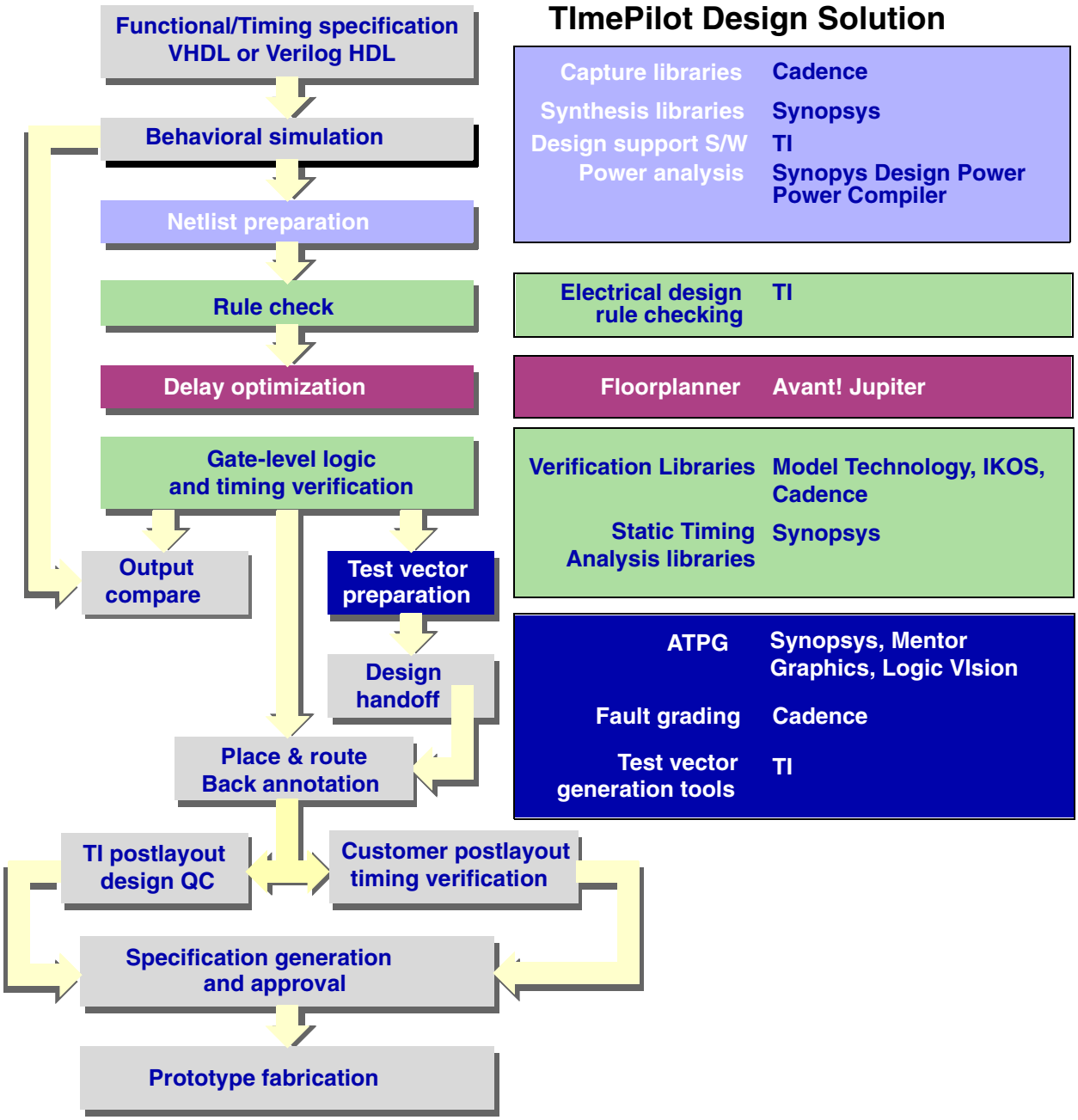


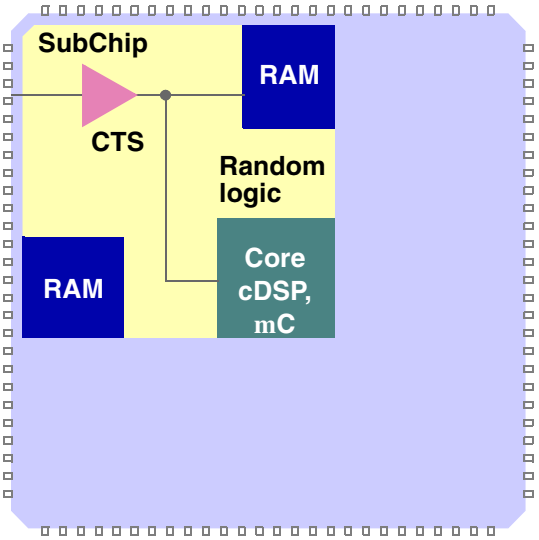
Table 7: TImePilot CAD Tool Support

Platform/Tool	Options
Hardware platforms and operating systems	Sun ULTRAsparc™ platforms (Solaris 2.7, 2.5.1/2.6) HP9000 (HP-UX™ 11, 10.20 with patch PHSS_15043) (C++HP 10.36) (aCC 1.18)
Architectural synthesis	Synopsys Behavioral Compiler
Limited synthesis	Synopsys ECO Compiler
Logic synthesis	Synopsys DC Professional/Expert
Formal verification	Chrysalis Design VERIFYer™, Synopsys Formality™
RAM compilation	Web-based ACE toolkit
Floorplanning	Avant! Jupiter™
Simulation	Mentor Graphics ModelSim™, Verilog-XL™, NC Verilog, IKOS Voyager NSIM CS/CSX™
Datapath	Synopsys DesignWare™
Static Timing Analysis (STA) signoff	Synopsys Primetime™
Logic design rule checking	Detector™
Test vector verification	SimOut™
Test vector generation	TDLGEN™
Test vector rule checking	TDLCHKR™
Automatic place and route	Avant! Apollo™
Test synthesis and ATPG	Synopsys TetraMAX™, Synopsys/Viewlogic Sunrise™, Mentor Graphics FastScan™, FlexText™, DFT Advisor™, LogicVision MEMBIST II
Fault grading	Cadence Verifault™
Evaluation	Paragon™
Power	Synopsys DesignPower™, DesignCompiler™

Design Reuse

A SubChip is a design module that undergoes placement and routing as a discrete block that can be reused as a component of a larger design, as illustrated in Figure 9. When reused, the placement and routing of the SubChip stay the same so that its previous functionality and timing are preserved. This capability allows for independent optimization of design modules and provides increased designer productivity through module reuse. SubChips can be used on multiple designs.

Figure 2: SubChip Components



A SubChip can include:

- TImeBuilder modules
- Clock tree synthesis (CTS)
- Random logic
- Cores
- Analog cells
- Other SubChips

Some benefits of SubChips include:

- They are user- or TI-defined functions with known postlayout timing, area, and power that can be used in prelayout chip designs and simulations.
- Multiple instances can be placed in a design and will have identical timing.
- SubChips can be used by multiple designs.
- Complex designs can be implemented and/or easily modified by the designer without the difficult modeling or characterization associated with a complex hard macro design.

Clock Tree Synthesis (CTS)

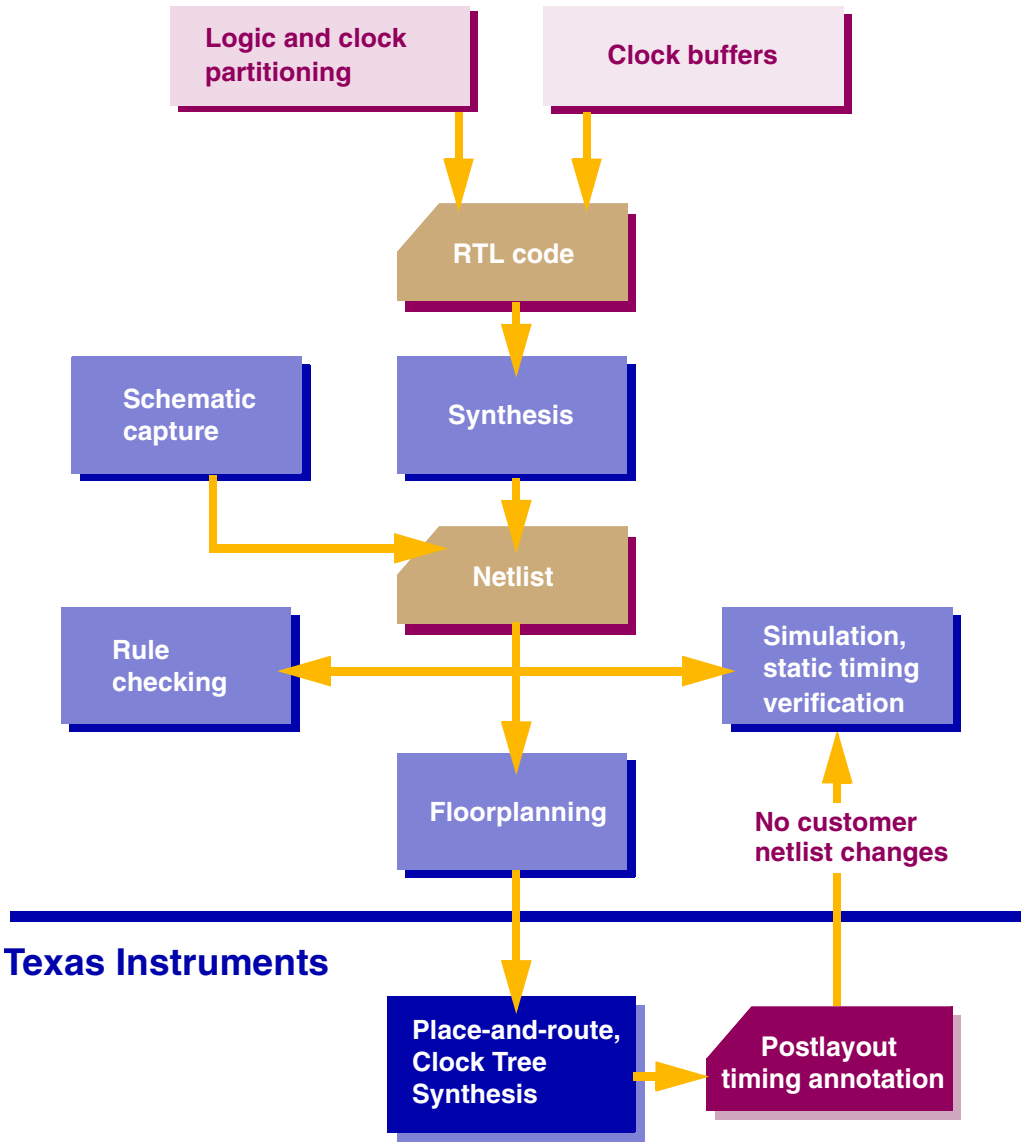
Clock tree synthesis (CTS), shown in Figure 3 on page 19, is the primary method of clock distribution for GS40 family standard cell designs. The key capabilities of the CTS flow are:

- Insertion delay, skew, and power management
- Capability to handle more than 200 clocks
- Gated clock support for lower power
- Ability to balance multiple clocks together
- Easy to use in design flow
- Good prelayout to postlayout correlation
- Layout-centered approach for lowest skew and delay
- No customer netlist modifications
- Balancing into a SubChip
- One CTS macro
- Automatic clock buffer selection

With clock tree synthesis, the customer instantiates a single CTS buffer per clock tree. The CTS buffer is expanded at layout into a multistage clock tree. The configuration of the clock tree is optimized for size, delay, and power in accordance with the requirements of the application, and the clock tree is placed according to the location of its loads.

The postlayout timing of the clock tree is back annotated to the customer's original netlist. The insertion delay is annotated as CTS buffer gate delay, and the clock skew is annotated to the input pin of the individual loads. Clock tree balancing and tuning are accomplished automatically by insertion of tuning buffers and loads at the root of the clock tree.

Figure 3: Clock Tree Synthesis Flow



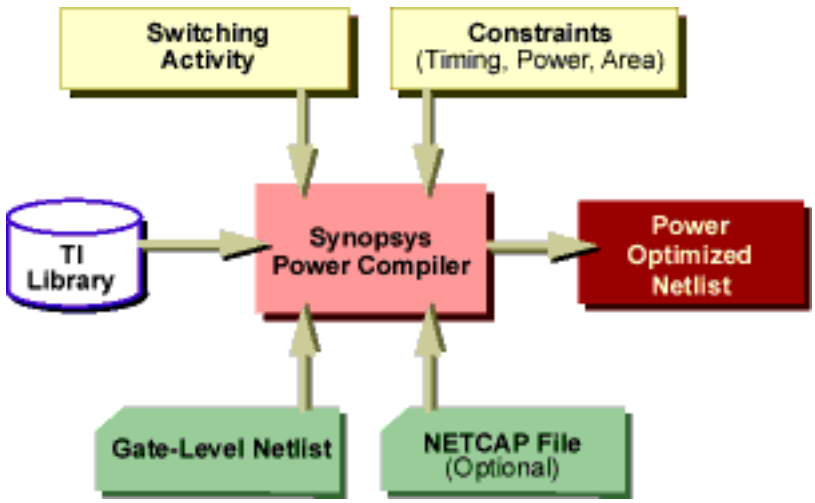
Power Analysis and Optimization

To achieve a low system power, the GS40 family provides:

- Support for Synopsys Power Compiler and DesignPower
- 1.1-V, 1.3-V, and 1.5-V libraries
- Core macros optimized for low power
- Optimized library for efficient synthesis, lowering net count and gate count to reduce power
- Full support for gated clock methodologies, which reduce switching activity through clock tree synthesis and clock balancing capabilities.
- Low-power and ultra-low-power I/Os
- TImeBuilder modules that draw zero dc current

To optimize gate-level power, the GS40 family fully supports the Synopsys power optimization tool, Power Compiler. A design flow using Power Compiler is shown in Figure 3.

Figure 4: Design Flow Using Power Compiler



To analyze how much power is actually dissipated in a specific netlist, the GS40 family supports the Synopsys power analysis tool, DesignPower. A design flow using DesignPower is shown in Figure 4.

Figure 5: Power Estimation Using Synopsys DesignPower