GS1503
HD EMBEDDED AUDIO CODEC

DATA SHEET

GS1503

FEATURES

- complies with SMPTE 292M and SMPTE 299M
- single chip HD embedded audio solution
- operates as an embedded audio multiplexer or demultiplexer
- full support for 48kHz synchronous 24-bit audio
- support for 8 channels of audio per device
- cascadable architecture supports up to 16 audio channels
- integrated scrambler/descrambler and word alignment
- CRC error detection and insertion
- audio control packet insertion and extraction
- arbitrary data packet insertion and extraction
- 3.3V power supply with 5V tolerant I/O
- 144 pin LQFP package

APPLICATIONS

HD SDI Embedded Audio

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS1503-CFZ	144 pin LQFP	0°C to 70°C

DESCRIPTION

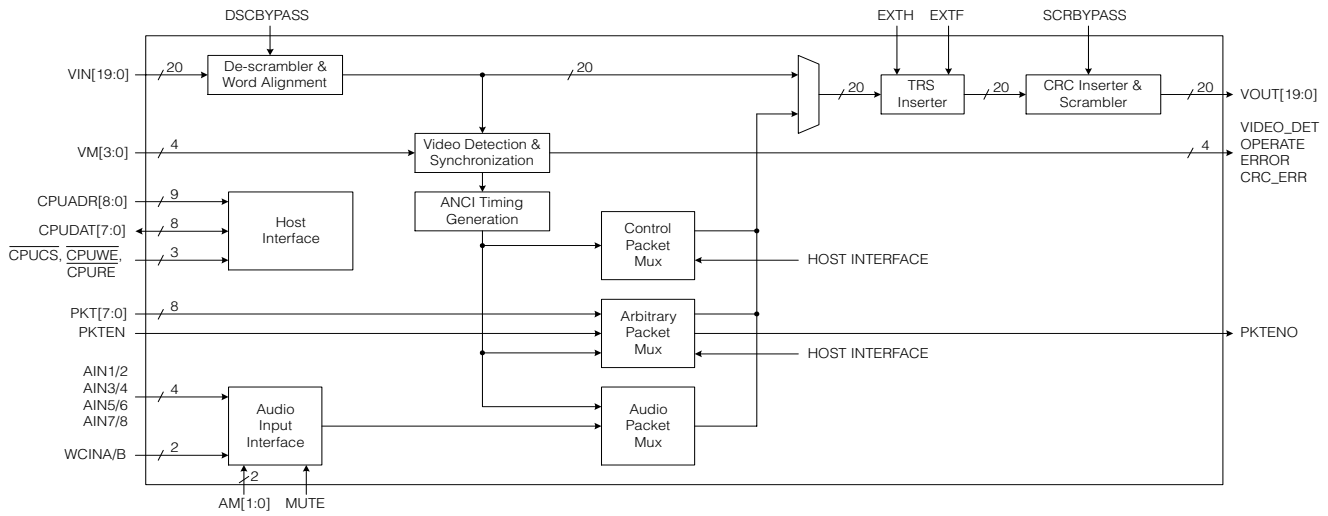
The GS1503 is a highly integrated, single chip solution for embedding/extracting digital audio streams into and out of high definition digital video signals. The GS1503 supports insertion/extraction of 24-bit synchronous audio data with a 48kHz sample rate. Audio signals with different sample rates may be converted to 48kHz by using audio sample rate converters before or after the GS1503.

Each GS1503 supports all processing required for embedding/extracting up to eight digital audio channels in the horizontal ancillary data space of the video chroma channel. Two GS1503's can be cascaded for insertion/extraction of up to 16 audio channels with no external glue logic.

The GS1503 supports embedding/extracting of audio control and arbitrary data packets in the horizontal ancillary data space of the video luma channel. It also supports line CRC detection and insertion.

The GS1503 supports HD video standards at 74.25MHz and 74.25/1.001MHz rates. It has an on chip SMPTE compliant scrambler/de-scrambler, and integrated word alignment. Use the GS1503 with Gennum's GS1545 or GS1522 for two chip HD SDI receive or transmit solutions.

The GS1503 operates from a single 3.3V power supply with 5V tolerant I/O and is packaged in a 144 pin LQFP package.



MULTIPLEX MODE BLOCK DIAGRAM

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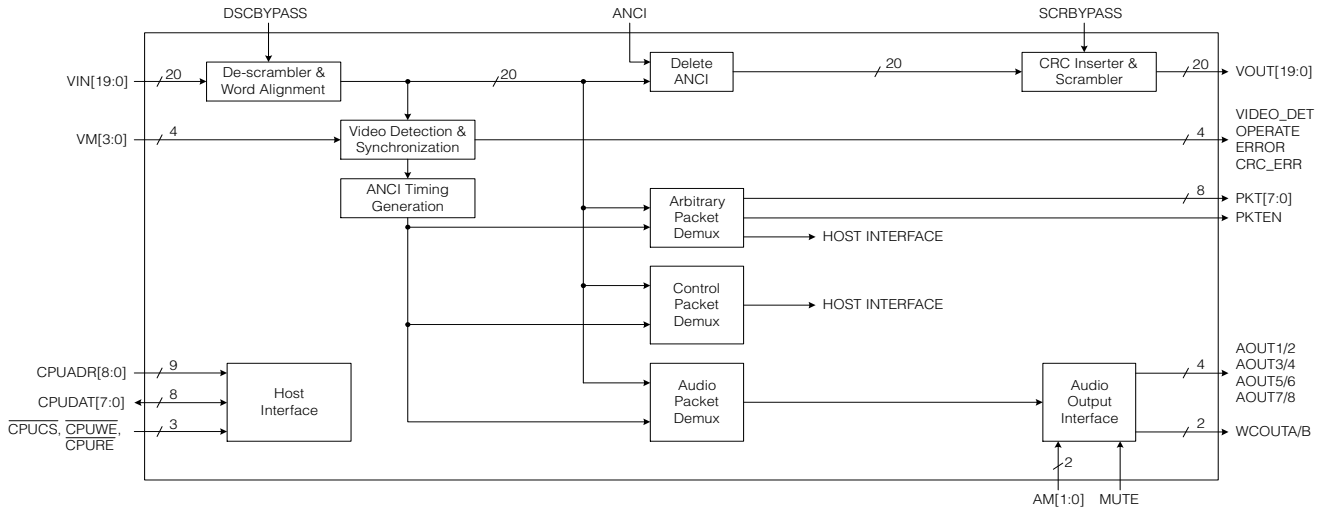


DEMULTIPLEX MODE BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage	-0.3V to 4.0V
Input Voltage (any input)	-0.3 to 5.5V
Operating Temperature	0°C to 70°C
Storage temperature	-65°C to 150°C
Lead Temperature (soldering, 10 sec.)	230°C

DC ELECTRICAL CHARACTERISTICS

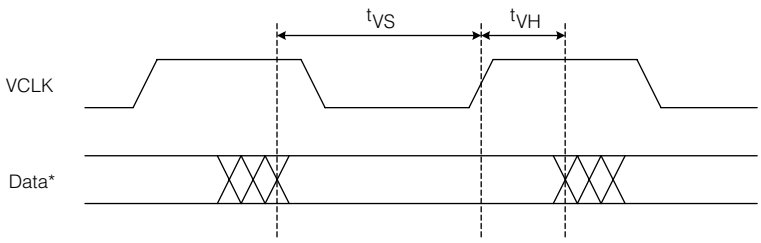
T_A = 0°C to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}	3.3V operating range	3.0	3.3	3.6	V
Supply Current	I_{DD}	V_{DD} = 3.3V		270		mA
Input Current	I_{IN}		-1	-	1	µA
Hi-Z Output Leakage Current	I_{OZ}		-1	-	1	µA
Output Voltage, Logic High	V_{OH}	I_{OH} = -12mA	V_{DD}-0.4	-	-	V
Output Voltage, Logic Low	V_{OL}	I_{OL} = 12mA	-	-	0.4	V
Input Voltage, Logic High	V_{IH}	TTL Level	2.0	-	-	V
Input Voltage, Logic Low	V_{IL}	TTL Level	-	-	0.8	V
Input Capacitance	C_I	f = 1MHz, V_{DD} = 0V	-	-	10	pF
Output Capacitance	C_O	f = 1MHz, V_{DD} = 0V	-	-	10	pF
I/O Capacitance	C_{IO}	f = 1MHz, V_{DD} = 0V	-	-	10	pF

AC ELECTRICAL CHARACTERISTICS

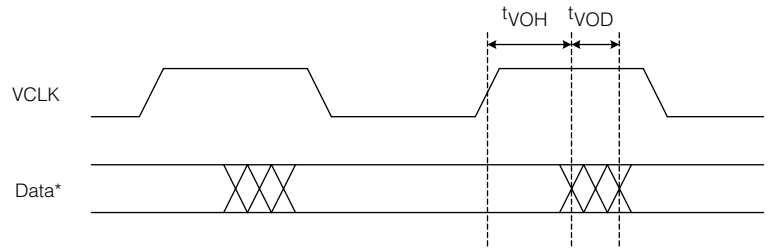
V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Video Clock Frequency			-	74.25	80	MHz
Video Clock Pulse Width Low	t_{VPWL}		5.0	-	-	ns
Video Clock Pulse Width High	t_{VPWH}		5.0	-	-	ns
Video Input Data Setup Time	t_{VS}		3.5	-	-	ns
Video Input Data Hold Time	t_{VH}		1.0	-	-	ns
Video Output Data Delay Time	t_{VOD}	With 10pF loading	-	-	8.5	ns
Video Output Data Hold Time	t_{VOH}	With 10pF loading	1.0	-	-	ns
Audio Clock Frequency			-	6.144	-	MHz
Audio Clock Pulse Width Low	t_{APWL}		60	-	-	ns
Audio Clock Pulse Width High	t_{APWH}		60	-	-	ns
Audio Input Data Setup Time	t_{AS}		10.5	-	-	ns
Audio Input Data Hold Time	t_{AH}		1.0	-	-	ns
Audio Output Data Delay Time	t_{AOD}	With 10pF loading	-	-	20.0	ns
Audio Output Data Hold Time	t_{AOH}	With 10pF loading	1.0	-	-	ns
Reset Pulse Width	t_{RESET}		1	-	-	ms
Device Latency		Multiplexer Mode Demultiplexer Mode	53 53	53 53	53 53	PCLKs



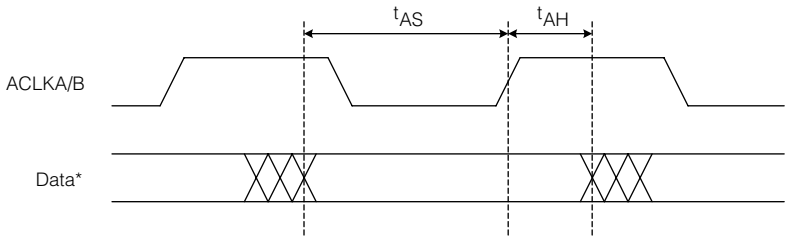
* VIN[19:0], EXTF, EXTH, PKTEN, PKT[7:0]

Fig. 1 Video Data Input Setup & Hold Time



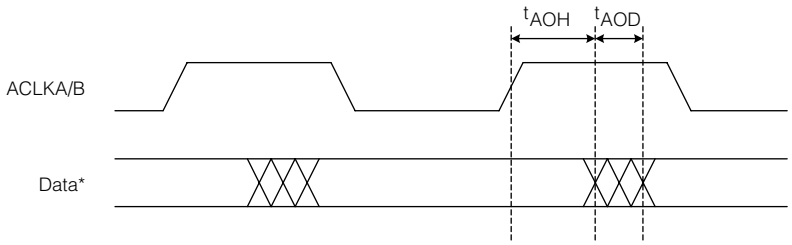
* VOUT[19:0], EXTF, EXTH, PKTEN, PKT[7:0]

Fig. 2 Video Data Output Delay & Hold Time



* WCINA, AIN1/2, AIN3/4, WCINB, AIN5/6, AIN7/8

Fig. 3 Audio Data Input Setup & Hold Time



* AOUT1/2, AOUT3/4, AOUT5/6, AOUT7/8

Fig. 4 Audio Data Output Delay & Hold Time

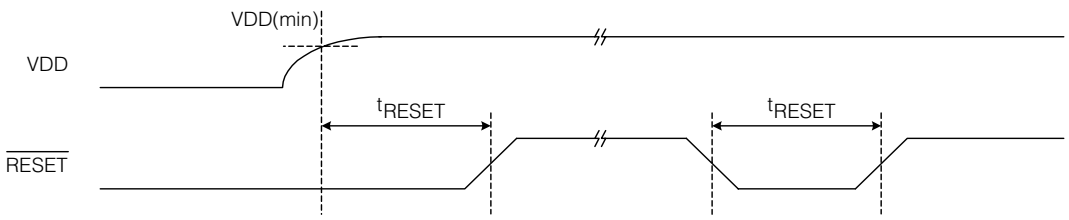


Fig. 5 Reset Timing

HOST INTERFACE

Mode A (CPU_SEL set HIGH)

PARAMETER	NUMBER	MIN	TYP	MAX	UNITS
Read Cycle Time	1	50	-	-	ns
Read Chip Select Setup Time	2	0	-	-	ns
Read Address Setup Time	3	15	-	-	ns
Read Data Output Delay Time	4	-	-	15	ns
Read Data Hold Time	5	0	-	-	ns
Write Cycle Time	6	50	-	-	ns
Write Chip Select Setup Time	7	10	-	-	ns
Write Address Setup Time	8	10	-	-	ns
Write Data Setup Time	9	10	-	-	ns
Write Data Hold Time	10	0	-	-	ns

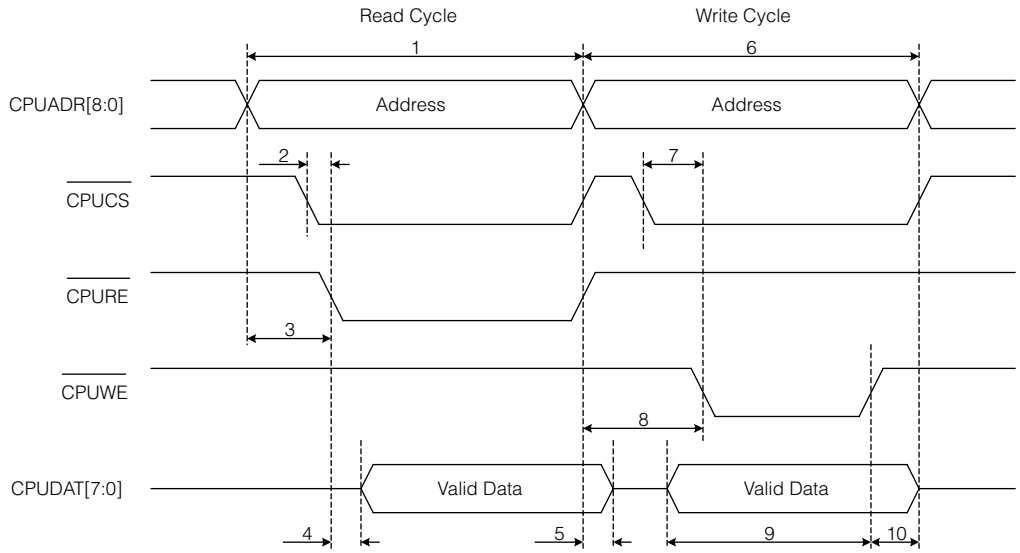


Fig. 6 Host Interface Mode A Timing (CPU_SEL set HIGH)

Mode B Read Cycle (CPU_SEL set LOW)

PARAMETER	NUMBER	MIN	TYP	MAX	UNITS
Read Address Cycle Time	1	80	-	-	ns
Read Cycle Time	2	80	-	-	ns
Read Enable Setup Time	3	20	-	-	ns
Read Address Setup Time	4	20	-	-	ns
Read Chip Select Setup Time	5	10	-	-	ns
Read Chip Select Hold Time	6	0	-	-	ns
Read Data Output Delay Time	7	-	-	10	ns
Read Data Hold Time	8	0	-	-	ns

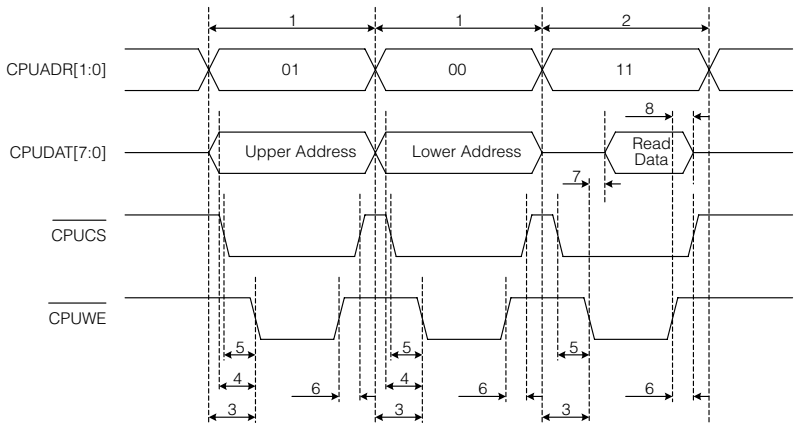


Fig. 7 Host Interface Mode B Read Cycle Timing (CPU_SEL set LOW)

Mode B Write Cycle (CPU_SEL set LOW)

PARAMETER	NUMBER	MIN	TYP	MAX	UNITS
Write Address Cycle Time	1	80	-	-	ns
Write Cycle Time	2	80	-	-	ns
Write Enable Setup Time	3	20	-	-	ns
Write Address Setup Time	4	20	-	-	ns
Write Chip Select Setup Time	5	10	-	-	ns
Write Chip Select Hold Time	6	0	-	-	ns
Write Data Setup Time	7	30	-	-	ns
Write Data Hold Time	8	0	-	-	ns

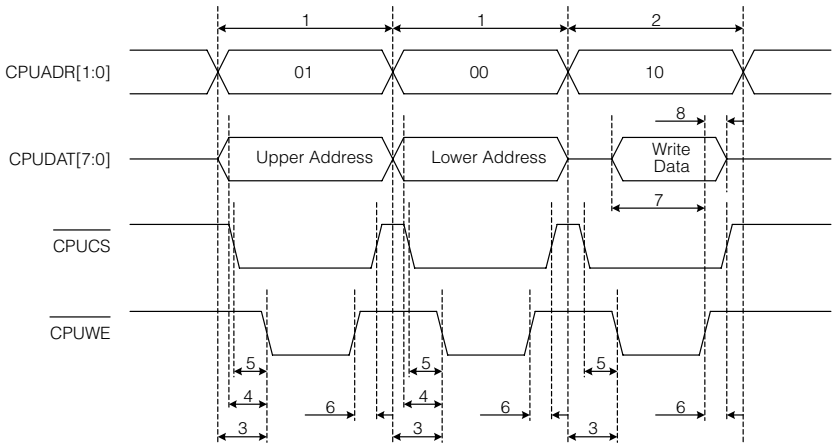
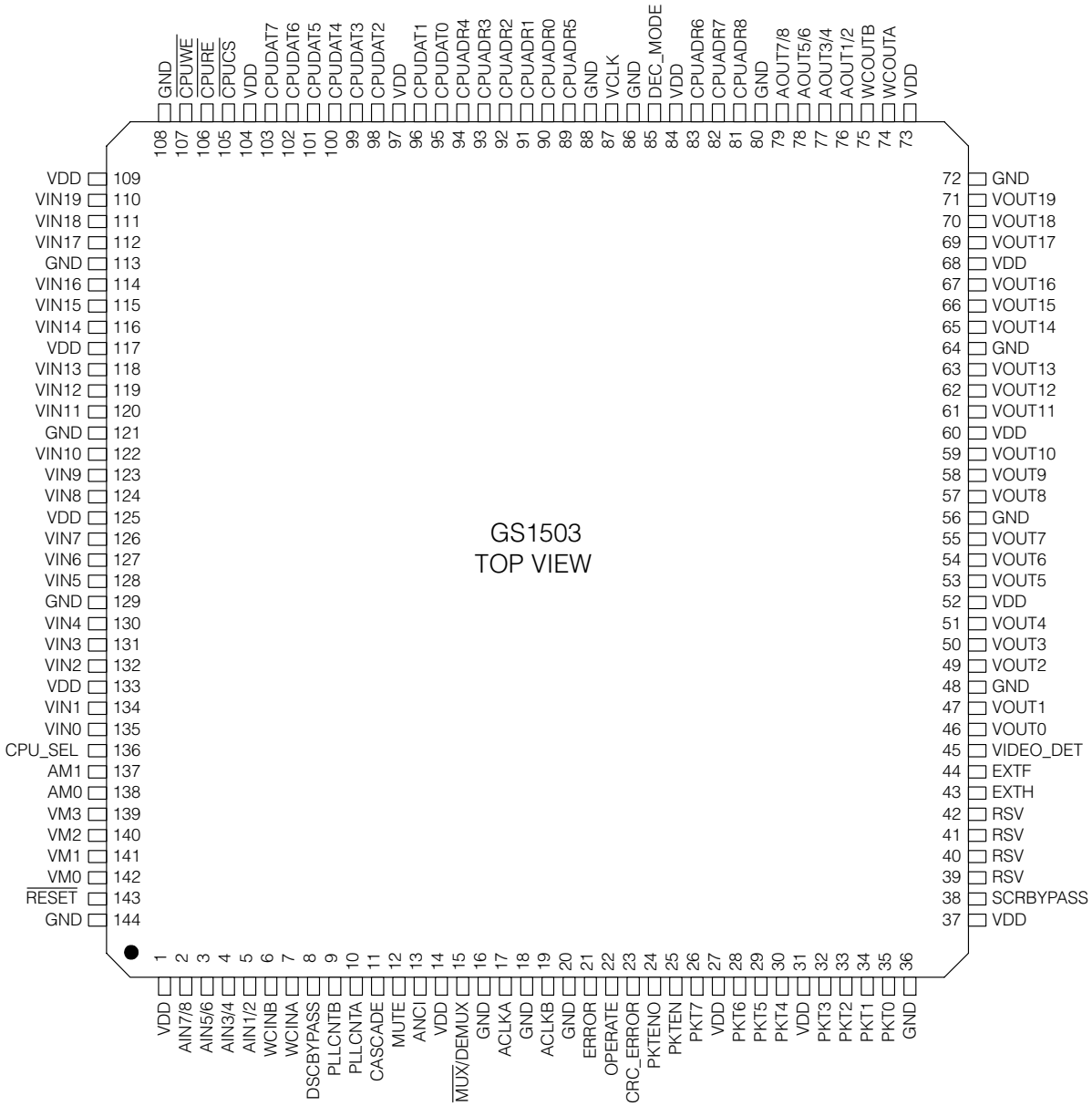


Fig. 8 Host Interface Mode B Write Cycle Timing (CPU_SEL set LOW)

Table 1: Host Interface Mode B Control Codes

CPUADR[1:0]	Data Bus Operation
01	Upper Address
00	Lower Address
11	Read Data
10	Write Data

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	TYPE	DESCRIPTION
1, 14, 27, 31, 37, 52, 60, 68, 73, 84, 97, 104, 109, 117, 125, 133	VDD	-	+3.3V power supply pins.
2	AIN7/8	I	Audio signal input for channels 7 and 8. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
3	AIN5/6	I	Audio signal input for channels 5 and 6. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
4	AIN3/4	I	Audio signal input for channels 3 and 4. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
5	AIN1/2	I	Audio signal input for channels 1 and 2. AES/EBU digital audio data is bi-phase mark encoded. For all non-AES/EBU input modes, bi-phase mark encoding is not required.
6	WCINB	I	48kHz word clock for channels 5 to 8. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode (DEC_MODE set LOW).
7	WCINA	I	48kHz word clock for channels 1 to 4. Used only when operating in Multiplex Mode and when the audio source is not an AES/EBU data stream. This pin should be grounded when inputting AES/EBU digital audio data or when operating in Demultiplex Mode (DEC_MODE set LOW).
8	DSCBYPASS	I	Descrambler bypass. When set LOW, the internal SMPTE 292M descrambler is enabled. When set HIGH, the internal SMPTE 292M descrambler is bypassed. The video input to the device must be word aligned.
9	PLLCNTB	O	Audio clock PLL control signal for channels 5 to 8.
10	PLLCNTA	O	Audio clock PLL control signal for channels 1 to 4.
11	CASCADE	I	Cascade mode select. When set HIGH, the GS1503 will default to audio groups 3 and 4. Two GS1503 devices can then be cascaded in series to allow up to 16 channels of audio to be multiplexed or demultiplexed (only one device requires CASCADE to be set HIGH). When set LOW, the GS1503 will default to audio groups 1 and 2.
12	MUTE	I	Audio mute. In Multiplex Mode, when set HIGH, the embedded audio packets are forced to '0'. In Demultiplex Mode, when set HIGH, the audio output data is forced to "0".
13	ANCI	I	Ancillary data delete select. Valid in Demultiplex Mode only. When set HIGH, all ancillary data packets are removed from both the Luma and Chroma channels of the input video signal. The data contained in the packets are output at the corresponding pins. When set LOW, all ancillary data packets remain in the video signal. *See Section 2-11.*
15	$\overline{\text{MUX}}$/DEMUX	I	Mode of operation. When set LOW, the GS1503 operates in Multiplex Mode. When set HIGH, the GS1503 operates in Demultiplex Mode.
16, 18, 20, 36, 48, 56, 64, 72, 80, 86, 88, 108, 113, 121, 129, 144	GND	-	Device ground.
17	ACLKA	I	Input audio signal clock at 6.144 MHz (128 fs) for channels 1 to 4.
19	ACLKB	I	Input audio signal clock at 6.144 MHz (128 fs) for channels 5 to 8.
21	ERROR	O	Format error indicator. When HIGH, the incoming video data stream contains TRS errors or there are errors within the incoming ancillary data packets.

PIN DESCRIPTIONS (Continued)

NUMBER	SYMBOL	TYPE	DESCRIPTION
22	OPERATE	O	Audio processing indicator. When HIGH, audio data is being multiplexed or demultiplexed.
23	CRC_ERROR	O	CRC error indicator. Will be set HIGH when a CRC error is detected in the incoming video data stream.
24	PKTENO	O	Arbitrary data packet timing signal. Valid in Multiplex Mode only. Will be HIGH when arbitrary data packets can be input to the device. This signal is only valid when multiplexing arbitrary data packets via the PKT[7:0] bus. *See Figure 30 for timing.*
25	PKTEN	I/O	Arbitrary data packet enable. In Multiplex Mode, PKTEN is an input and must be set HIGH two VCLK cycles after the PKTENO signal goes HIGH. Arbitrary packet data is input to the device two VCLK cycles after PKTEN is set HIGH. In Demultiplex Mode, PKTEN is an output and is set HIGH two VCLK cycles before the device outputs arbitrary packet data. *See Figures 30 and 42.*
26, 28, 29, 30, 32, 33, 34, 35	PKT[7:0]	I/O	Arbitrary data I/O bus. PKT[7] is the MSB and PKT[0] is the LSB. In Multiplex Mode, the user must input the arbitrary data packet words starting from the data identification (DID) to the last user data word (UDW) according to SMPTE 291M. The GS1503 internally converts the data to 10 bits by generating the parity bit (bit 8) and inversion bit (bit 9). The checksum (CS) word is also generated internally. In Demultiplex Mode, the GS9023 outputs the arbitrary data packet words starting from the DID to the last UDW. *See Figures 30 and 42.*
38	SCRBYPASS	I	Scrambler bypass. When set LOW, the output video stream is scrambled according to SMPTE 292M and NRZ(I) encoded. When set HIGH, the scrambler and NRZ(I) encoder are bypassed.
39, 40, 41, 42	RSV	-	Connect to ground.
43	EXTH	I/O	Horizontal sync signal. The GS1503 outputs a horizontal sync signal derived from the incoming TRS. In Multiplex Mode, with EXT_SEL set HIGH in the Host Interface, a horizontal sync signal can be input to the device for TRS and line number insertion.
44	EXTF	I/O	Field sync signal. The GS1503 outputs a field sync signal derived from the incoming TRS. In Multiplex Mode, with EXT_SEL set HIGH in the Host Interface, a field sync signal can be input to the device for TRS and line number insertion. For progressive formats, a signal with a high to low transition at the position of line one must be provided. *See Figures 14 and 15.*
45	VIDEO_DET	O	Video input signal detection. Indicates that the device has detected a valid video input stream. NOTE: When EXT_SEL is set HIGH in the Host Interface, VIDEO_DET will indicate when valid EXTH and EXTF signals have been detected.
71, 70, 69, 67, 66, 65, 63, 62, 61, 59, 58, 57, 55, 54, 53, 51, 50, 49, 47, 46	VOUT[19:0]	O	Parallel digital video signal output. VOUT[19] is the MSB and VOUT[0] is the LSB.
74	WCOUTA	O	48kHz word clock for channels 1 to 4. Valid only when operating in Demultiplex Mode.
75	WCOUTB	O	48kHz word clock for channels 5 to 8. Valid only when operating in Demultiplex Mode.
76	AOUT1/2	O	Audio signal output for channels 1 and 2. The AES/EBU digital audio output is bi-phase mark encoded. In both non-AES/EBU modes, the output is not bi-phase mark encoded.
77	AOUT3/4	O	Audio signal output for channels 3 and 4. The AES/EBU digital audio output is bi-phase mark encoded. In both non-AES/EBU modes, the output is not bi-phase mark encoded.
78	AOUT5/6	O	Audio signal output for channels 5 and 6. The AES/EBU digital audio output is bi-phase mark encoded. In both non-AES/EBU modes, the output is not bi-phase mark encoded.

PIN DESCRIPTIONS (Continued)

NUMBER	SYMBOL	TYPE	DESCRIPTION
79	AOUT7/8	O	Audio signal output for channels 7 and 8. The AES/EBU digital audio output is bi-phase mark encoded. In both non-AES/EBU modes, the output is not bi-phase mark encoded.
85	DEC_MODE	I	Demultiplex Mode select. Valid in Demultiplex Mode only. When set HIGH, the GS1503 requires a 48kHz word clock input at WCINA and WCINB. This word clock must be synchronous to the word clock used to embed the audio data. The embedded audio clock phase information in the ancillary data packet will be ignored. *See Section 2-12.*
87	VCLK	I	Video clock signal input.
81, 82, 83, 89, 94, 93, 92, 91, 90	CPUADR[8:0]	I	Host Interface address bus. CPUADR[8] is the MSB and CPUADR[0] is the LSB. In Host Interface Mode B (CPU_SEL set LOW), CPUADR[1:0] are used as the Host Interface control bus. *See Table 1.*
103, 102, 101, 100, 99, 98, 96, 95	CPUDAT[7:0]	I/O	Host Interface data bus. CPUDAT[7] is the MSB and CPUDAT[0] is the LSB. In Host Interface Mode B (CPU_SEL set LOW), CPUDAT[7:0] are used as the Host Interface address and data bus.
105	$\overline{\text{CPUCS}}$	I	Chip select for Host Interface. Active LOW.
106	$\overline{\text{CPURE}}$	I	Read enable for Host Interface. Active LOW. In Host Interface Mode B (CPU_SEL set LOW), this input is not used.
107	$\overline{\text{CPUWE}}$	I	Write enable for Host Interface. Active LOW. In Host Interface Mode B (CPU_SEL set LOW), this input is used as the Host Interface control enable.
110, 111, 112, 114, 115, 116, 118, 119, 120, 122, 123, 124, 126, 127, 128, 130, 131, 132, 134, 135	VIN[19:0]	I	Parallel digital video signal input. VIN[19] is the MSB and VIN[0] is the LSB.
136	CPU_SEL	I	Host Interface mode select. When set HIGH, the GS1503 is configured for Host Interface Mode A. When set LOW, the GS1503 is configured for Host Interface Mode B.
137, 138	AM[1:0]	I	Audio format select. In Multiplex Mode, AM[1:0] indicates the input audio data format. In Demultiplex Mode, AM[1:0] indicates the output audio data format. AM[1] is the MSB and AM[0] is the LSB. *See Tables 3 and 11.*
139, 140, 141, 142	VM[3:0]	I	Video standard select. VM[3] is the MSB and VM[0] is the LSB. *See Table 2 or 10.*
143	$\overline{\text{RESET}}$	I	Device reset. Active LOW.

DETAILED DESCRIPTION

1. MULTIPLEX MODE

1.1 FUNCTIONAL OVERVIEW

The GS1503 HD Embedded Audio CODEC fully supports the multiplexing of Audio Data Packets, Audio Control Packets and Arbitrary Data Packets as per SMPTE 291M and 299M. The device can be configured to operate with all video standards defined in SMPTE 292M, levels A through M. The GS1503 also supports the 1080/24PsF, 25PsF and 30PsF video formats as described in SMPTE RP211.

The video input format can be one of the following configurations:

10-bit Y and C_b/C_r input with TRS and Line Numbers

8-bit Y and C_b/C_r input with TRS and Line Numbers

10-bit or 8-bit Y and C_b/C_r input without TRS and Line Numbers (GS1503 will insert TRS and Line Numbers based on EXTF and EXTH inputs)

20-bit scrambled input

The video output format can be one of the following configurations:

20-bit scrambled output

10-bit Y and C_b/C_r output

Up to a maximum of 8 channels of 48kHz digital audio can be multiplexed per device. The audio input format can be selected as either AES/EBU, or one of two serial audio data input modes. A maximum of 16 channels of audio can be multiplexed by serially cascading two devices.

Audio control packets, as defined in SMPTE 299M, can also be multiplexed to provide information to receivers about the nature of the embedded audio data. The contents of the audio control packet can be programmed via the Host Interface.

The GS1503 will also multiplex arbitrary data packets as defined in SMPTE 291M. The arbitrary data packets can serve as an auxiliary data signal for proprietary applications. The GS1503 can be configured to multiplex arbitrary data packets, input via the Host Interface or using dedicated external pins. Up to a maximum of 255 8-bit words can be multiplexed (excluding Ancillary Data Flags and Checksum).

To use the GS1503 in Multiplex Mode, set the $\overline{\text{MUX}}$/DEMUX external pin LOW.

1.2 VIDEO STANDARD

The video standard is selected from the VM[3:0] external pins or VM[3:0] bits 3-0 in Host Interface register 000h. To configure the video standard via the Host Interface, VM_SEL bit 7 in Host Interface register 000h must be set HIGH. The GS1503 will default to the VM[3:0] external pin setting. The supported video standards are listed in Table 2.

Table 2: Supported Video Standards

VM [3:0]	INPUT FORMAT	REFERENCE SMPTE DOCUMENT	SMPTE 292M LEVEL
1110b	1035i (30 & 30/1.001 Hz)	260M	A, B
1100b	1080i (25 Hz)	295M	C
1000b	1080i/1080sF (30 & 30/1.001 Hz)	274M, RP211	D, E
1010b	1080i/1080sF (25 Hz)	274M, RP211	F
1111b	1080sF (24 & 24/1.001 Hz)	RP211	
0010b	1080p (30 & 30/1.001 Hz)	274M	G, H
0100b	1080p (25 Hz)	274M	I
0110b	1080p (24 & 24/1.001 Hz)	274M	J, K
0000b	720p (60 & 60/1.001 Hz)	296M	L, M
0001b	720p (30 & 30/1.001 Hz)	296M	
0011b	720p (50 Hz)	296M	
0101b	720p (25 Hz)	296M	
0111b	720p (24 & 24/1.001 Hz)	296M	
All other settings are reserved			

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VM_SEL	0: External pin select 1: Register select	000	7	1	0
VM[3:0]	Video formal selection (VM[3] is MSB)		3-0	*See Table 2*	0

1.3 VIDEO INPUT FORMAT

1.3.1 10-bit Y and C_b/C_r Input Video with TRS and Line Numbers

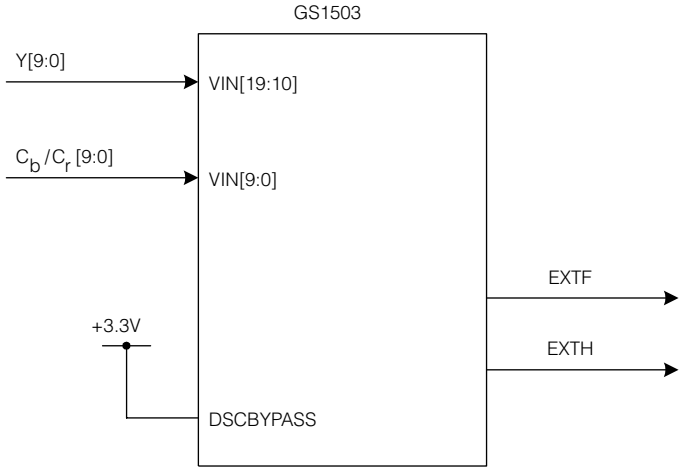


Fig. 9 Configuration for 10-bit Y and C_b/C_r Input Video with TRS and Line Numbers

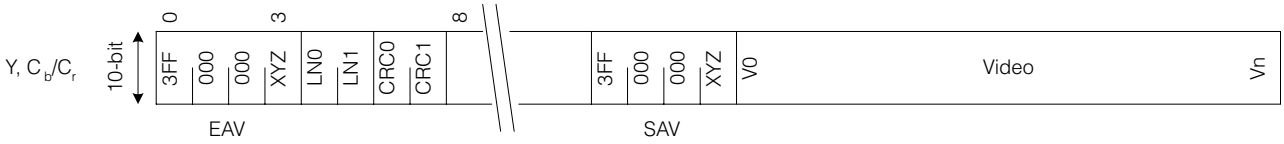


Fig. 10 Video Input Format 10-bit with TRS and Line Numbers

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	0	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	0	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	1	0

1.3.2 8-bit Y and C_b/C_r Input Video with TRS and Line Numbers

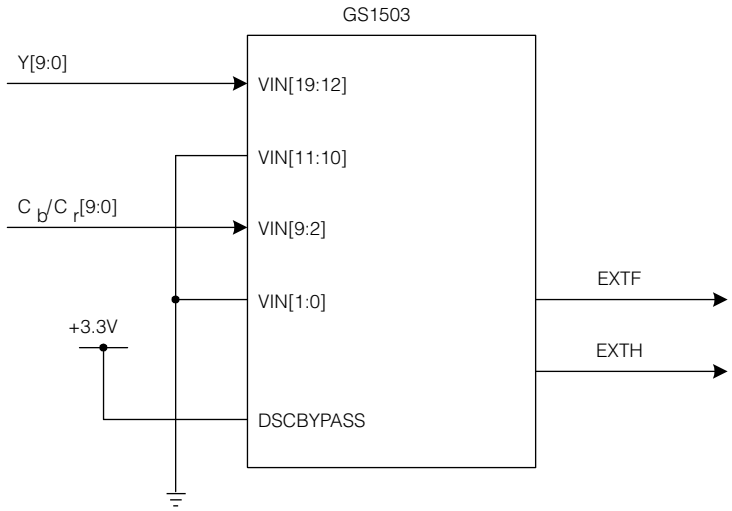


Fig. 11 Configuration for 8-bit Y and C_b/C_r Input Video with TRS and Line Numbers

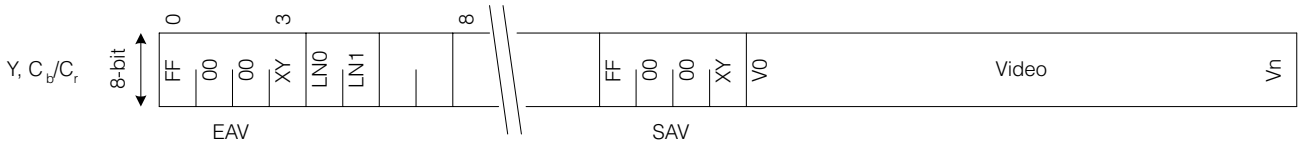


Fig. 12 Video Input Format 8-bit with TRS and Line Numbers

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	0	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	1	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	1	0

1.3.3 10-bit or 8-bit Y and C_b/C_r Input without TRS and Line Numbers

The GS1503 will insert TRS and Line Numbers based on EXTF and EXTH inputs. *See Figure 14 for timing.* In progressive format video standards, a high-to-low edge signal must be input at the EXTF external pin on every frame to indicate the position of line 1. *See Figure 15.*

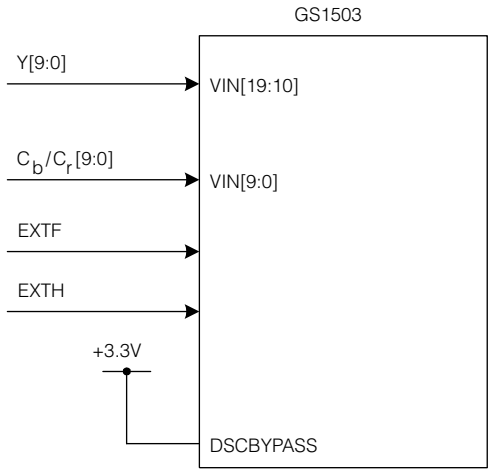


Fig. 13 Configuration for 10-bit or 8-bit Y and C_b/C_r Input Video without TRS and Line Numbers

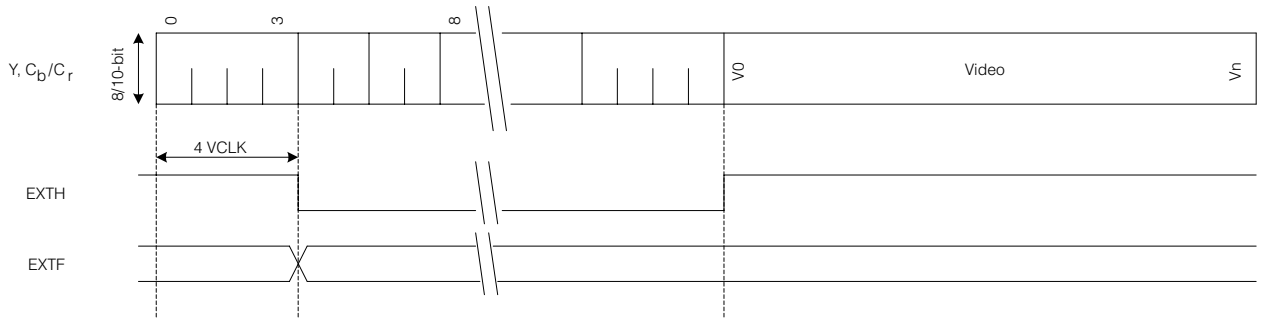


Fig. 14 Video Input Format (8/10-bit without TRS and Line Numbers)

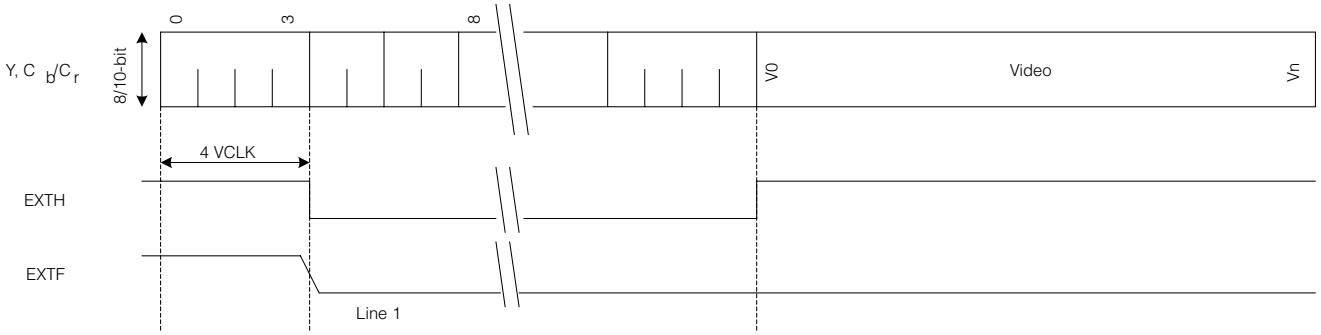


Fig. 15 Video Input Format (Progressive)

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	1	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	0 or 1	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	1	0

1.3.4 20-bit Scrambled Input

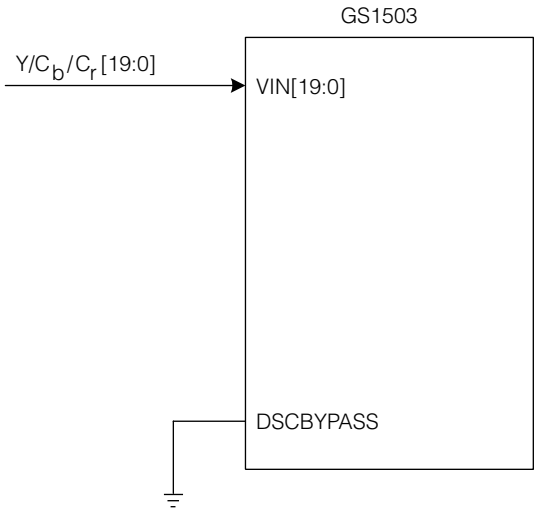


Fig. 16 Configuration for 20-bit Scrambled Input

Register Settings (Default Mode)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	0	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	0	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	0	0

1.4 VIDEO OUTPUT FORMAT

1.4.1 20-bit Scrambled Output

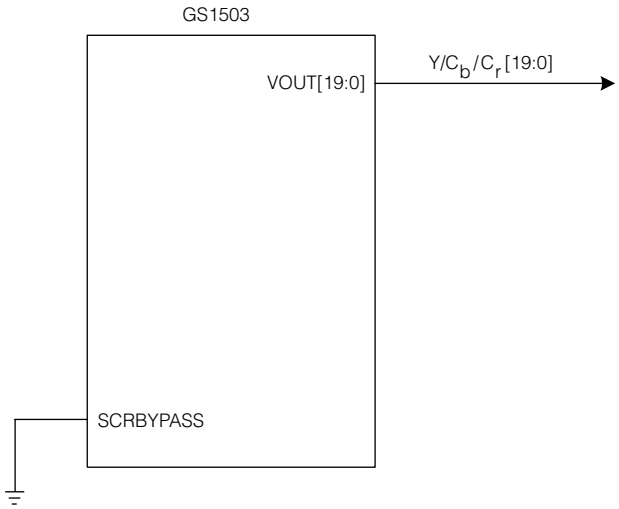


Fig. 17 Configuration for 20-bit Scrambled Output

Register Settings (Default Mode)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
SCRBYPASS	0: SMPTE 292M scrambling enabled 1: Bypass SMPTE 292M scrambling	001	2	0	0

1.4.2 10-bit Y and C_b/C_r Output

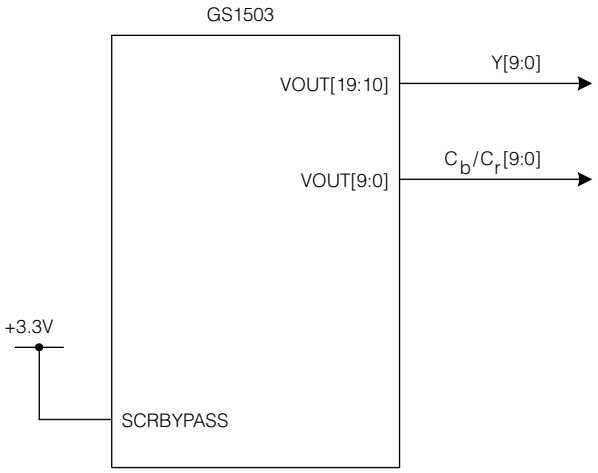


Fig. 18 Configuration for 10-bit Y and C_b/C_r Output

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
SCRBYPASS	0: SMPTE 292M scrambling enabled 1: Bypass SMPTE 292M scrambling	001	2	1	0

1.5 VIDEO DATA PROCESSING

1.5.1 Video Signal Input Detection

The GS1503 will set the VIDEO_DET external pin HIGH when three consecutive TRS are detected in the input video signal. Also, the VIDEO_DET bit of Host Interface register 000h is set HIGH.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VIDEO_DET	Video input signal detection (1: Detection)	000	6	-	0

1.5.2 Video Input CRC Error Detection

The GS1503 will set the CRC_ERR external pin HIGH when a CRC error is detected in the input video signal. Also, the CRC_ERR bit 5 of Host Interface register 000h is set HIGH. The number of CRC errors accumulated in one video frame can be read form CRC_CNT[11:0] in Host Interface registers 006h and 007h.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CRC_ERR	Video input signal CRC error detection (1: Detection)	000	5	-	0
CRC_CNT[11:0]	Video input signal CRC error accumulation in 1 video frame	006 007	3-0 7-0	-	0

1.5.3 Video Output CRC Insertion

When the CRC_INS bit 4 of Host Interface register 000h is set HIGH, the GS1503 will re-calculate the video line CRC words. The re-calculated CRC words are inserted in the video output signal. When CRC_INS is set LOW, the line CRC words are not updated and existing CRC words at the input of the device will be output unchanged.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CRC_INS	Video line CRC insertion (1: Insertion)	000	4	1	1

1.5.4 Illegal Code Re-mapping

When LIMIT_ON bit 4 of Host Interface register 008h is set HIGH, input video words between 000-003 are re-mapped to 004, and values between 3FC-3FF are re-mapped to 3FB. Valid only when the EXT_SEL bit 3 of Host Interface register 000h is set HIGH.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	1	0
LIMIT_ON	Illegal code re-mapping (1: Enabled)	008	4	1	0

1.5.5 Input Blanking

When VBLK_INS bit 3 of Host Interface register 008h is set HIGH, the input video vertical blanking will be set to 040h for the Luma channel and 200h for the Chroma channel.

When HBLK_INS bit 2 of Host Interface register 008h is set HIGH, the input video horizontal blanking will be set to 040h for the Luma channel and 200h for the Chroma channel. The TRS, line number and CRC words will also be set to blanking values.

The blanking function is performed at the output of the GS1503 video data stream. If the HBLK_INS bit is set HIGH, any multiplexed audio will be replaced with blanking codes.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VBLK_INS	Input vertical blanking (1: Enabled)	008	3	1	0
HBLK_INS	Input horizontal blanking (1: Enabled)		2	1	0

1.5.6 Line Number Insertion

When LN_INS bit 1 of Host Interface register 008h is set HIGH, the GS1503 will insert line numbers into the video data stream. When set LOW, existing line numbers will remain in the output video stream.

When EXT_SEL bit 3 of Host Interface register 001h is set HIGH, line numbers will be inserted based on the timing of EXTH and EXTF input signals.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
LN_INS	Line number insertion (1: Enabled)	008	1	1	1

1.5.7 TRS Word Insertion

When TRS_INS bit 0 of Host Interface register 008h is set HIGH, the GS1503 will insert TRS codes into the video data stream. When set LOW, existing TRS codes will remain in the output video stream.

When EXT_SEL bit 3 of Host Interface register 001h is set HIGH, TRS codes will be inserted based on the timing of EXTH and EXTF input signals.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
TRS_INS	TRS word insertion (1: Enabled)	008	0	1	1

1.6 AUDIO DATA PROCESSING

1.6.1 Digital Audio Input Format

The GS1503 will accept two audio input formats, AES/EBU digital audio input and serial input, as listed in Table 3. Serial input can be formatted in the following two modes. *See Figure 19:*

24-bit Left Justified; MSB first

24-bit Right Justified; MSB last

The audio input format is configured using the AM[1:0] external pins or via AM[1:0] bits 1-0 in Host Interface register 010h. To configure the audio input format via the Host Interface, AM_SEL bit 7 in Host Interface register 010h must be set HIGH. The GS1503 will default to the AM[1:0] external pin setting.

Table 3: Audio Input Formats

AM[1:0]	AUDIO INPUT FORMAT
0	Serial audio input: 24-bit Left Justified; MSB first
1	Serial audio input: 24-bit Right Justified; MSB last
2	AES/EBU audio input

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
AM_SEL	0: External pin setting 1: Register setting	010	7	1	0
AM[1:0]	Audio input format selection (AM[1] is MSB)		1-0	*See Table 3*	0

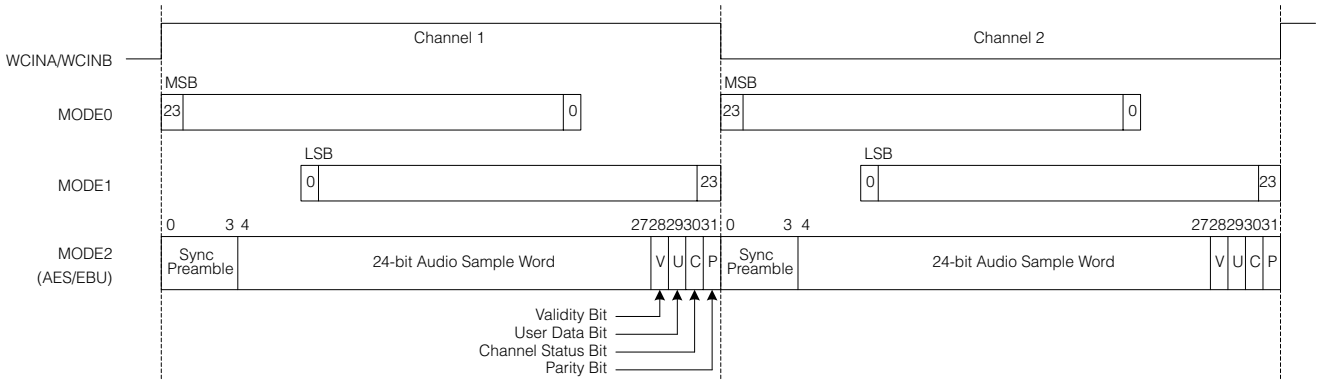


Fig. 19 Audio Input Formats

1.6.2 Digital Audio Input Timing

1.6.2.1 AES/EBU Format Input

A 6.144MHz (128fs) audio clock must be supplied to the ACLKA and ACLKB inputs. ACLKA is used to clock the AES/EBU digital audio signal for channels 1 to 4 (AIN1/2 and AIN3/4) into the device. ACLKB is used to clock the AES/EBU digital audio signal for channels 5 to 8 (AIN5/6 and AIN7/8) into the device. In AES/EBU input mode, the WCINB and WCINB external pins should be grounded. *See Figure 20 for timing.*

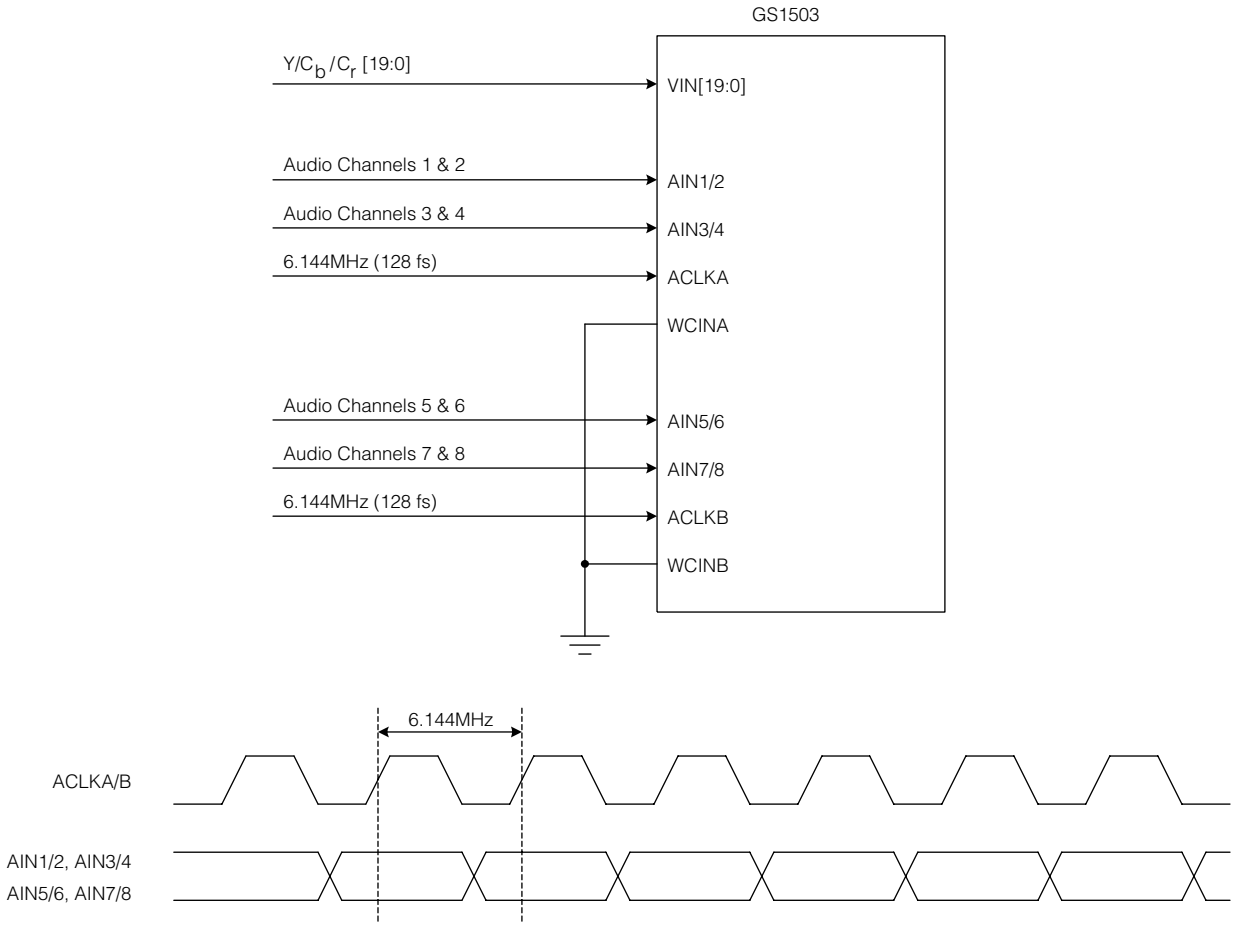


Fig. 20 AES/EBU Input Configuration and Timing

1.6.2.2 Serial Audio Input Modes

A 6.144MHz (128fs) audio clock must be supplied to the ACLKA and ACLKB inputs. An audio word clock at 48kHz (fs) must also be supplied to the WCINA and WCINB inputs, as shown in Figure 21. The AUDIO_CS[183:0] bits in Host Interface registers 058h to 06Eh can be used to enter the 22 8-bit bytes of the Audio Channel Status Block, as defined in AES3-1992. NOTE: The CRC byte is generated internally by the GS1503. The GS1503 will default to Professional audio mode with 24-bit word length and emphasis off. *See Table 9*.

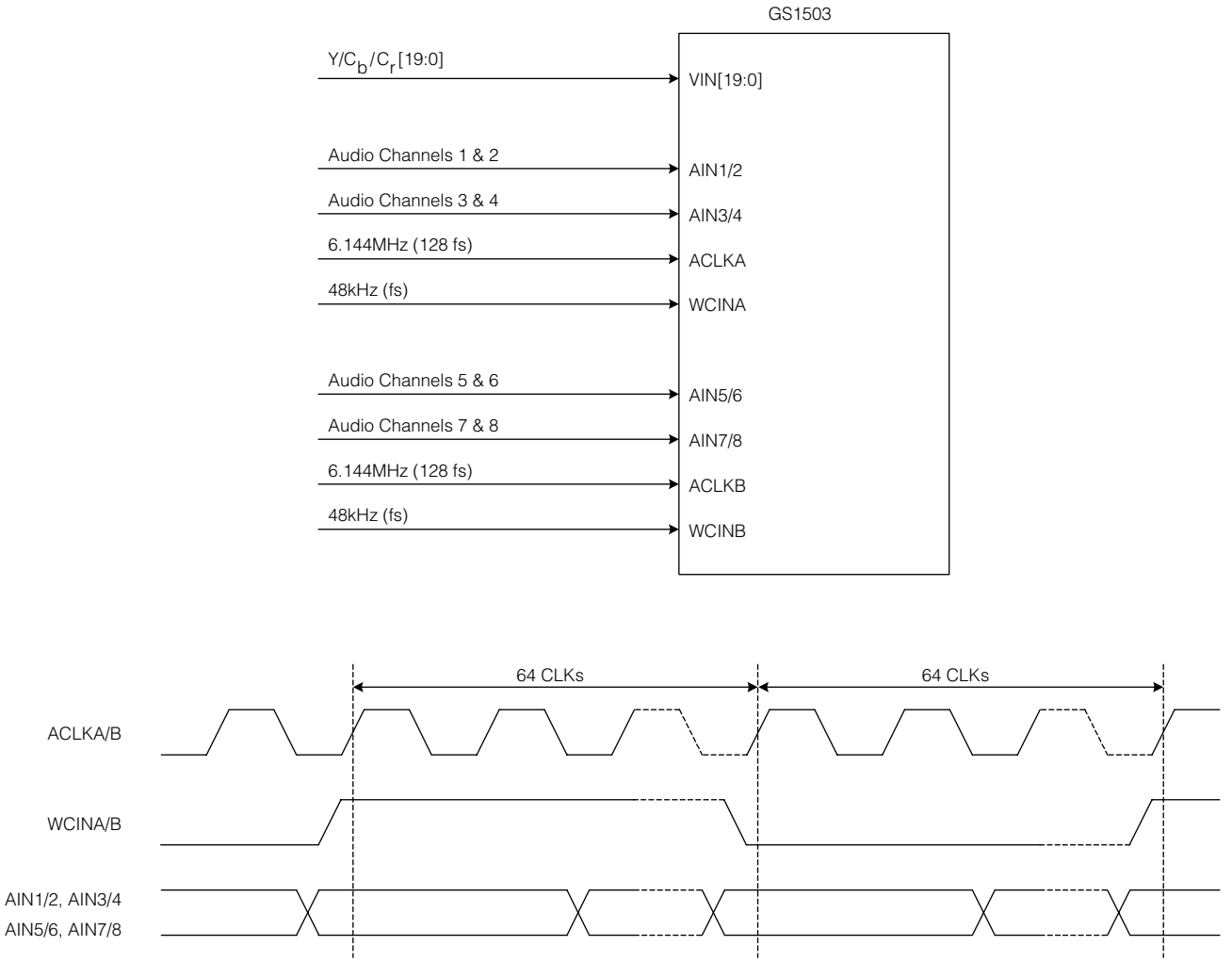


Fig. 21 Serial Audio Input Configuration and Timing

1.6.3 Audio Clock Phase Locked Loop

Figure 22 shows the configuration for deriving the 6.144MHz audio clock in AES/EBU audio input mode. The GS1503 will internally synchronize the AES/EBU audio input to the corresponding ACLK, using the clock extracted from the AES/EBU bi-phase mark encoding. This configuration is not required for serial audio input modes. *See the Reference Design Section 3 for circuit specifics.*

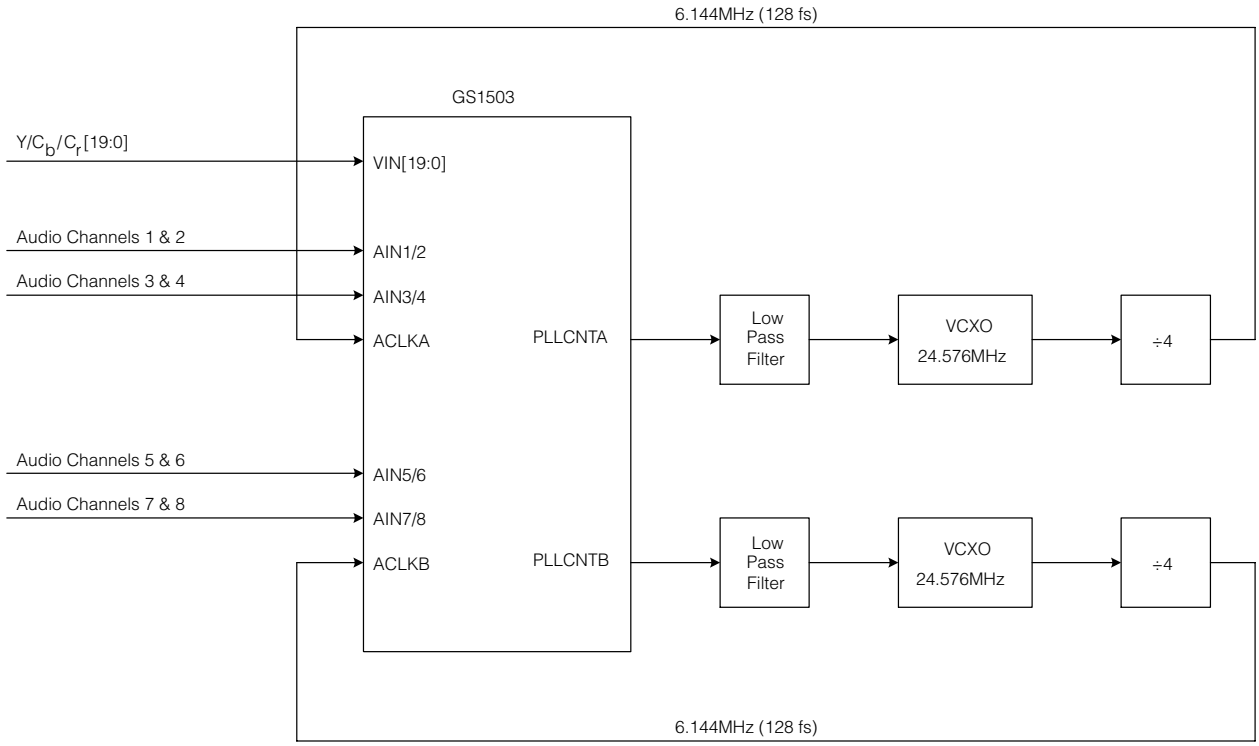


Fig. 22 Block Diagram of GS1503 Audio Clock PLL

1.6.4 Audio Signal Input Detection

The audio input signal detect registers will be set HIGH in AES/EBU audio mode when the preamble of the audio input data is detected 3 times consecutively. In serial audio input mode, the GS1503 will set the audio input signal detect registers HIGH when a 48kHz word clock is detected at the corresponding inputs. Audio channels 1 to 4 will be set when WCINA is validated, and audio channels 5 to 8 when WCINB is validated. Host Interface register 010h, bits 6-3, report the individual audio channels pairs detected.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
AUD7/8_DET	Ch7/8 Audio input signal detection (1:Detection)	010	6	-	0
AUD5/6_DET	Ch5/6 Audio input signal detection (1:Detection)		5	-	0
AUD3/4_DET	Ch3/4 Audio input signal detection (1:Detection)		4	-	0
AUD1/2_DET	Ch1/2 Audio input signal detection (1:Detection)		3	-	0

1.6.5 Audio Channel Status CRC Error Detection

In AES/EBU audio mode, the GS1503 will check the Channel Status CRC for errors. If any Channel Status CRC errors are detected in an AES/EBU audio input channel pair, the corresponding bit in Host Interface register 011h will be set HIGH. In serial audio input mode, the CRC error flags are always set LOW.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ACRC7/8_ERR	Ch7/8 Audio Channel Status CRC error detection (1: Detection)	011	7	-	0
ACRC5/6_ERR	Ch5/6 Audio Channel Status CRC error detection (1: Detection)		6	-	0
ACRC3/4_ERR	Ch3/4 Audio Channel Status CRC error detection (1: Detection)		5	-	0
ACRC1/2_ERR	Ch1/2 Audio Channel Status CRC error detection (1: Detection)		4	-	0

1.6.6 Audio Input Parity Error Detection

In AES/EBU audio mode, the GS1503 will check for Audio Parity errors. If any Audio Parity errors are detected in an AES/EBU audio input channel pair, the corresponding bit in Host Interface register 012h will be set HIGH. In serial audio input mode, the Audio Parity error flags are always set LOW.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
AP7/8_ERR	Ch7/8 Audio parity error detection (1: Detection)	012	3	-	0
AP5/6_ERR	Ch5/6 Audio parity error detection (1: Detection)		2	-	0
AP3/4_ERR	Ch3/4 Audio parity error detection (1: Detection)		1	-	0
AP1/2_ERR	Ch1/2 Audio parity error detection (1: Detection)		0	-	0

1.6.7 Audio Channel Status CRC Insert Function

When bits 3-0 of Host Interface register 011h are set HIGH, the GS1503 will re-calculate the Channel Status CRC word for the corresponding audio input channel pair. The re-calculated Channel Status CRC word is multiplexed into the audio data packet as per SMPTE 299M. When bits 3-0 of Host Interface register 011h are set LOW, the Channel Status CRC word is not updated and the existing Channel Status CRC word will be multiplexed. In serial audio input mode, these registers should be set LOW.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ACRC7/8_INS	Ch7/8 Audio Channel Status CRC insertion (1: Insertion)	011	3	1	0
ACRC5/6_INS	Ch5/6 Audio Channel Status CRC insertion (1: Insertion)		2	1	0
ACRC3/4_INS	Ch3/4 Audio Channel Status CRC insertion (1: Insertion)		1	1	0
ACRC1/2_INS	Ch1/2 Audio Channel Status CRC insertion (1: Insertion)		0	1	0

1.7 AUDIO DATA PACKETS

1.7.1 Audio Data Packet Structure

Figure 23 shows the structure of the audio data packets as defined in SMPTE 299M. The audio data packets are multiplexed into the Chroma channel of the video data stream. Table 4 lists the description of the individual audio data packet words. Note that the GS1503 will automatically generate certain audio data packet words.

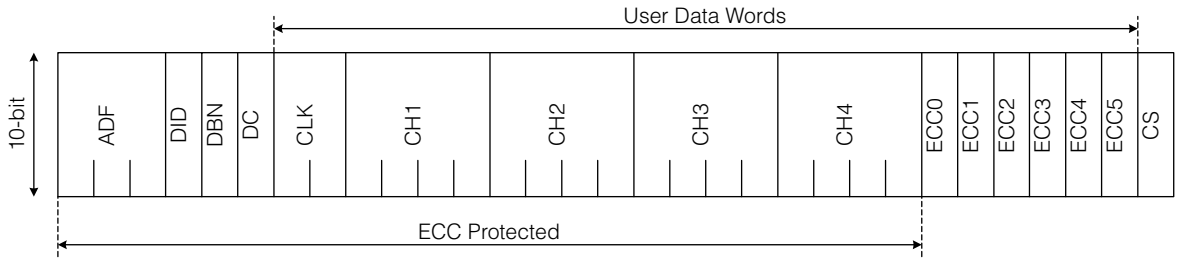


Fig. 23 Audio Data Packet Structure

Table 4: Audio Data Packet Word Descriptions

NAME	NO OF WORDS	DESCRIPTION	DATA	AUTO-GENERATION
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	2E7h 1E6h 1E5h 2E4h	*See Table 5 in Section 1-7-2*
DBN	1	Data Block Number	Repeat 1-255	Yes
DC	1	Data Count	218h	Yes
CLK	2	Audio Clock Phase Data	-	Yes
CH1	4	Channel 1 audio data	-	
CH2	4	Channel 2 audio data	-	
CH3	4	Channel 3 audio data	-	
CH4	4	Channel 4 audio data	-	
ECC0-5	6	Error correction code for lower 8 bits of first 24 words	-	Yes
CS	1	Checksum. Calculates the sum of lower 9 bits of 22 words from DID	-	Yes

1.7.2 Audio Data Packet DID Setting

The audio group DID for audio input channels 1 to 4 (AIN1/2 and AIN3/4) is set in DATAIDA[1:0] bits 1-0 of Host Interface register 014h. The audio group DID for audio input channels 5 to 8 (AIN5/6 and AIN7/8) is set in DATAIDB[1:0] bits 3-2 of Host Interface register 014h. Table 5 shows the 2-bit Host Interface setting for the corresponding audio group DID.

When CASCADE is set LOW (external pin or register), the GS1503 will default to audio groups 1 and 2, where AIN1/2 and AIN3/4 will be multiplexed with audio group 1 DID, and AIN5/6 and AIN7/8 with audio group 2 DID.

Table 5: Audio Data Packet Group DID Host Interface Setting

AUDIO GROUP	10-BIT DATA	HOST INTERFACE REGISTER SETTING (2-BIT)
1	2E7h	11b
2	1E6h	10b
3	1E5h	01b
4	2E4h	00b

Register Settings (CASCADE set LOW)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DATAIDA [1-0]	Ch1-4 Audio data packet DID setting	014	1-0	*See Table 5*	11b
DATAIDB [1-0]	Ch5-8 Audio data packet DID setting		3-2		10b

When CASCADE is set HIGH (external pin or register), the GS1503 will default to audio groups 3 and 4, where AIN1/2 and AIN3/4 will be multiplexed with audio group 3 DID, and AIN5/6 and AIN7/8 with audio group 4 DID.

Register Settings (CASCADE set HIGH)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DATAIDA [1-0]	Ch1-4 Audio data packet DID setting	014	1-0	*See Table 5*	01b
DATAIDB [1-0]	Ch5-8 Audio data packet DID setting		3-2		00b

1.7.3 Audio Channel Multiplex Enable

Multiplexing of individual audio channels is enabled using the CHACT[7:0] bits 7-0 of Host Interface register 013h. When set HIGH, the corresponding audio channel is multiplexed into the audio data packet in the Chroma video data stream. CHACT7 corresponds to audio input channel 8 and CHACT0 corresponds to audio input channel 1. When all bits are set LOW, no audio data packets will be multiplexed and the GS1503 will be in bypass mode.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CHACT7	Ch8 multiplex enable (1: Enabled)	013	7	-	1
CHACT6	Ch7 multiplex enable (1: Enabled)		6		1
CHACT5	Ch6 multiplex enable (1: Enabled)		5		1
CHACT4	Ch5 multiplex enable (1: Enabled)		4		1
CHACT3	Ch4 multiplex enable (1: Enabled)		3		1
CHACT2	Ch3 multiplex enable (1: Enabled)		2		1
CHACT1	Ch2 multiplex enable (1: Enabled)		1		1
CHACT0	Ch1 multiplex enable (1: Enabled)		0		1

1.8 VIDEO SWITCHING LINE SETTING

The video switching point for field 1 and field 2 can be configured via the GS1503 Host Interface. The SW_LNA[12:0] register is used to configure the video switching line for field 1, and SW_LNB[12:0] to set video switching line for field 2. In progressive format video standards, only the SW_LNA[12:0] register is used. The default settings are line 7 for field 1 and line 569 for field 2 as defined in SMPTE 299M.

The GS1503 will not multiplex any audio data packets in the line immediately after the video switching point. For example, with the default setting of line 7 field 1, there will be no audio data packets in line 8. The next packets will appear on line 9. Audio control packets will be multiplexed once per field, two lines after the video switching point (on line 9, using the previous example). Arbitrary data packets will not be multiplexed in the two lines following the video switching point .

NOTE: The SMPTE 299M standard defines the video switching point as lines 7 and 569. If the SW_LNA[12:0] and SW_LNB[12:0] registers are programmed with values other than lines 7 and 569, the output of the GS1503 is not guaranteed to be compatible with all HD audio demultiplex systems. With non-SMPTE 299M compliant switch line settings, the user should avoid inputting a video data stream to the GS1503, which already contains embedded audio data and control packets.

For reliable operation, non-SMPTE 299M compliant video data streams with embedded audio should not be used in conjunction with the GS1503 in Multiplex Mode.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
SW_LNA[12:0]	Video Field 1 switching point setting	004 005	4-0 7-0	-	7d
SW_LNB[12:0]	Video Field 2 switching point setting	002 003	4-0 7-0	-	569d

1.9 MULTIPLEX CASCADE MODE

Two GS1503 devices can be cascaded in series to allow up to 16 channels of audio to be multiplexed (only one device requires CASCADE to be set HIGH). Figure 24 shows the cascade architecture for a 16-channel system. To configure the GS1503 for cascade mode, the CASCADE external pin or CASCADE bit 7 of Host Interface register 014h is set HIGH. When set HIGH, the GS1503 will default to audio groups 3 and 4. When set LOW, the GS1503 will default to audio groups 1 and 2.

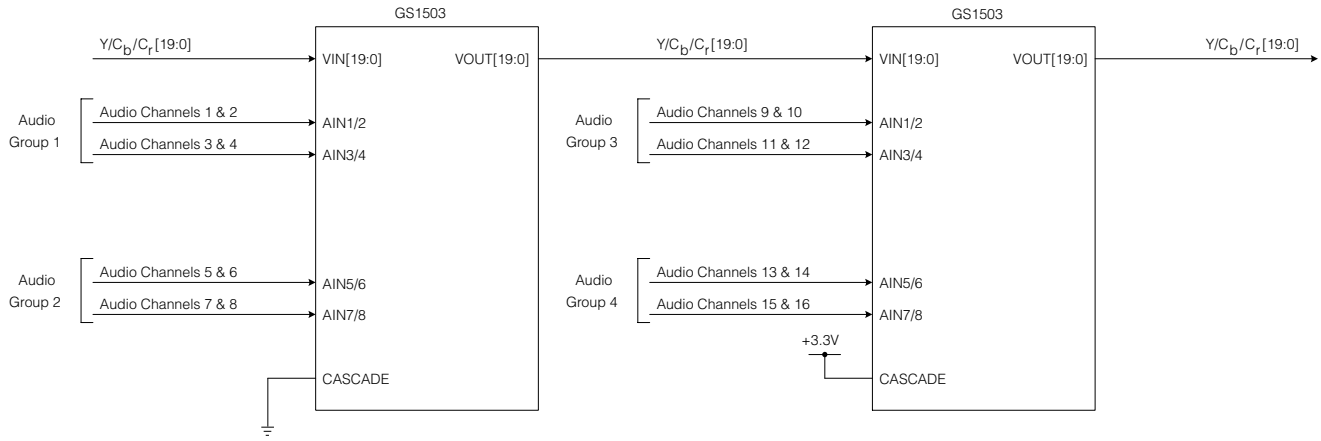


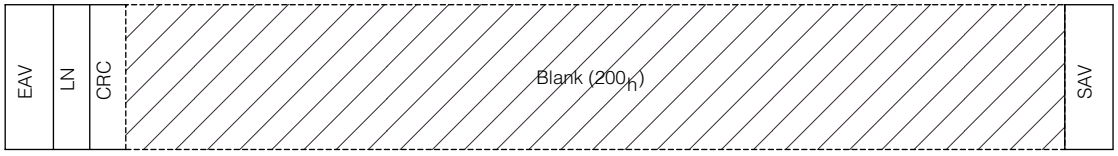
Fig. 24 Multiplexing 16 Channels of Audio using Cascade Architecture

Register Settings

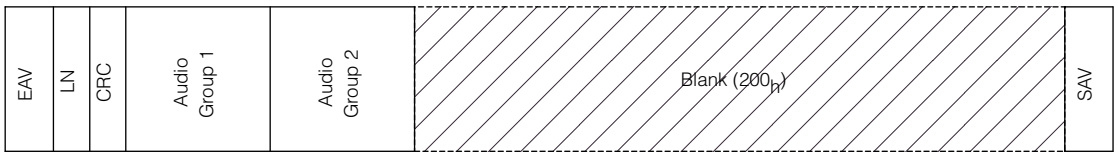
NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CASCADE	Cascade enable (1: Enabled)	014	7	1	0

When CASCADE is set LOW, the GS1503 will multiplex audio data and control packets as shown in Figure 25 (NOTE: Only the Chroma channel of the video data stream is shown). Any existing audio data or control packets will be deleted and replaced with blanking data before the new packets are multiplexed. New packets are multiplexed immediately after the two video line CRC words.

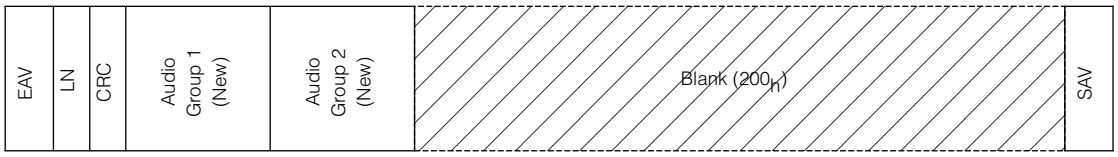
When CASCADE is set HIGH, the GS1503 will multiplex the audio data and control packets immediately after the existing packets, as shown in Figure 26. Avoid multiplexing new ancillary data packets with the same audio group DID as existing packets.



Video Signal before GS1503 (no existing Audio Data Packets)

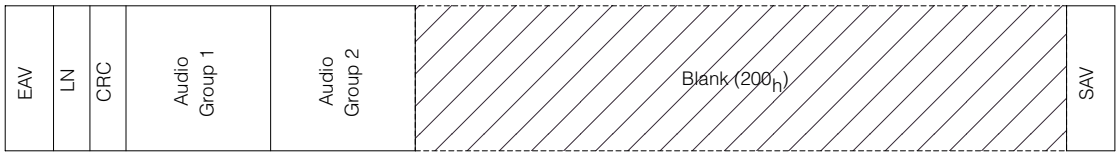


Video Signal before GS1503 (with existing Audio Data Packets)



Video Signal after GS1503 Insertion of Audio Groups 1 & 2 (CASCADE = 0)

Fig. 25



Video Signal before GS1503 (with existing Audio Data Packets)

Video Signal after GS1503 Insertion of Audio Groups 3 & 4 (CASCADE = 1)

Fig. 26

The GS1503 assumes that the ancillary data space from the first blanking location to the SAV contains no ancillary data packets. Existing ancillary data packets must be contiguous from the beginning of the HANC space or the GS1503 will overwrite existing packets with blanking before multiplexing new packets. *See Figure 27*.

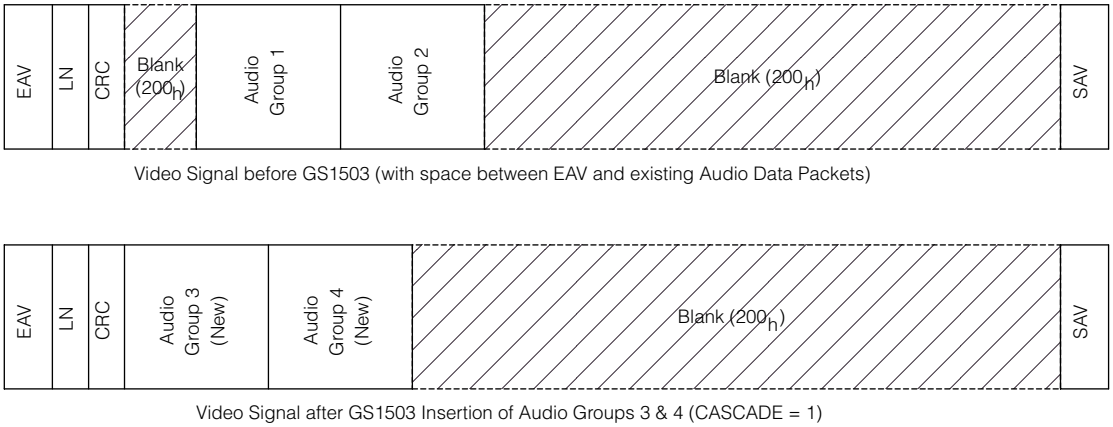


Fig. 27

1.10 AUDIO CONTROL PACKETS

1.10.1 Audio Control Packet Structure

Figure 28 shows the structure of the audio control packet as defined in SMPTE 299M. An audio control packet is multiplexed once per field in the Luma channel of the video data stream. Table 6 lists descriptions of the individual audio control packet words. The GS1503 will automatically generate certain audio control packet words.

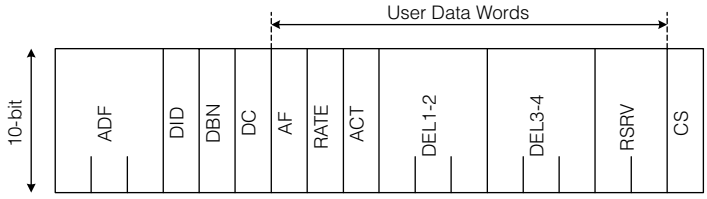


Fig. 28 Audio Control Packet Structure

Table 6: Audio Control Packet Word Descriptions

NAME	NO OF WORDS	DESCRIPTION	DATA	AUTO-GENERATION
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	1E3h 2E2h 2E1h 1E0h	*See Table 7 in Section 1-10-2*
DBN	1	Data Block Number	200h	Yes
DC	1	Data Count	10Bh	Yes
AF	1	Audio Frame Number	-	9-bit Host Interface Setting
RATE	1	Sampling Frequency	-	4-bit Host Interface Setting
ACT	1	Active Channel	-	CHACT[7:0] setting
DEL1-2	3	Ch1/2 Delay Data	-	27-bit Host Interface setting
DEL3-4	3	Ch3/4 Delay Data	-	27-bit Host Interface setting
RSRV	2	Reserved Words	200h	18-bit Host Interface setting
CS	1	Checksum. Calculates the sum of lower 9 bits of 15 words from DID	-	Yes

1.10.2 Audio Control Packet DID Setting

To multiplex audio control packets for audio channels 1 to 4 (inputs AIN1/2 and AIN3/4), the CTRONA bit 2 of Host Interface register 02Fh must be set HIGH. To multiplex audio control packets for audio channels 5 to 8 (inputs AIN5/6 and AIN7/8), the CTRONB bit 2 of Host Interface register 020h must be set HIGH.

The audio control packet group DID for audio input channels 1 to 4 is set in CTRIDA[1:0] bits 1-0 of Host Interface register 02Fh. The audio control packet group DID for audio input channels 5 to 8 is set in CTRIDB[1:0] bits 3-2 of Host Interface register 020h. Table 7 shows the 2-bit Host Interface setting for the corresponding audio control packet group DID.

When CASCADE is set LOW (external pin or register), the GS1503 will default to audio groups 1 and 2, where the audio control packet for AIN1/2 and AIN3/4 will be multiplexed with group 1 DID, and AIN5/6 and AIN7/8 with group 2 DID.

Control packet data can be programmed via the corresponding registers in the Host Interface.

Table 7: Audio Control Packet Group DID Host Interface Settings

AUDIO GROUP	10-BIT DATA	HOST INTERFACE REGISTER SETTING (2-BIT)
1	1E3h	11b
2	2E2h	10b
3	2E1h	01b
4	1E0h	00b

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CTRONA	Ch1-4 Audio control packet multiplex enable (1: Enabled)	02F	2	1	1
CTRIDA[1:0]	Ch1-4 Audio control packet DID set		1-0	*See Table 7*	11b
AF_NOA[8:0]	Ch1-4 Audio frame number	030 031	0 7-0		0
RATEA[2:0]	Ch1-4 Sampling frequency data	032	3-1	-	0
ASXA	Ch1-4 Synchronization (0:Synchronous; 1: Non-synchronous)		0	-	0
DEL1-2A[26:0]	Ch1/2 Delay data	033 034 035 036	1-0 7-0 7-0 7-0	-	0
DEL3-4A[26:0]	Ch3/4 Delay data	037 038 039 03A	1-0 7-0 7-0 7-0	-	0
RSRVA[17:0]	Ch1-4 Reserved words	03B 03C 03D	1-0 7-0 7-0	-	0
CTRONB	Ch5-8 Audio control packet multiplex enable (1: Enabled)	020	2	1	1
CTRIDB[1:0]	Ch5-8 Audio control packet DID set		1-0	*See Table 7*	10b
AF_NOB[8:0]	Ch5-8 Audio frame number	021 022	0 7-0	-	0
RATEB[2:0]	Ch5-8 Sampling frequency data	023	3-1	-	0
ASXB	Ch5-8 Synchronization (0:Synchronous; 1: Non-synchronous)		0	-	0
DEL1-2B[26:0]	Ch5/6 Delay data	024 025 026 027	1-0 7-0 7-0 7-0	-	0
DEL3-4B[26:0]	Ch7/8 Delay data	028 029 02A 02B	1-0 7-0 7-0 7-0	-	0
RSRVB[17:0]	Ch5-8 Reserved words	02C 02D 02E	1-0 7-0 7-0	-	0

1.11 ARBITRARY DATA PACKETS

The GS1503 can multiplex arbitrary data packets according to SMPTE 291M. Typically, this consists of linear time code (LTC), vertical interval time code (VITC) or other user data, which is multiplexed once per video field. The GS1503 has two modes in which arbitrary data can be multiplexed into the Luma channel of the video data stream. A maximum of 255 user data words can be multiplexed in one packet. Figure 29 shows the structure of the arbitrary data packet.

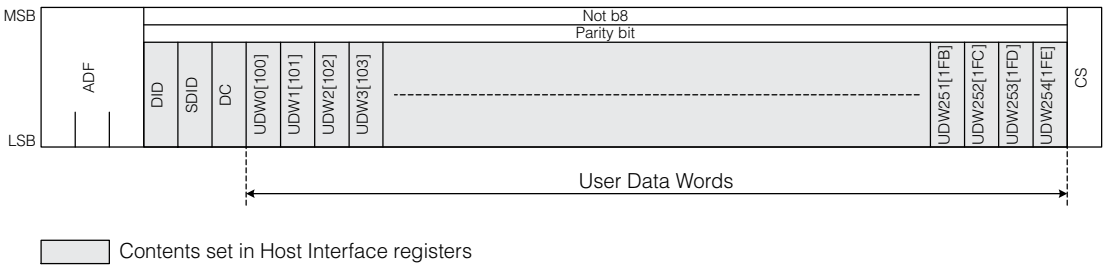


Fig. 29 Arbitrary Data Packet Structure

1.11.1 Arbitrary Data Multiplexing In External Pin Mode

This is the default mode for multiplexing arbitrary data packets. The GS1503 will set the PKTENO external pin HIGH when arbitrary data can be input to the device. Two VCLK cycles after PKTENO goes HIGH, the user should set the PKTEN arbitrary packet enable pin HIGH. Two VCLK cycles after PKTEN is set HIGH, arbitrary data can be input at the PKT[7:0] bus. See Figure 30 for timing.

The user is required to enter the following arbitrary data: Data ID (DID), Secondary Data ID (SDID), Data Count (DC) and User Data Words (UDW: maximum of 255), via the PKT[7-0] pins. This GS1503 automatically generates the Ancillary Data Flag (ADF), Checksum (CS) and bit 8 (Parity Bit) and bit 9 (Not bit 8).

The PKTENO pin will be set HIGH on all video lines except the two lines following the video switching point. For example, with the default setting of line 7 field 1, PKTENO will not be set HIGH on lines 8 and 9. The switching point is set in the SW_LNA[12:0] and SW_LNB[12:0] Host Interface registers for field 1 and field 2 respectively. *See Section 1-8.*

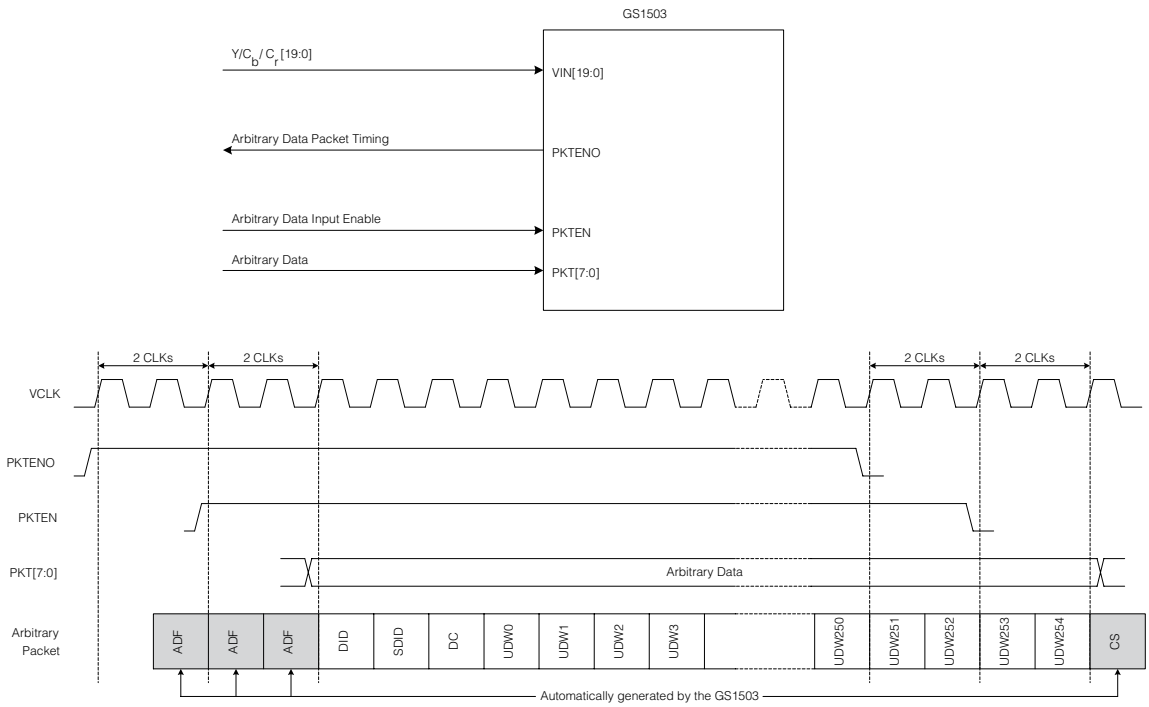


Fig. 30 Arbitrary Data Packet Input Timing Diagram

1.11.2 Arbitrary Data Multiplexing in Host Interface Mode

To select this mode, set ARBITMODE bit 0 in Host Interface register 050h HIGH. In this mode, the DID, SDID, DC and User Data Words must be programmed via the corresponding Host Interface registers. Set the video line number for field 1 and field 2 in which the arbitrary data packets are to be multiplexed using the ARBITLINEA[12:0] and ARBITLINEB[12:0] Host Interface registers respectively. The arbitrary data packet is multiplexed when ARBITON bit 1 in Host Interface register 050h is set HIGH. ARBITON should be set LOW during the programming of the arbitrary data packet in the Host Interface.

ARBITLINEA[12:0] and ARBITLINEB[12:0] should not be set to the two line numbers following the line number set in the SW_LNA[12:0] and SW_LNB[12:0] Host Interface registers. For example, with the default setting of line 7 field 1, ARBITLINEA[12:0] should not be set to line 8 or 9.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ARBITON	Arbitrary packet multiplex enable (1: Enabled) Valid only when ARBITMODE is HIGH	050	1	1	0
ARBITMODE	Arbitrary packet mode selection (0: External pin mode; 1: Host mode)		0	1	0
ARBITDID[7-0]	Arbitrary packet DID setting	051	7-0	-	0
ARBITSDID[7-0]	Arbitrary packet SDID setting	052	7-0	-	0
ARBITDC[7-0]	Arbitrary packet DC setting	053	7-0	-	0
ARBITLINEA[12:0]	Field 1 multiplexing line	054 055	3-0 7-0	-	0
ARBITLINEB[12:0]	Field 2 multiplexing line	056 057	3-0 7-0	-	0
ARBITUDW	Arbitrary packet UDW setting	100-1FE	7-0	-	0

Table 8: Multiplex Mode Host Interface Registers

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Video	VM_SEL	Video input format (external pin/internal register) configuration select. When set LOW, the video input format is configured via the VM[3:0] pins. When set HIGH, the video input format is configured via the "VM[3:0]" bits.	000	7	R/W	0
	VIDEO_DET	Video signal detection flag. Set HIGH when 3 consecutive TRS are detected in the input video signal.		6	R	0
	CRC_ERR	Video input signal CRC error detection. Set HIGH when a CRC error is detected in the input video signal. This register is refreshed on every video frame.		5	R	0
	CRC_INS	Video CRC insertion. When set HIGH, the Luma and Chroma line CRC words are re-calculated and inserted into the output video signal.		4	R/W	1
	VM[3:0]	Video input format selection. See Table 2. Valid when "VM_SEL" is HIGH.		3-0	R/W	0
	EXT_SEL	External EXTH/EXTF input select. When set LOW, the EXTH and EXTF pins are configured as outputs. When set HIGH, the GS1503 will insert TRS and Line Numbers based on signals input at the EXTH and EXTF pins.	001	3	R/W	0
	SCRBYPASS	Scramble processing bypass select. When set HIGH, the internal scrambler and NRZ(I) encoder is bypassed. NOTE: The status of the SCRBYPASS external pin is not updated in this register. The value programmed in this register is logical OR'd with the SCRBYPASS external pin setting.		2	R/W	0
	8BIT_SEL	8-bit input selection. When set HIGH, the GS1503 will accept an 8-bit input video signal.		1	R/W	0
	DSCBYPASS	Descramble process bypass select. When set HIGH, the internal SMPTE 292M descrambler is bypassed. NOTE: The status of the DSCBYPASS external pin is not updated in this register. The value programmed in this register is logical OR'd with the DSCBYPASS external pin setting.		0	R/W	0
	SW_LNB[12:0]	Video Field 2 switching line setting. Designates the video switching point for field 2. The default line number is 569, as defined by SMPTE 299M.	002 003	4-0 7-0	R/W	569d
	SW_LNA[12:0]	Video Field 1 switching line setting. Designates the video switching point for field 1. The default line number is 7, as defined by SMPTE 299M.	004 005	4-0 7-0	R/W	7d
	CRC_CNT[11:0]	CRC error accumulation. Reports the accumulated number of CRC errors in one video frame.	006 007	3-0 7-0	R	0
	RSV	Not used.	008	7-5	-	0
	LIMIT_ON	Illegal code re-mapping select. When set HIGH, input video words between 000-003 are re-mapped to 004, and values between 3FC-3FF are re-mapped to 3FB. Valid only when "EXT_SEL" is set HIGH.		4	R/W	0
	VBLK_INS	Vertical blanking enable. When set HIGH, the output video vertical blanking will be set to 040h for the Luma channel and 200h for the Chroma channel.		3	R/W	0

Table 8: Multiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	HBLK_INS	Horizontal blanking enable. When set HIGH, the output video horizontal blanking, including TRS, line numbers and line CRC words, will be set to 040h for the Luma channel and 200h for the Chroma channel. NOTE: If blanking of line numbers and TRS words is required, LN_INS and TRS_INS must be set LOW.		2	R/W	0
	LN_INS	Line insertion enable. When set HIGH, the GS1503 will insert line numbers into the video data stream. When set LOW, existing line numbers will remain in the output video stream.		1	R/W	1
	TRS_INS	TRS insertion enable. When set HIGH, the GS1503 will insert TRS codes into the video data stream. When set LOW, existing TRS codes will remain in the output video stream.		0	R/W	1
Audio	AM_SEL	Audio input format (external pin/register) configuration select. When set LOW, the audio input format is configured via the AM[1:0] pins. When set HIGH, the audio input format is configured via the "AM[1:0]" bits.	010	7	R/W	0
	AUD7/8_DET	Ch7/8 audio input signal detection. When set HIGH, an audio signal has been detected at the AIN7/8 input pin.		6	R	0
	AUD5/6_DET	Ch5/6 audio input signal detection. When set HIGH, an audio signal has been detected at the AIN5/6 input pin.		5	R	0
	AUD3/4_DET	Ch3/4 audio input signal detection. When set HIGH, an audio signal has been detected at the AIN3/4 input pin.		4	R	0
	AUD1/2_DET	Ch1/2 audio input signal detection. When set HIGH, an audio signal has been detected at the AIN1/2 input pin.		3	R	0
	RSV	Not used.		2	-	0
	AM[1:0]	Audio input format select. *See Table 3.* Valid when "AM_SEL" is HIGH.		1-0	R/W	0

Table 8: Multiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	ACRC7/8_INS	Ch7/8 audio Channel Status CRC insertion. When set HIGH, the Ch7/8 audio input Channel Status CRC is re-calculated before being multiplexed into the Audio Data Packet. Valid only when AES/EBU audio input format is selected.	011	7	R/W	0
	ACRC5/6_INS	Ch5/6 audio Channel Status CRC addition. When set HIGH, the Ch5/6 audio input Channel Status CRC is re-calculated before being multiplexed into the Audio Data Packet. Valid only when AES/EBU audio input format is selected.		6	R/W	0
	ACRC3/4_INS	Ch3/4 audio Channel Status CRC addition. When set HIGH, the Ch3/4 audio input Channel Status CRC is re-calculated before being multiplexed into the Audio Data Packet. Valid only when AES/EBU audio input format is selected.		5	R/W	0
	ACRC1/2_INS	Ch1/2 audio Channel Status CRC addition. When set HIGH, the Ch1/2 audio input Channel Status CRC is re-calculated before being multiplexed into the Audio Data Packet. Valid only when AES/EBU audio input format is selected.		4	R/W	0
	ACS7/8_ERR	Ch7/8 audio Channel Status error detection. When set HIGH, a Channel Status CRC error has been detected in the Ch7/8 audio input. Valid only when AES/EBU audio input format is selected.		3	R	0
	ACS5/6_ERR	Ch5/6 audio Channel Status error detection. When set HIGH, a Channel Status CRC error has been detected in the Ch5/6 audio input. Valid only when AES/EBU audio input format is selected.		2	R	0
	ACS3/4_ERR	Ch3/4 audio Channel Status error detection. When set HIGH, a Channel Status CRC error has been detected in the Ch3/4 audio input. Valid only when AES/EBU audio input format is selected.		1	R	0
	ACS1/2_ERR	Ch1/2 audio Channel Status error detection. When set HIGH, a Channel Status CRC error has been detected in the Ch1/2 audio input. Valid only when AES/EBU audio input format is selected.		0	R	0
	AP7/8_ERR	Ch7/8 audio parity error detection. When set HIGH, an audio parity error has been detected in the Ch7/8 audio input. Valid only when AES/EBU audio input format is selected.	012	3	R	0
	AP5/6_ERR	Ch5/6 audio parity error detection. When set HIGH, an audio parity error has been detected in the Ch5/6 audio input. Valid only when AES/EBU audio input format is selected.		2	R	0
	AP3/4_ERR	Ch3/4 audio parity error detection. When set HIGH, an audio parity error has been detected in the Ch3/4 audio input. Valid only when AES/EBU audio input format is selected.		1	R	0
	AP1/2_ERR	Ch1/2 audio parity error detection. When set HIGH, an audio parity error has been detected in the Ch1/2 audio input. Valid only when AES/EBU audio input format is selected.		0	R	0
Audio Channel Status Block	AUDIO_CS[7:0] : AUDIO_CS [183:176]	Audio Channel Status set. Valid in Serial Audio Input modes. Used to enter the 22 8-bit bytes of the Audio Channel Status Block, as defined in AES3-1992. NOTE: The CRC byte is generated internally by the GS1503.	058 : 06E	7-0 : 7-0	R/W	*See Table 9*

Table 8: Multiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Audio Data Packet	CHACT[7-0]	Audio channel multiplex enable. When set HIGH, the corresponding audio channel is multiplexed into the Chroma video data stream. "CHACT[7]" corresponds to audio input channel 8 and "CHACT[0]" corresponds to audio input channel 1. When all bits are set LOW, no audio data packets will be multiplexed and the GS1503 will be in bypass mode.	013	7-0	R/W	FFh
	CASCADE	Cascade select. When set HIGH, the GS1503 will default to audio groups 3 and 4. When set LOW, the GS1503 will default to audio groups 1 and 2. NOTE: The status of the CASCADE external pin is not updated in this register. The value programmed in this register is logical OR'd with the CASCADE external pin setting.	014	7	R/W	0
	CAS_ERR	Cascade connection error detection. When set HIGH, existing audio data packets have been detected with the same audio group DID as set in "DATAIDA[1:0]" and "DATAIDB[1:0]" registers. Valid only when CASCADE (external pin or register) is set HIGH		6	R	0
	AMUTEB	Ch5-8 audio mute enable. When set HIGH, the multiplexed audio packets for audio channels 5 to 8 are forced to zero. NOTE: The status of the MUTE external pin is not updated in this register. The value programmed in this register is logical OR'd with the MUTE external pin setting.		5	R/W	0
	AMUTEA	Ch1-4 audio mute enable. When set HIGH, the multiplexed audio packets for audio channels 1 to 4 are forced to zero. NOTE: The status of the MUTE external pin is not updated in this register. The value programmed in this register is logical OR'd with the MUTE external pin setting.		4	R/W	0
	DATAIDB[1:0]	Ch5-8 audio group DID setting. Designates the audio group DID for audio channels 5 to 8. *See Table 5.* When CASCADE (external pin or register) is set HIGH, the default setting is audio group 2. When CASCADE is set HIGH, the default setting is audio group 4.		3-2	R/W	10b
	DATAIDA[1:0]	Ch1-4 audio group DID setting. Designates the audio group DID for audio channels 1 to 4. *See Table 5.* When CASCADE (external pin or register) is set HIGH, the default setting is audio group 1. When CASCADE is set HIGH, the default setting is audio group 3.		1-0	R/W	11b
Audio Control Packet	RSV	Not used.	020	7-3	-	0
	CTRONB	Ch5-8 audio control packet multiplex enable. When set HIGH, the audio control packets for audio channels 5 to 8 will be multiplexed into the Luma channel of the video data stream.		2	R/W	1
	CTRIDB[1:0]	Ch5-8 audio control packet DID setting. Designates the audio control packet DID for audio channels 5 to 8. *See Table 7.* The default setting is audio group 2.		1-0	R/W	10b

Table 8: Multiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	AF_NOB[8:0]	Ch5-8 audio frame number. Designates the audio frame number for audio channels 5 to 8. Will be multiplexed into the audio control packet as per SMPTE 299M.	021 022	0 7-0	R/W	0
	RATEB[2:0]	Ch5-8 sampling frequency set. Designates the audio sampling frequency for audio channels 5 to 8. Will be multiplexed into the RATE word of the audio control packet as per SMPTE 299M. The default setting is 48kHz.	023	3-1	R/W	0
	ASXB	Ch5-8 synchronization set. When set HIGH, the "asx" bit of the audio control packet RATE word designates audio channels 5 to 8 as asynchronous, as per SMPTE 299M. When set LOW, the "asx" bit of the audio control packet RATE word designates synchronous audio (default setting).		0	R/W	0
	DEL1-2B[26:0]	Ch5/6 delay data. Designates the accumulated audio processing delay relative to video for audio channels 5 and 6. Will be multiplexed into the audio control packet as per SMPTE 299M.	024 025 026 027	1-0 7-0 7-0 7-0	R/W	0
	DEL3-4B[26:0]	Ch7/8 delay data. Designates the accumulated audio processing delay relative to video for audio channels 7 and 8. Will be multiplexed into the audio control packet as per SMPTE 299M.	028 029 02A 02B	1-0 7-0 7-0 7-0	R/W	0
	RSRVB[17:0]	Ch5-8 reserve words. Designates the value set in the RSRV words of the audio control packet for audio channels 5 to 8, as per SMPTE 299M. NOTE: As these words are reserved for future use, they should be set to zero.	02C 02D 02E	1-0 7-0 7-0	R/W	0
	RSV	Not used.	02F	7-3	-	0
	CTRONA	Ch1-4 audio control packet multiplex enable. When set HIGH, the audio control packets for audio channels 1 to 4 will be multiplexed into the Luma channel of the video data stream.		2	R/W	1
	CTRIDA[1:0]	Ch1-4 audio control packet DID setting. Designates the audio control packet DID for audio channels 1 to 4. *See Table 7.* The default setting is audio group 1.		1-0	R/W	11b
	AF_NOA[8:0]	Ch1-4 audio frame number. Designates the audio frame number for audio channels 5 to 8. Will be multiplexed into the audio control packet as per SMPTE 299M.	030 031	0 7-0	R/W	0
	RATEA[2:0]	Ch1-4 sampling frequency set. Designates the audio sampling frequency for audio channels 1 to 4. Will be multiplexed into the RATE word of the audio control packet as per SMPTE 299M. The default setting is 48kHz.	032	3-1	R/W	0
	ASXA	Ch1-4 synchronization set. When set HIGH, the "asx" bit of the audio control packet RATE word designates audio channels 1 to 4 as asynchronous, as per SMPTE 299M. When set LOW, the "asx" bit of the audio control packet RATE word designates synchronous audio (default setting).		0	R/W	0

Table 8: Multiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	DEL1-2A[26:0]	Ch1/2 delay data. Designates the accumulated audio processing delay relative to video for audio channels 1 and 2. Will be multiplexed into the audio control packet as per SMPTE 299M.	033 034 035 036	1-0 7-0 7-0 7-0	R/W	0
	DEL3-4A[26:0]	Ch3/4 delay data. Designates the accumulated audio processing delay relative to video for audio channels 3 and 4. Will be multiplexed into the audio control packet as per SMPTE 299M.	037 038 039 03A	1-0 7-0 7-0 7-0	R/W	0
	RSRVA[17:0]	Ch1-4 reserve words. Designates the value set in the RSRV words of the audio control packet for audio channels 1 to 4, as per SMPTE 299M. NOTE: As these words are reserved for future use, they should be set to zero.	03B 03C 03D	1-0 7-0 7-0	R/W	0
Arbitrary Data Packet	ARBITON	Arbitrary data packet multiplex. Valid only when "ARBITMODE" is HIGH. When set HIGH, arbitrary data packets will be multiplexed into the Luma video data stream using the Host Interface register settings.	050	1	R/W	0
	ARBITMODE	Arbitrary packet mode select. When set HIGH, arbitrary data packets are multiplexed using the Host Interface register settings. When set LOW, arbitrary data packets are multiplexed using the external pin inputs.		0	R/W	0
	ARBITDID[7:0]	Arbitrary packet Data ID setting. Designates the 8 LSBs of the arbitrary data packet DID word. The 2 MSBs are internally generated. "ARBITDID[7]" is the MSB and "ARBITDID[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	051	7-0	R/W	0
	ARBITSDID[7:0]	Arbitrary packet Secondary Data ID setting. Designates the 8 LSBs of the arbitrary data packet secondary DID word. The 2 MSBs are internally generated. "ARBITSDID[7]" is the MSB and "ARBITSDID[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	052	7-0	R/W	0
	ARBITDC[7:0]	Arbitrary packet DC setting. Designates the 8 LSBs of the arbitrary data packet Data Count word. The 2 MSBs are internally generated. "ARBITDC[7]" is the MSB and "ARBITDC[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	053	7-0	R/W	0
	ARBITLINEB[12:0]	Field 2 arbitrary packet multiplex line number setting. Designates the field 2 video line in which the arbitrary data packets will be multiplexed. Valid only when "ARBITMODE" is HIGH.	054 055	3-0 7-0	R/W	0
	ARBITLINEA[12:0]	Field 1 arbitrary packet multiplex line number setting. Designates the field 1 video line in which the arbitrary data packets will be multiplexed. Valid only when "ARBITMODE" is HIGH.	056 057	3-0 7-0	R/W	0
	ARBITUDW0 : ARBITUDW254	Arbitrary packet User Data Word set. Designates the 8 LSBs for each of the 255 arbitrary packet User Data Words. The 2 MSBs are internally generated. Valid only when "ARBITMODE" is HIGH.	100 : 1FE	7-0 : 7-0	R/W	0

Table 9: Audio Channel Status Default Values

ADDRESS	VALUE	CHANNEL STATUS
058	85	Professional; Valid Audio; No Emphasis (manual override disabled); 48kHz Sampling Frequency (manual override disabled).
059	08	Two-Channel Mode (manual override disabled).
05A	2C	Maximum Audio Sample Word Length is 24bits; Encoded Audio Word Length is 24-bit.
Others	00	-

2. DEMULTIPLEX MODE

2.1 FUNCTIONAL OVERVIEW

The GS1503 HD Embedded Audio CODEC fully supports the demultiplexing of Audio Data Packets, Audio Control Packets and Arbitrary Data Packets as per SMPTE 291M and 299M. The device can be configured to operate with all video standards defined in SMPTE 292M, levels A through M. The GS1503 also supports the 1080/24PsF, 25PsF and 30PsF video formats as described in SMPTE RP211.

The video input format can be one of the following configurations:

10-bit Y and C_b/C_r input with TRS and Line Numbers

20-bit scrambled input

The video output format can be one of the following configurations:

20-bit scrambled output

10-bit Y and C_b/C_r output

Up to a maximum of 8 channels of 48kHz digital audio can be demultiplexed per device. The audio output format can be selected as either AES/EBU, or one of two serial audio data output modes. A maximum of 16 channels of audio can be demultiplexed by serially cascading two devices.

Audio control packets, as defined in SMPTE 299M, can also be demultiplexed to obtain information about the nature of the embedded audio data. The contents of the audio control packet are stored in registers of the Host Interface.

The GS1503 will also demultiplex arbitrary data packets as defined in SMPTE 291M. The arbitrary data packets can serve as an auxiliary data signal for proprietary applications. The GS1503 can be configured to demultiplex arbitrary data packets and output them at dedicated external pins or via the Host Interface registers. Up to a maximum of 255 8-bit words can be demultiplexed (excluding Ancillary Data Flags and Checksum).

To use the GS1503 in Demultiplex Mode, set the $\overline{\text{MUX}}$/DEMUX external pin HIGH.

2.2 VIDEO STANDARD

The video standard is selected from the VM[3:0] external pins or VM[3:0] bits 3-0 in Host Interface register 000h. To configure the video standard via the Host Interface, VM_SEL bit 7 in Host Interface register 000h must be set HIGH. The GS1503 will default to the VM[3:0] external pin setting. The supported video standards are listed in Table 10.

.

Table 10: Supported Video Standards

VM [3:0]	INPUT FORMAT	REFERENCE SMPTE DOCUMENT	SMPTE 292M LEVEL
1110b	1035i (30 & 30/1.001 Hz)	260M	A, B
1100b	1080i (25 Hz)	295M	C
1000b	1080i/1080sF (30 & 30/1.001 Hz)	274M, RP211	D, E
1010b	1080i/1080sF (25 Hz)	274M, RP211	F
1111b	1080sF (24 & 24/1.001 Hz)	RP211	
0010b	1080p (30 & 30/1.001 Hz)	274M	G, H
0100b	1080p (25 Hz)	274M	I
0110b	1080p (24 & 24/1.001 Hz)	274M	J, K
0000b	720p (60 & 60/1.001 Hz)	296M	L, M
0001b	720p (30 & 30/1.001 Hz)	296M	
0011b	720p (50 Hz)	296M	
0101b	720p (25 Hz)	296M	
0111b	720p (24 & 24/1.001 Hz)	296M	
All other settings are reserved			

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VM_SEL	0: External pin select 1: Register select	000	7	1	0
VM[3:0]	Video formal selection (VM[3] is MSB)		3-0	*See Table 10*	0

2.3 VIDEO INPUT FORMAT

2.3.1 20-bit Scrambled Input

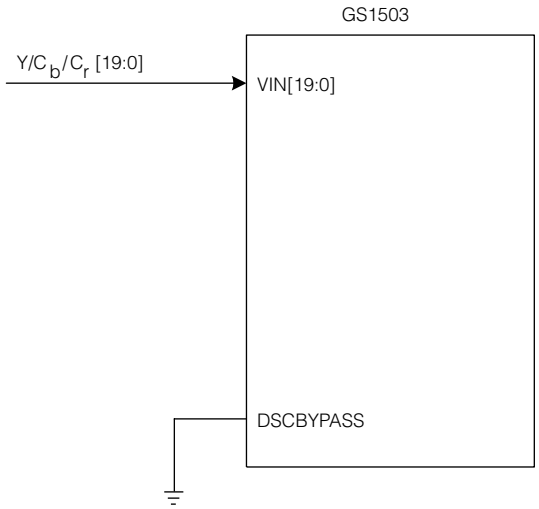


Fig. 31 20-bit Scrambled Input Configuration

Register Settings (Default Mode)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	0	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	0	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	0	0

2.3.2 10-bit Y and C_b/C_r Input with TRS and Line Numbers

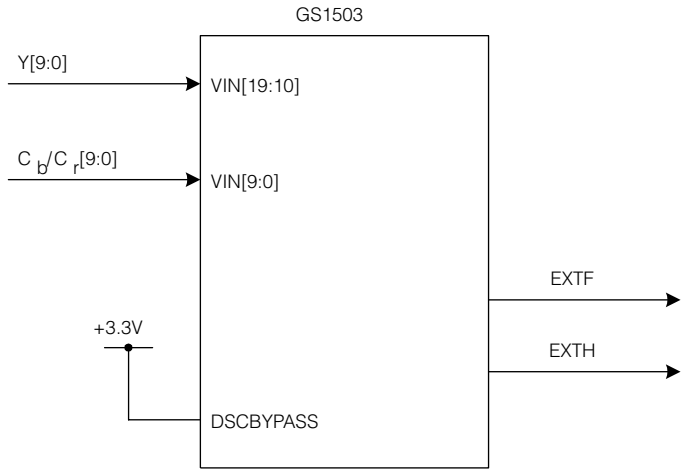


Fig. 32 10-bit Y and C_b/C_r Input with TRS and Line Numbers Configuration

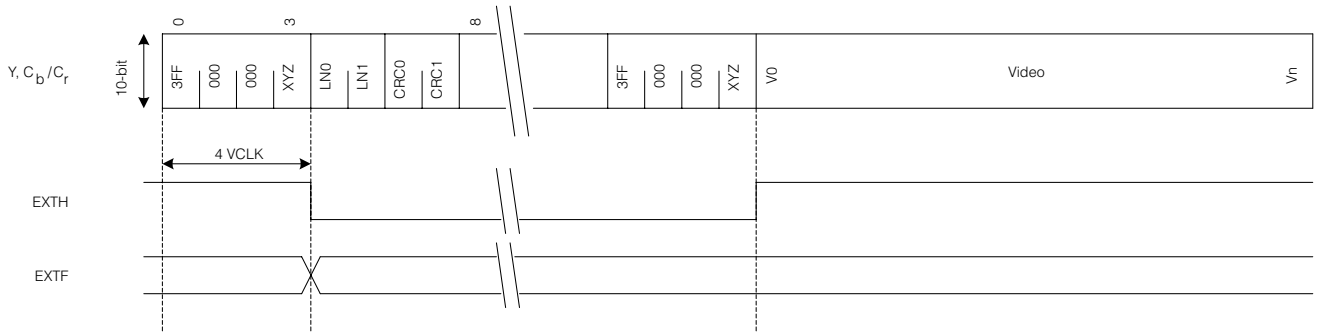


Fig. 33 Video Input Format (10-bit with TRS and Line Numbers)

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
EXT_SEL	0: EXTH/EXTF output select 1: EXTH/EXTF input select	001	3	0	0
8BIT_SEL	0: 10-bit mode select 1: 8-bit mode select		1	0	0
DSCBYPASS	0: Descrambling enabled 1: Bypass descrambling		0	1	0

2.4 VIDEO OUTPUT FORMAT

2.4.1 10-bit Y and C_b/C_r Output

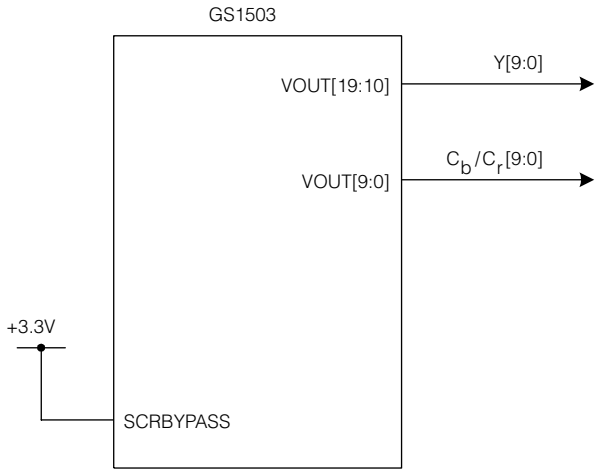


Fig. 34 10-bit Y and C_b/C_r Output Configuration

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
SCRBYPASS	0: SMPTE 292M scrambling enabled 1: Bypass SMPTE 292M scrambling	001	2	1	0

2.4.2 20-bit Scrambled Output

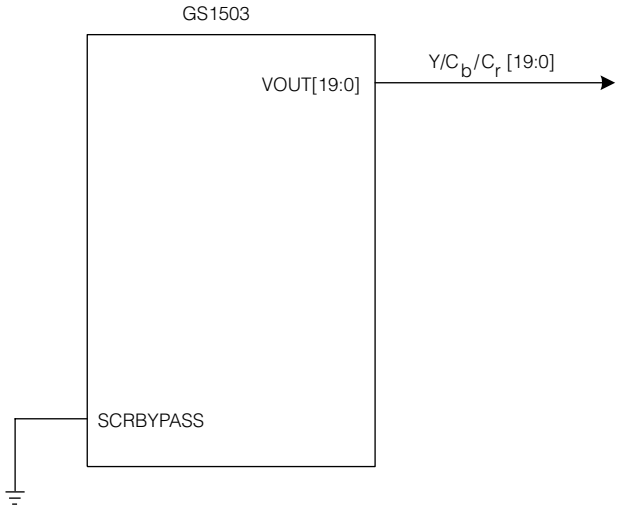


Fig. 35 20-bit Scrambled Output Configuration

Register Settings (Default Mode)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
SCRBYPASS	0: SMPTE 292M scrambling enabled 1: Bypass SMPTE 292M scrambling	001	2	0	0

2.5 VIDEO DATA PROCESSING

2.5.1 Video Signal Input Detection

The GS1503 will set the VIDEO_DET external pin HIGH when three consecutive TRS are detected in the input video signal. Also, the VIDEO_DET bit of Host Interface register 000h is set HIGH.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VIDEO_DET	Video input signal detection (1: Detection)	000	6	-	0

2.5.2 Video Input CRC Error Detection

The GS1503 will set the CRC_ERR external pin HIGH when a CRC error is detected in the input video signal. Also, the CRC_ERR bit 5 of Host Interface register 000h is set HIGH. The number of CRC errors accumulated in one video frame can be read form CRC_CNT[11:0] in Host Interface registers 006h and 007h.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CRC_ERR	Video input signal CRC error detection (1: Detection)	000	5	-	0
CRC_CNT[11:0]	Video input signal CRC error accumulation in 1 video frame	006 007	3-0 7-0	-	0

2.5.3 Video Output CRC Insertion

When the CRC_INS bit 4 of Host Interface register 000h is set HIGH, the GS1503 will re-calculate the video line CRC words. The re-calculated CRC words are inserted in the video output signal. When CRC_INS is set LOW, the line CRC words are not updated and existing CRC words at the input of the device will be output unchanged.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CRC_INS	Video line CRC insertion (1: Insertion)	000	4	1	1

2.5.4 Input Blanking

When VBLK_INS bit 3 of Host Interface register 008h is set HIGH, the input video vertical blanking will be set to 040h for the Luma channel and 200h for the Chroma channel.

When HBLK_INS bit 2 of Host Interface register 008h is set HIGH, the input video horizontal blanking will be set to 040h for the Luma channel and 200h for the Chroma channel. The TRS, line number and CRC words will also be set to blanking values.

The blanking function is performed at the output of the GS1503 video data stream. If the HBLK_INS bit is set HIGH, any embedded audio or control packets will be replaced with blanking codes. The GS1503 will demultiplex data contained in the packets, prior to the blanking function, and output at the corresponding pins.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
VBLK_INS	Input vertical blanking (1: Enabled)	008	3	1	0
HBLK_INS	Input horizontal blanking (1: Enabled)		2	1	0

2.5.5 Line Number Insertion

When LN_INS bit 1 of Host Interface register 008h is set HIGH, the GS1503 will insert line numbers into the video data stream. When set LOW, existing line numbers will remain in the output video stream.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
LN_INS	Line number insertion (1: Enabled)	008	1	1	1

2.5.6 TRS Word Insertion

When TRS_INS bit 0 of Host Interface register 008h is set HIGH, the GS1503 will insert TRS codes into the video data stream. When set LOW, existing TRS codes will remain in the output video stream.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
TRS_INS	TRS word insertion (1: Enabled)	008	0	1	1

2.6 AUDIO DATA PROCESSING

2.6.1 Digital Audio Output Format

The GS1503 has two audio output formats, AES/EBU digital audio output and serial output, as listed in Table 11. The serial audio output can be formatted in the following two modes. *See Figure 36:*

24-bit Left Justified; MSB first

24-bit Right Justified; MSB last

The audio output format is configured using the AM[1:0] external pins or via AM[1:0] bits 1-0 in Host Interface register 010h. To configure the audio output format via the Host Interface, AM_SEL bit 7 in Host Interface register 010h must be set HIGH. The GS1503 will default to the AM[1:0] external pin setting.

NOTE: When configured in AES/EBU audio mode, the GS1503 will not output a 48kHz (fs) word clock at the WCOUTA and WCOUTB pins.

Table 11: Audio Output Formats

AM[1:0]	AUDIO OUTPUT FORMAT
0	Serial audio output: 24-bit Left Justified; MSB first
1	Serial audio output: 24-bit Right Justified; MSB last
2	AES/EBU audio output

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
AM_SEL	0: External pin setting 1: Register setting	010	7	1	0
AM[1:0]	Audio output format selection (AM[1] is MSB)		1-0	*See Table 11*	0

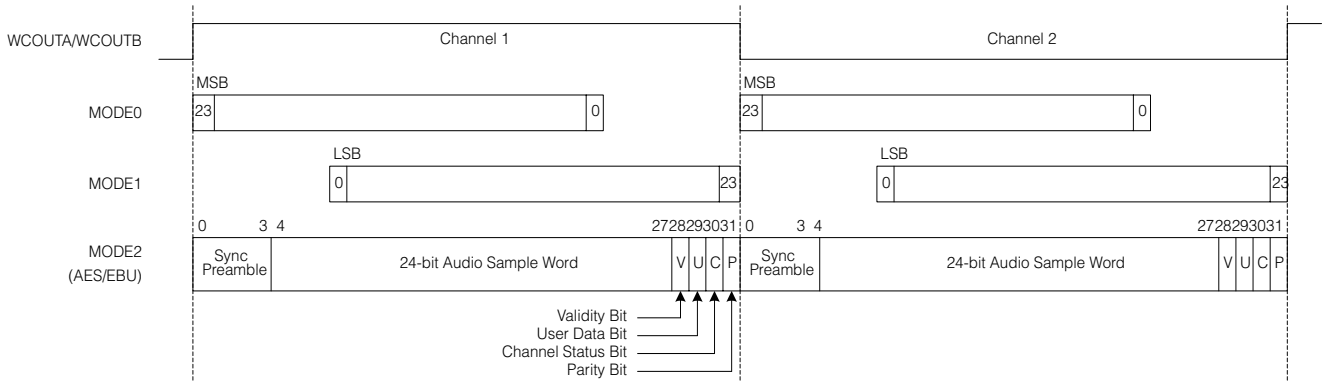


Fig. 36 Audio Output Formats

2.6.2 Digital Audio Output Timing

2.6.2.1 AES/EBU Format Output

A 6.144MHz (128fs) audio clock must be supplied to the ACLKA and ACLKB inputs. ACLKA is used to clock AES/EBU digital audio signal for channels 1 to 4 (AOUT1/2 and AOUT3/4). ACLKB is used to clock AES/EBU digital audio signal for channels 5 to 8 (AOUT5/6 and AOUT7/8). In AES/EBU output mode, the audio word clock inputs WCINB and WCINB should be grounded. *See Figure 37 for timing*.

The user can access the Audio Channel Status Block information via the AUDIO_CS[183:0] bits in Host Interface registers 058h to 06Eh. To read the Audio Channel Status information, the CS_MODE bit 3 of Host Interface register 06Fh should be set HIGH. The embedded audio channel from which the Channel Status information is to be extracted is set in the CH_SEL[2:0] bits 2-0 of Host Interface register 06Fh. The CH_SEL[2:0] setting for audio channel 1 is 000b, through to 111b for channel 8. The CS_RQST bit must be set HIGH to begin the process of extracting the Audio Channel Status information. Once extracted, the GS1503 will set CS_WEND bit HIGH and the user can access the data for Host Interface registers 058h to 06Eh.

When CS_MODE is set LOW, the Audio Channel Status information in the AES/EBU audio outputs will be replaced with data programmed in the AUDIO_CS[183:0] bits of Host Interface registers 058h to 06Eh.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CS_WEND	Audio Channel Status write flag (1: Data ready)	06F	5	-	0
CS_RQST	Audio Channel Status request (1: enable)		4	1	0
CS_MODE	0: Audio Channel Status replace 1: Audio Channel Status demultiplex		3	1	0
CH_SEL[2:0]	Audio Channel Status select		2-0	-	000b

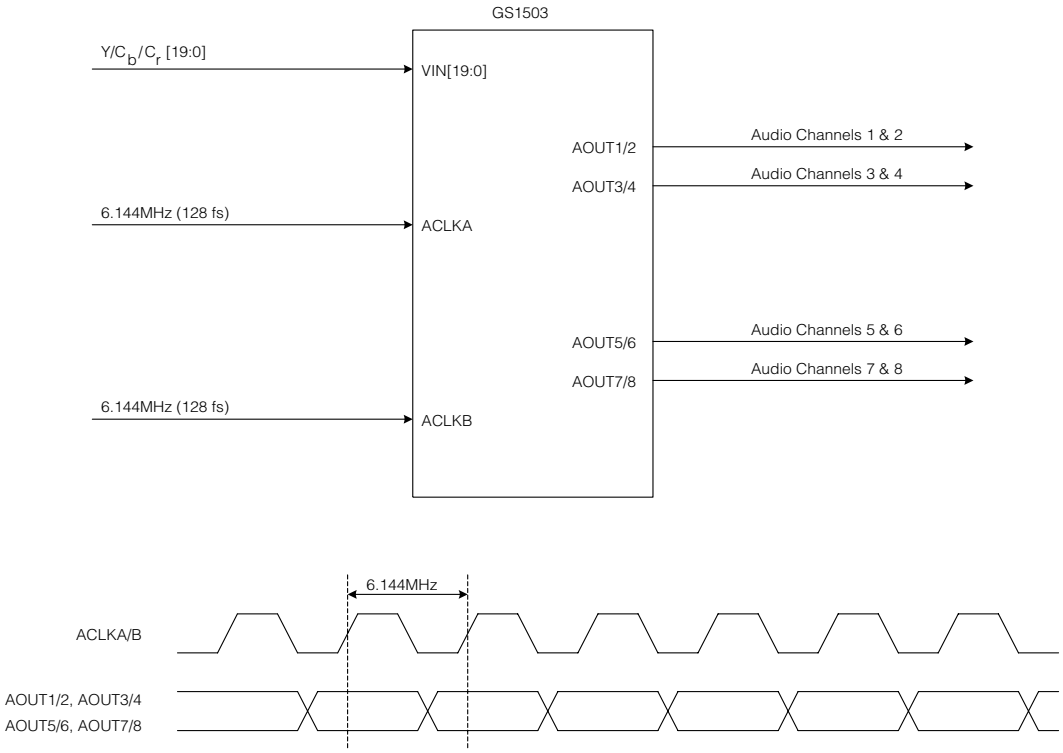


Fig. 37 AES/EBU Audio Output Configuration and Timing

2.6.2.2 Serial Audio Output Modes

A 6.144MHz (128fs) audio clock must be supplied to the ACLKA and ACLKB inputs. An audio word clock at 48kHz (fs) will be output at the WCOUTA and WCOUTB external pins, as shown in Figure 38.

The user can access the Audio Channel Status Block information via the AUDIO_CS[183:0] bits in Host Interface registers 058h to 06Eh. To read the Audio Channel Status information, the CS_MODE bit 3 of Host Interface register 06Fh should be set HIGH. The embedded audio channel from which the Channel Status information is to be extracted is set in the CH_SEL[2:0] bits 2-0 of Host Interface register 06Fh. The CH_SEL[2:0] setting for audio channel 1 is 000b, through to 111b for channel 8.

The CS_RQST bit must be set HIGH to begin the process of extracting the Audio Channel Status information. Once extracted, the GS1503 will set CS_WEND bit HIGH and the user can access the data for Host Interface registers 058h to 06Eh.

When DEC_MODE (external pin or register setting) is set LOW, the audio word clock inputs WCINB and WCINB should be grounded. *See section 2-12*.

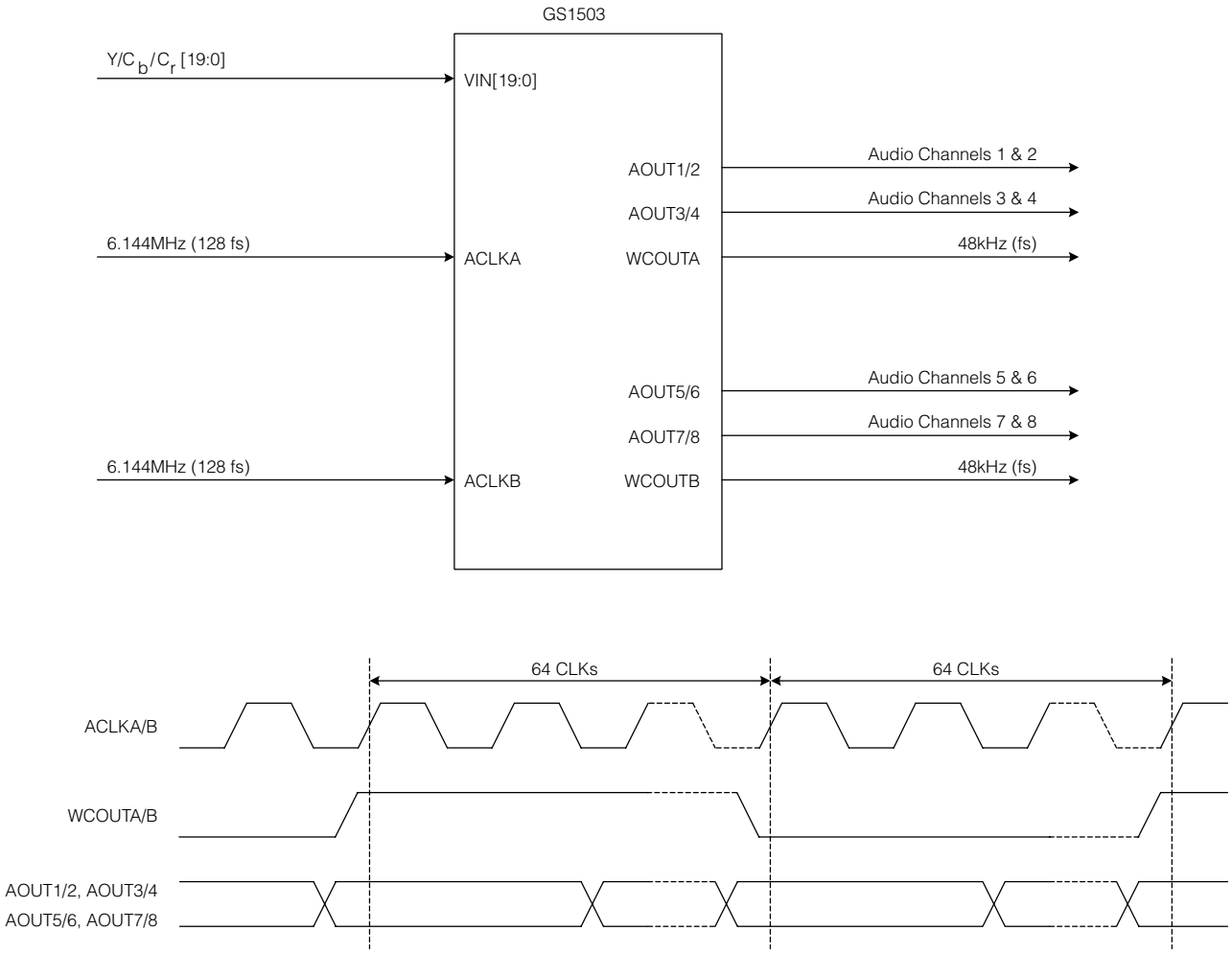


Fig. 38 Serial Audio Output Configuration and Timing

2.6.3 Audio Clock Phase Locked Loop

Figure 39 shows the configuration for deriving the 6.144MHz audio clock in AES/EBU and serial audio output modes. The GS1503 will internally synchronize the audio output to the corresponding ACLK. This configuration is not required when DEC_MODE is set HIGH. *See the Reference Design Section 3 for circuit specifics.*

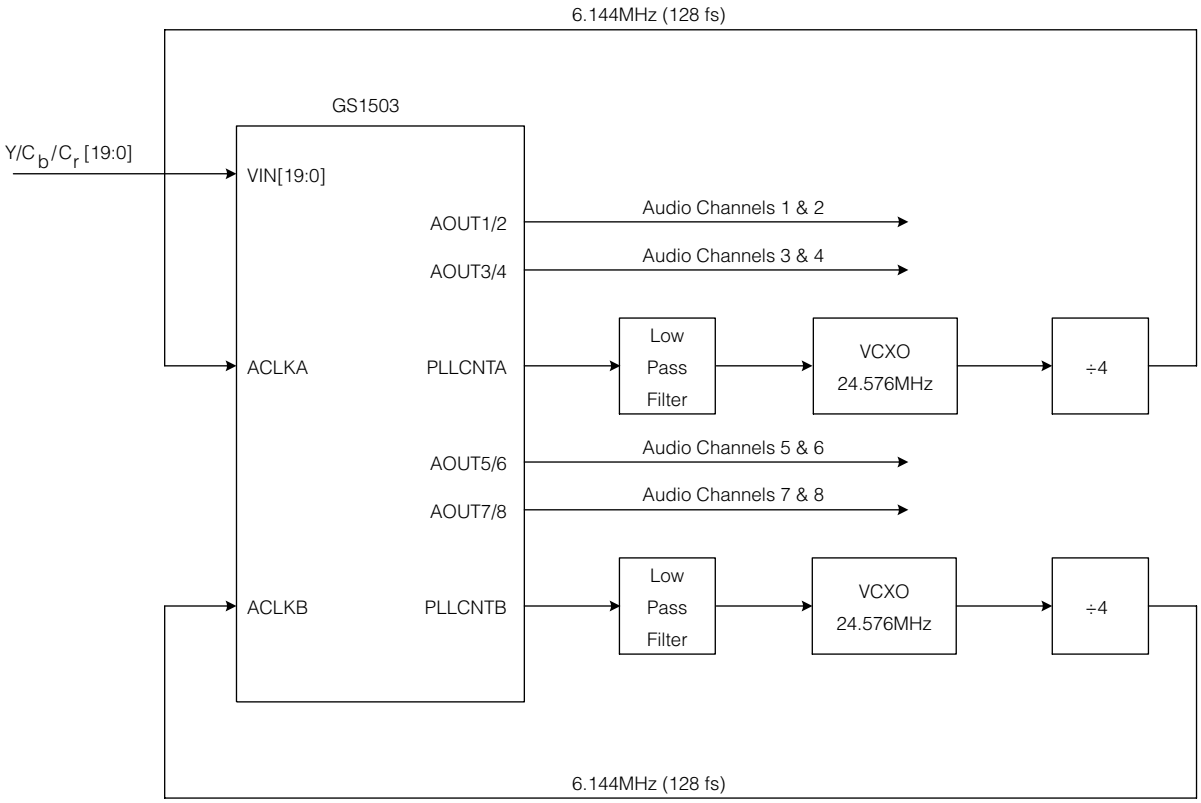


Fig. 39 Block Diagram of GS1503 Audio Clock PLL

2.6.4 Audio Data Packet Detection

The audio data packet detect registers will be set HIGH when a corresponding audio group DID has been detected in the Chroma channel of the input video stream. Host Interface register 013h, bits 7-4, report the individual audio groups detected.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ADPG4_DET	Audio group 4 data packet detection (1:Detection)	013	7	-	0
ADPG3_DET	Audio group 3 data packet detection (1:Detection)		6	-	0
ADPG2_DET	Audio group 2 data packet detection (1:Detection)		5	-	0
ADPG1_DET	Audio group 1 data packet detection (1:Detection)		4	-	0

2.6.5 ECC Error Detection & Correction

The GS1503 performs BCH(31,25) forward error detection and correction as described in SMPTE 299M. The error correction for audio data packets with audio group DID set in DATAIDA[1:0] is activated when ECCA_ON bit 0 of Host Interface register 013h is set HIGH. Similarly, error correction for audio data packets with audio group DID set in DATAIDB[1:0] is activated when ECCB_ON bit 1 of Host Interface register 013h is set HIGH

When a one-bit error is detected in a bit array of the ECC protected region of the audio data packet with audio group DID set in DATAIDA[1:0], ECCA_ERR bit 1 in Host Interface register 015h is set HIGH. When a one-bit error is detected in the ECC protected region of the audio data packet with audio group DID set in DATAIDB[1:0], the ECCB_ERR bit 5 in Host Interface register 015h is set HIGH. In both cases, the ERROR external pin will also be set HIGH.

A bit array is defined as all 24 bits of bit 0. The next bit array is all 24 bits of bit 1, and so on through to bit 7. Up to 8 bits in error can be corrected, providing each bit error is in a different bit array. When there are two bits in error in the same 24-bit array, the errors will be detected, but not corrected. When there are more than two bits in error in a single bit array, the errors will not be detected or corrected.

The number of audio data packets corrected in one video frame will be reported in the corresponding Host Interface registers CORRECTA[11:0] and CORRECTB[11:0]. The GS1503 will also report the number of audio data packets which could not be corrected in one video frame in the corresponding Host Interface registers NO_CORRECTA[11:0] and NO_CORRECTB[11:0].

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ECCB_ERR	Ch5-8 Audio data packet ECC error detection (1: Detection)	015	5	-	0
ECCA_ERR	Ch1-4 Audio data packet ECC error detection (1: Detection)		1	-	0
CORRECTB[11:0]	Ch5-8 correctable packets in one video frame	016 017	3-0 7-0	-	0
NO_CORRECTB[11:0]	Ch5-8 un-correctable packets in one video frame	018 019	3-0 7-0	-	0
CORRECTA[11:0]	Ch1-4 correctable packets in one video frame	01A 01B	3-0 7-0	-	0
NO_CORRECTA[11:0]	Ch5-8 un-correctable packets in one video frame	01C 01D	3-0 7-0	-	0
ECCB_ON	Ch5-8 Audio data packet error correction (1: ON)	013	1	1	1
ECCA_ON	Ch1-4 Audio data packet error correction (1: ON)		0	1	1

2.6.6 Audio Data Packet Error Detection

When the 1-255 count sequence in the Data Block Number (DBN) word of audio data packets with audio group DID set in DATAIDA[1:0] is discontinuous, the DBNA_ERR bit 3 of Host Interface register 015h will be set HIGH. When the1-255 count sequence in the DBN word of audio data packets with audio group DID set in DATAIDB[1:0] is discontinuous, the DBNB_ERR bit 7 of Host Interface register 015h will be set HIGH.

The GS1503 will check the parity (bit 8) for the CLK, CH1-4 and ECC0-5 words in the embedded audio data packets. When a parity bit error is detected in audio data packets with audio group DID set in DATAIDA[1:0], the ADPB8A_ERR bit 2 of Host Interface register 015h will be set HIGH. When a parity bit error is detected in audio data packets with audio group DID set in DATAIDB[1:0], the ADPB8B_ERR bit 6 of Host Interface register 015h will be set HIGH.

The GS1503 will re-calculate the audio data packets Checksum and compare against the embedded Checksum word. When a Checksum error is detected in audio data packets with audio group DID set in DATAIDA[1:0], the ADPCSA_ERR bit 0 of Host Interface register 015h will be set HIGH. When a Checksum error is detected in audio data packets with audio group DID set in DATAIDB[1:0], the ADPCSB_ERR bit 4 of Host Interface register 015h will be set HIGH.

When any of the above errors are detected, the ERROR external pin will also be set HIGH.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DBNB_ERR	Ch5-8 Audio data packet DBN error detection (1:Detection)	015	7	-	0
ADPB8B_ERR	Ch5-8 Audio data packet bit8 error detection (1:Detection)		6	-	0
ADPCSB_ERR	Ch5-8 Audio data packet CS error detection (1:Detection)		4	-	0
DBNA_ERR	Ch1-4 Audio data packet DBN error detection (1:Detection)		3	-	0
ADPB8A_ERR	Ch1-4 Audio data packet bit8 error detection (1:Detection)		2	-	0
ADPCSA_ERR	Ch1-4 Audio data packet CS error detection (1:Detection)		0	-	0

2.6.7 Audio Data Packet DID Setting

The audio group DID for audio output channels 1 to 4 (AOUT1/2 and AOUT3/4) is set in DATAIDA[1:0] bits 1-0 of Host Interface register 014h. The audio group DID for audio output channels 5 to 8 (AOUT5/6 and AOUT7/8) is set in DATAIDB[1:0] bits 3-2 of Host Interface register 014h. Table 12 shows the 2-bit Host Interface setting for the corresponding audio group DID.

When CASCADE is set LOW (external pin or register), the GS1503 will default to audio groups 1 and 2, where AOUT1/2 and AOUT3/4 will be demultiplexed from audio data packets with group 1 DID, and AOUT5/6 and AOUT7/8 will be demultiplexed from audio data packets with group 2 DID.

Table 12: Audio Group DID Host Interface Settings

AUDIO GROUP	10-BIT DATA	HOST INTERFACE REGISTER SETTING (2-BIT)
1	2E7h	11b
2	1E6h	10b
3	1E5h	01b
4	2E4h	00b

Register Settings (CASCADE set LOW)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DATAIDA[1-0]	Ch1-4 Audio data packet DID setting	014	1-0	*See Table 12*	11b
DATAIDB[1-0]	Ch5-8 Audio data packet DID setting		3-2		10b

When CASCADE is set HIGH (external pin or register), the GS1503 will default to audio groups 3 and 4, where AOUT1/2 and AOUT3/4 will be demultiplexed from audio data packets with group 3 DID, and AOUT5/6 and AOUT7/8 will be demultiplexed from audio data packets with group 4 DID.

Register Settings (CASCADE set HIGH)

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DATAIDA[1-0]	Ch1-4 Audio data packet DID setting	014	1-0	*See Table 12*	01b
DATAIDB[1-0]	Ch5-8 Audio data packet DID setting		3-2		00b

2.7 DEMULTIPLEX CASCADE MODE

Two GS1503 devices can be cascaded in parallel to allow up to 16 channels of audio to be demultiplexed (only one device requires CASCADE to be set HIGH). Figure 40 shows the cascade architecture for a 16-channel system. To configure the GS1503 for cascade mode, the CASCADE external pin or CASCADE bit 7 of Host Interface register 014h is set HIGH. When set HIGH, the GS1503 will default to audio groups 3 and 4. When set LOW, the GS1503 will default to audio groups 1 and 2.

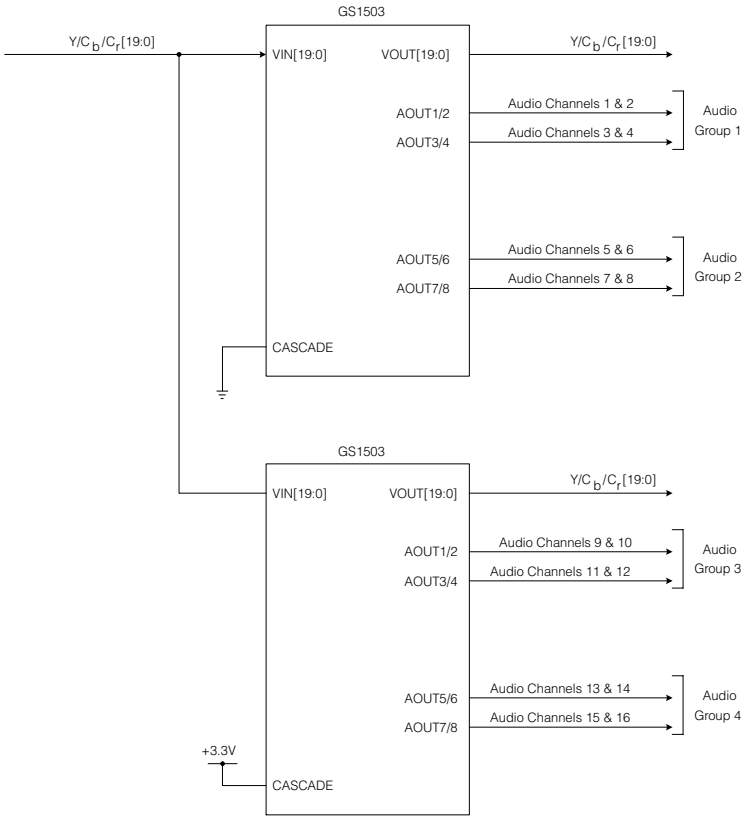


Fig. 40 Demultiplexing 16 Channels of Audio using Cascade Architecture

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CASCADE	Cascade enable (1: Enabled)	014	7	1	0

2.8 AUDIO CONTROL PACKETS

2.8.1 Audio Control Packet Detection

The audio control packet detect registers will be set HIGH when a corresponding audio group DID has been detected in the Luma channel of the input video stream. Host Interface register 020h, bits 7-4, report the individual audio groups detected.

The audio control packet group DID for audio output channels 1 to 4 is set in CTRIDA[1:0] bits 1-0 of Host Interface register 02Fh. The audio control packet group DID for audio output channels 5 to 8 is set in CTRIDB[1:0] bits 3-2 of Host Interface register 020h. Table 13 shows the 2-bit Host Interface setting for the corresponding audio control packet group DID.

2.8.2 Audio Control Packet DID Setting

To demultiplex audio control packets for audio channels 1 to 4 (AOUT1/2 and AOUT3/4), the CTRONA bit 2 of Host Interface register 02Fh is set HIGH. To demultiplex audio control packets for audio channels 5 to 8 (AOUT5/6 and AOUT7/8), the CTRONB bit 2 of Host Interface register 020h is set HIGH.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ACPG4_DET	Audio group 4 control packet detection (1: Detection)	020	7	-	0
ACPG3_DET	Audio group 3 control packet detection (1: Detection)		6	-	0
ACPG2_DET	Audio group 2 control packet detection (1: Detection)		5	-	0
ACPG1_DET	Audio group 1 control packet detection (1: Detection)		4	-	0

When CASCADE is set LOW (external pin or register), the GS1503 will default to audio groups 1 and 2, where audio control packet data for channels 1 to 4 will be demultiplexed from packets with group 1 DID, and audio control packet data for channels 5 to 8 will be demultiplexed from packets with group 2 DID.

Control packet data is accessible via the corresponding registers in the Host Interface.

Table 13: Audio Control Packet Group DID Host Interface Settings

AUDIO GROUP	10-BIT DATA	HOST INTERFACE REGISTER SETTING (2-BIT)
1	1E3h	11b
2	2E2h	10b
3	2E1h	01b
4	1E0h	00b

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CTRONA	Ch1-4 Audio control packet demultiplex enable (1: Enabled)	02F	2	1	1
CTRIDA[1:0]	Ch1-4 Audio control packet DID set		1-0	*See Table 13*	11b
AF_NOA[8:0]	Ch1-4 Audio frame number	030 031	0 7-0		0
RATEA[2:0]	Ch1-4 Sampling frequency data	032	3-1	-	0
ASXA	Ch1-4 Synchronization (0: Synchronous; 1: Non-synchronous)		0	-	0
DEL1-2A[26:0]	Ch1/2 Delay data	033 034 035 036	1-0 7-0 7-0 7-0	-	0
DEL3-4A[26:0]	Ch3/4 Delay data	037 038 039 03A	1-0 7-0 7-0 7-0	-	0
RSRVA[17:0]	Ch1-4 Reserved words	03B 03C 03D	1-0 7-0 7-0	-	0

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
CTRONB	Ch5-8 Audio control packet demultiplex enable (1: Enabled)	020	2	1	1
CTRIDB[1:0]	Ch5-8 Audio control packet DID set		1-0	*See Table 13*	10b
AF_NOB[8:0]	Ch5-8 Audio frame number	021 022	0 7-0	-	0
RATEB[2:0]	Ch5-8 Sampling frequency data	023	3-1	-	0
ASXB	Ch5-8 Synchronization (0: Synchronous; 1: Non-synchronous)		0	-	0
DEL1-2B[26:0]	Ch5/6 Delay data	024 025 026 027	1-0 7-0 7-0 7-0	-	0
DEL3-4B[26:0]	Ch7/8 Delay data	028 029 02A 02B	1-0 7-0 7-0 7-0	-	0
RSRVB[17:0]	Ch5-8 Reserved words	02C 02D 02E	1-0 7-0 7-0	-	0

2.9 ARBITRARY DATA PACKETS

The GS1503 can demultiplex arbitrary data packets according to SMPTE 291M. Typically, arbitrary data packets consist of linear time code (LTC), vertical interval time code (VITC) or other user data, which is multiplexed once per video field. The GS1503 has two modes in which arbitrary data can be demultiplexed from the Luma channel of the video data stream. A maximum of 255 user data words can be demultiplexed. Figure 41 shows the structure of the arbitrary data packet.

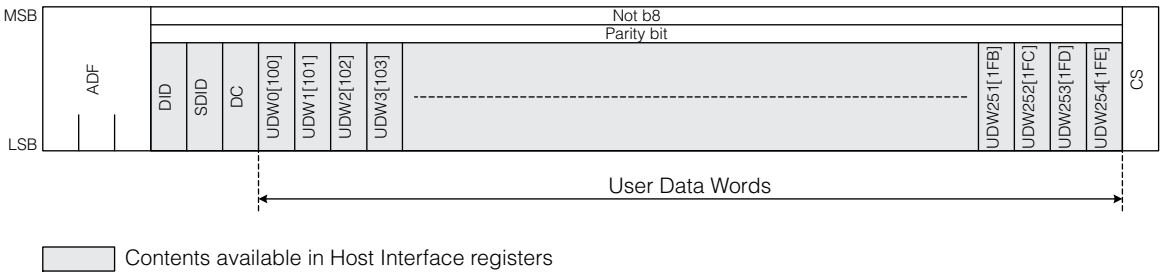


Fig. 41 Arbitrary Data Packet Structure

2.9.1 Arbitrary Data Demultiplexing in External Pin Mode

This is the default mode for demultiplexing arbitrary data packets. The GS1503 will set the PKTEN external pin HIGH before arbitrary data will be output. Two VCLK cycles after PKTEN goes HIGH, arbitrary data is output on the PKT[7:0] bus. See Figure 42 for timing.

The following arbitrary data is output on the PKT[7:0] bus: Data ID (DID), Secondary Data ID (SDID), Data Count (DC) and User Data Words (UDW: up to a maximum of 255 words).

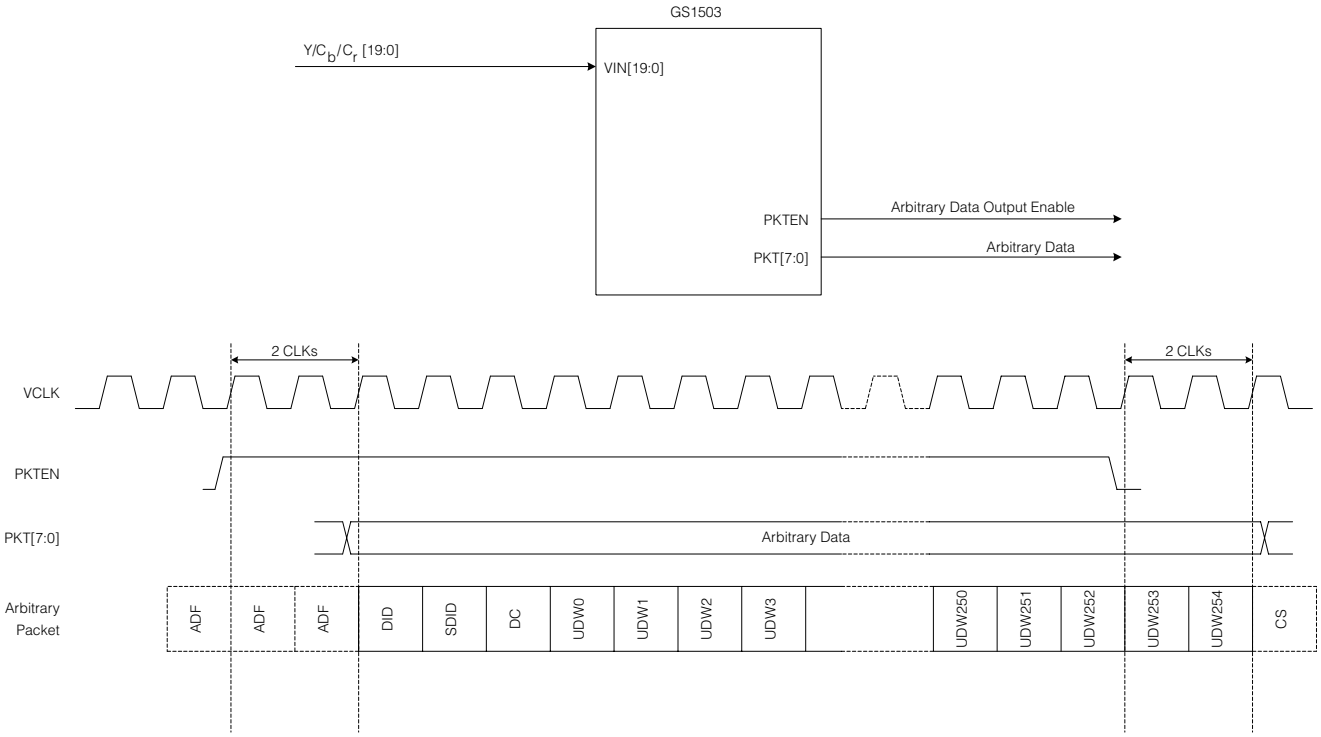


Fig. 42 Arbitrary Data Packet Output Timing Diagram

2.9.2 Arbitrary Data Demultiplexing in Host Interface Mode

To select this mode, set ARBITMODE bit 0 in Host Interface register 050h HIGH. In this mode, the DID, SDID, DC and User Data Words must be programmed in the corresponding Host Interface registers. Set the video line number for field 1 and field 2 from which the arbitrary data packets are to be demultiplexed using the ARBITLINEA[12:0] and ARBITLINEB[12:0] Host Interface registers respectively. The arbitrary data packet is demultiplexed when the ARBITON bit 1 in Host Interface register 050h is set HIGH. ARBITON should be set LOW when reading the arbitrary data packet User Data Words from the ARBITUDW Host Interface registers.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ARBITON	Arbitrary packet demultiplex enable (1: Enabled) Valid only when ARBITMODE is HIGH	050	1	1	0
ARBITMODE	Arbitrary packet mode selection (0: External pin mode; 1: Host mode)		0	1	0
ARBITDID[7-0]	Arbitrary packet DID setting	051	7-0	-	0
ARBITSDID[7-0]	Arbitrary packet SDID setting	052	7-0	-	0
ARBITDC[7-0]	Arbitrary packet DC setting	053	7-0	-	0
ARBITLINEA[12:0]	Field 1 multiplexing line	054 055	3-0 7-0	-	0
ARBITLINEB[12:0]	Field 2 multiplexing line	056 057	3-0 7-0	-	0
ARBITUDW	Arbitrary packet UDW	100-1FE	7-0	-	0

2.10 ANCILLARY DATA DELETION

The GS1503 can be configured to delete the embedded ancillary data packets, after demultiplexing. There are two modes for ancillary data deletion.

2.10.1 Entire Ancillary Data Deletion

When the ANCI external pin or ANCI bit 1 of Host Interface register 040h is set HIGH, all ancillary data packets in both the Luma and Chroma channel of the input video stream are deleted. The data is replaced with blanking values 040h in the Luma channel and 200h in the Chroma channel. The DEL_SEL bit 0 of Host Interface register 040h must be set LOW.

2.10.2 Audio Group Designation Ancillary Data Deletion

When the ANCI bit 1 of Host Interface register 040h is set HIGH, and DEL_SEL bit 0 of Host Interface register 040h is HIGH, only audio data and control packets which are designated in Host Interface registers 041h will be deleted. To delete the arbitrary data packets, the corresponding DID must be set in the NDID[7:0] Host Interface register 042h.

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
ANCI	Ancillary data packet delete (1: Deletion enabled)	040	1	1	0
DEL_SEL	Ancillary data packet delete mode select (0: Entire data delete; 1: Group designated data delete)		0	1	0
ADPG4_DEL	Audio group 4 data packet delete (1: Delete)	041	7	-	0
ADPG3_DEL	Audio group 3 data packet delete (1: Delete)		6	-	0
ADPG2_DEL	Audio group 2 data packet delete (1: Delete)		5	-	0
ADPG1_DEL	Audio group 1 data packet delete (1: Delete)		4	-	0
ACPG4_DEL	Audio group 4 control packet delete (1: Delete)		3	-	0
ACPG3_DEL	Audio group 3 control packet delete (1: Delete)		2	-	0
ACPG2_DEL	Audio group 2 control packet delete (1: Delete)		1	-	0
ACPG1_DEL	Audio group 1 control packet delete (1: Delete)		0	-	0
NDID[7:0]	Arbitrary packet DID delete setting	042	7-0	-	0

2.11 DEMULTIPLEX MODE WITH WORD CLOCK INPUT

Some commercially available HD audio embedding modules do not encode the audio word clock phase information correctly in the CLK words of the audio data packet. If this clock information is not correctly encoded, the GS1503 will not output the audio data correctly. Also, the GS1503 will be unable to reproduce the 48kHz audio word clock (fs) at the WCOUTA and WCOUTB pins in serial audio output modes.

If the GS1503 is to be used in conjunction with a HD audio module, which encodes audio clock phase information incorrectly, the DEC_MODE external pin or DECMODE bit 2 of Host Interface register 01Eh must be set HIGH. When HIGH, an audio word clock synchronous to the original word clock used for embedding must be input at the WCINA and WCINB pins. Figure 43 shows a system example.

When the embedded clock phase data for audio channel 1 to 4 is detected as being in error, the MUXERRA bit 0 of Host Interface register 01Eh will be set HIGH. Similarly, when the embedded clock phase data for audio channel 5 to 8 is detected as being in error, the MUXERRB bit 1 of Host Interface register 01Eh will be set HIGH

Register Settings

NAME	DESCRIPTION	ADDRESS	BIT	SETTING	DEFAULT
DECMODE	Demultiplex Mode with word clock input enable (1: Enabled)	01E	2	1	0
MUXERRB	Ch5-8 embedded clock phase information error detect (1: Detected)		1	-	0
MUXERRA	Ch1-4 embedded clock phase information error detect (1: Detected)		0	-	0

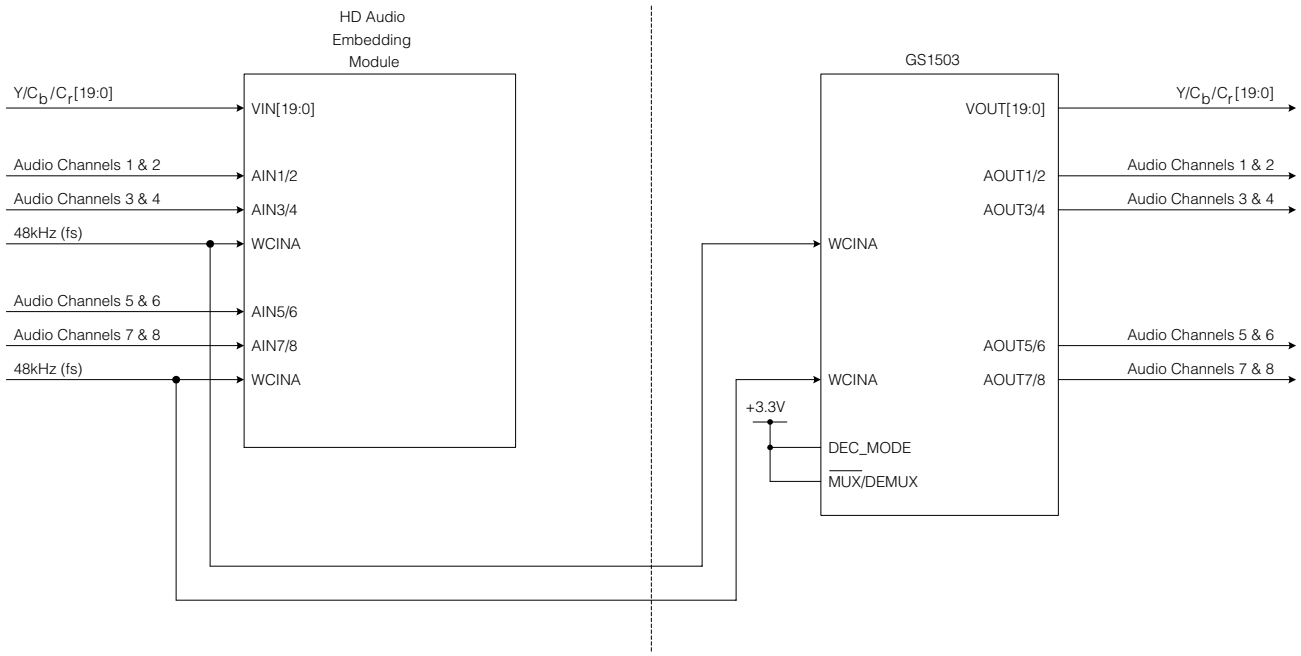


Fig. 43 Demultiplex Mode with 48kHz Word Clock Input System Example

Figure 44 shows the timing relationship between the audio word clock inputs and word clock outputs when the GS1503 is configured to serial audio output mode.

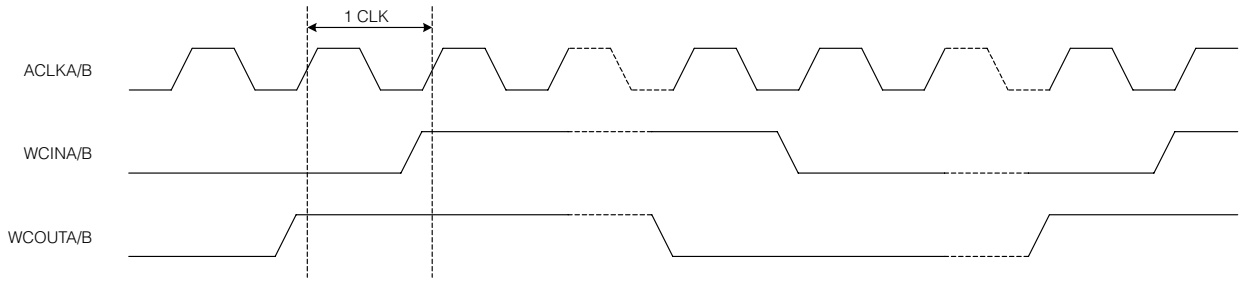


Fig. 44 WCINA/B Input to WCOUTA/B Output Timing Diagram

Table 14: Demultiplex Mode Host Interface Registers

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Video	VM_SEL	Video input format (external pin/internal register) configuration select. When set LOW, the video input format is configured via the VM[3:0] pins. When set HIGH, the video input format is configured via the "VM[3:0]" bits.	000	7	R/W	0
	VIDEO_DET	Video signal detection flag. Set HIGH when 3 consecutive TRS are detected in the input video signal.		6	R	0
	CRC_ERR	Video input signal CRC error detection. Set HIGH when a CRC error is detected in the input video signal. This register is refreshed on every video frame.		5	R	0
	CRC_INS	Video CRC insertion. When set HIGH, the Luma and Chroma line CRC words are re-calculated and inserted into the output video signal.		4	R/W	1
	VM[3:0]	Video input format selection. *See Table 10*. Valid when "VM_SEL" is HIGH.		3-0	R/W	0
	EXT_SEL	External EXTH/EXTF input select. When set LOW, the EXTH and EXTF pins are configured as outputs. When set HIGH, the GS1503 will insert TRS and Line Numbers based on signals input at the EXTH and EXTF pins.	001	3	R/W	0
	SCRBYPASS	Scramble processing bypass select. When set HIGH, the internal scrambler and NRZ(I) encoder is bypassed. NOTE: The status of the SCRBYPASS external pin is not updated in this register. The value programmed in this register is logical OR'd with the SCRBYPASS external pin setting.		2	R/W	0
	8BIT_SEL	8-bit input selection. When set HIGH, the GS1503 will accept an 8-bit input video signal.		1	R/W	0
	DSCBYPASS	Descramble process bypass select. When set HIGH, the internal SMPTE 292M descrambler is bypassed. NOTE: The status of the DSCBYPASS external pin is not updated in this register. The value programmed in this register is logical OR'd with the DSCBYPASS external pin setting.		0	R/W	0
	CRC_CNT[11:0]	CRC error accumulation. Reports the accumulated number of CRC errors in one video frame.	006 007	3-0 7-0	R	0
	RSV	Not used.	008	7-4	R/W	0
	VBLK_INS	Vertical blanking enable. When set HIGH, the output video vertical blanking will be set to 040h for the Luma channel and 200h for the Chroma channel.		3	R/W	0
	HBLK_INS	Horizontal blanking enable. When set HIGH, the output video horizontal blanking, including TRS, line numbers and line CRC words, will be set to 040h for the Luma channel and 200h for the Chroma channel. NOTE: If blanking of line numbers and TRS words is required, LN_INS and TRS_INS must be set LOW.		2	R/W	0

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	LN_INS	Line insertion enable. When set HIGH, the GS1503 will insert line numbers into the video data stream. When set LOW, existing line numbers will remain in the output video stream.		1	R/W	1
	TRS_INS	TRS insertion enable. When set HIGH, the GS1503 will insert TRS codes into the video data stream. When set LOW, existing TRS codes will remain in the output video stream.		0	R/W	1
Audio	AM_SEL	Audio input format (external pin/register) configuration select. When set LOW, the audio input format is configured via the AM[1:0] pins. When set HIGH, the audio input format is configured via the "AM[1:0]" bits.	010	7	R/W	0
	RSV	Not used.		6-2	-	0
	AM[1:0]	Audio input format select. *See Table 11.* Valid when "AM_SEL" is HIGH.		1-0	R/W	0
	RSV	Not used.	01E	7-3	-	0
	DECMODE	Demultiplex Mode select. When set HIGH, the GS1503 requires a 48kHz word clock input at WCINA and WCINB. This word clock must be synchronous to the word clock used to embed the audio data. The embedded clock information in the audio data packet will be ignored. *See Section 2-12.* NOTE: The status of the DEC_MODE external pin is not updated in this register. The value programmed in this register is logical OR'd with the DEC_MODE external pin setting.		2	R/W	0
	MUXERRB	Ch5-8 audio sample clock error. When set HIGH, the GS1503 is unable to recover the audio clock phase data in the embedded audio data packet for audio channels 5 to 8. *See Section 2-12.*		1	R	0
	MUXERRA	Ch1-4 audio sample clock error. When set HIGH, the GS1503 is unable to recover the audio clock phase data in the embedded audio data packet for audio channels 1 to 4. *See Section 2-12.*		0	R	0
Audio Channel Status Block	AUDIO_CS[7:0] : AUDIO_CS [183:176]	Audio Channel Status. When "CS_MODE" is set HIGH, the 22 8-bit bytes of the Audio Channel Status Block, as defined in AES3-1992, are available in these registers. Valid in both AES/EBU and serial audio modes. When "CS_MODE" is set LOW, the Audio Channel Status information in the AES/EBU audio outputs will be replaced with data programmed in these registers. Valid only in AES/EBU audio mode.	058 : 06E	7-0 : 7-0	R	0
	RSV	Not used	06F	7-6	-	0

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	CS_WEND	Audio Channel Status write flag. When set HIGH, indicates that the audio channel status information has been written into the Host Interface registers 058h to 06Eh and can be read by the user. Valid only when "CS_MODE" is set HIGH.		5	R	0
	CS_RQST	Audio Channel Status request. When set HIGH, the GS1503 will read and store the Audio Channel Status information from the audio channel set in Host Interface register "CH_SEL[2:0]". Valid only when "CS_MODE" is set HIGH.		4	R/W	0
	CS_MODE	Audio Channel Status mode. When set HIGH, the user can access the embedded Audio Channel Status information from the Host Interface registers 058h to 06Eh. Valid in both AES/EBU and serial audio modes. When set LOW, the Audio Channel Status information for all audio outputs will be replaced with data programmed in Host Interface registers 058h - 06Eh. Valid only in AES/EBU audio mode.		3	R/W	0
	CH_SEL[2:0]	Audio Channel Status select. Designates the embedded audio channel from which the Audio Channel Status information will be demultiplexed. The setting 000b represent audio channel 1, through to 111b for channel 8. Valid only when "CS_MODE" is set HIGH.		2-0	R/W	000b

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Audio Data Packet	ADPG4_DET	Audio group 4 data packet detect. When set HIGH, audio data packets with group 4 DID have been detected in the incoming Chroma video data stream. NOTE: Once this bit has been set, it will remain set until a device reset is performed.	013	7	R	0
	ADPG3_DET	Audio group 3 data packet detect. When set HIGH, audio data packets with group 3 DID have been detected in the incoming Chroma video data stream. NOTE: Once this bit has been set, it will remain set until a device reset is performed.		6	R	0
	ADPG2_DET	Audio group 2 data packet detect. When set HIGH, audio data packets with group 2 DID have been detected in the incoming Chroma video data stream. NOTE: Once this bit has been set, it will remain set until a device reset is performed.		5	R	0
	ADPG1_DET	Audio group 1 data packet detect. When set HIGH, audio data packets with group 1 DID have been detected in the incoming Chroma video data stream. NOTE: Once this bit has been set, it will remain set until a device reset is performed.		4	R	0
	RSV	Not used.		3-2	-	0
	ECCB_ON	Ch5-8 error correction enable. When set HIGH, the GS1503 will perform error correction on audio data packets for channels 5 to 8, based on the six ECC words.		1	R/W	1
	ECCA_ON	Ch1-4 error correction enable. When set HIGH, the GS1503 will perform error correction on audio data packets for channels 1 to 4, based on the six ECC words.		0	R/W	1

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	CASCADE	Cascade select. When set HIGH, the GS1503 will default to audio groups 3 and 4. When set LOW, the GS1503 will default to audio groups 1 and 2. NOTE: The status of the CASCADE external pin is not updated in this register. The value programmed in this register is logical OR'd with the CASCADE external pin setting.	014	7	R/W	0
	RSV	Not used.		6	-	0
	AMUTEB	Ch5-8 audio mute enable. When set HIGH, the multiplexed audio packets for audio channels 5 to 8 are forced to zero. NOTE: The status of the MUTE external pin is not updated in this register. The value programmed in this register is logical OR'd with the MUTE external pin setting.		5	R/W	0
	AMUTEA	Ch1-4 audio mute enable. When set HIGH, the multiplexed audio packets for audio channels 1 to 4 are forced to zero. NOTE: The status of the MUTE external pin is not updated in this register. The value programmed in this register is logical OR'd with the MUTE external pin setting.		4	R/W	0
	DATAIDB[1:0]	Ch5-8 audio group DID setting. Designates the audio group DID for audio channels 5 to 8. *See Table 12*. When CASCADE (external pin or register) is set HIGH, the default setting is audio group 2. When CASCADE is set HIGH, the default setting is audio group 4.		3-2	R/W	10b
	DATAIDA[1:0]	Ch1-4 audio group DID setting. Designates the audio group DID for audio channels 1 to 4. *See Table 12*. When CASCADE (external pin or register) is set HIGH, the default setting is audio group 1. When CASCADE is set HIGH, the default setting is audio group 3.		1-0	R/W	11b

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	DBNB_ERR	Ch5-8 audio data packet DBN error. When set HIGH, a Data Block Number has been detected in the audio data packet for audio channels 5 to 8.	015	7	R	0
	ADPB8B_ERR	Ch5-8 audio data packet 'bit 8' error. When set HIGH, a 'bit 8' error has been detected in the audio data packet for audio channels 5 to 8.		6	R	0
	ECCB_ERR	Ch5-8 audio data packet error. When set HIGH, an error has been detected in the audio data packet for audio channels 5 to 8, based on the six ECC words.		5	R	0
	ADPCSB_ERR	Ch5-8 audio data packet CS error. When set HIGH, a Checksum error has been detected with the audio data packet for audio channels 5 to 8.		4	R	0
	DBNA_ERR	Ch1-4 audio data packet DBN error. When set HIGH, a Data Block Number has been detected in the audio data packet for audio channels 1 to 4.		3	R	0
	ADPB8A_ERR	Ch1-4 audio data packet 'bit 8' error. When set HIGH, a 'bit 8' error has been detected in the audio data packet for audio channels 1 to 4.		2	R	0
	ECCA_ERR	Ch1-4 audio data packet error. When set HIGH, an error has been detected in the audio data packet for audio channels 1 to 4, based on the six ECC words.		1	R	0
	ADPCSA_ERR	Ch1-4 audio data packet CS error. When set HIGH, a Checksum error has been detected with the audio data packet for audio channels 1 to 4.		0	R	0
	CORRECTB [11:0]	Ch5-8 ECC correctable packets. Designates the number of audio data packets for channels 5 to 8 that have been corrected in one video frame using the BCH forward error correction system.	016 017	3-0 7-0	R	0
	NO_CORRECTB [11:0]	Ch5-8 ECC un-correctable packets. Designates the number of audio data packets for channels 5 to 8 that could not be corrected in one video frame using the BCH forward error correction system.	018 019	3-0 7-0	R	0
	CORRECTA [11:0]	Ch1-4 ECC correctable packets. Designates the number of audio data packets for channels 1 to 4 that have been corrected in one video frame using the BCH forward error correction system.	01A 01B	3-0 7-0	R	0
	NO_CORRECTA [11:0]	Ch1-4 ECC un-correctable packets. Designates the number of audio data packets for channels 1 to 4 that could not be corrected in one video frame using the BCH forward error correction system.	01C 01D	3-0 7-0	R	0

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Audio Control Packet	ACPG4_DET	Audio group 4 control packet detect. When set HIGH, audio control packets with group 4 DID have been detected in the incoming Luma video data stream.	020	7	R	0
	ACPG3_DET	Audio group 3 control packet detect. When set HIGH, audio control packets with group 3 DID have been detected in the incoming Luma video data stream.		6	R	0
	ACPG2_DET	Audio group 2 control packet detect. When set HIGH, audio control packets with group 2 DID have been detected in the incoming Luma video data stream.		5	R	0
	ACPG1_DET	Audio group 1 control packet detect. When set HIGH, audio control packets with group 1 DID have been detected in the incoming Luma video data stream.		4	R	0
	RSV	Not used.		3	-	0
	CTRONB	Ch5-8 audio control packet demultiplex enable. When set HIGH, the audio control packets in the Luma channel of the video data stream for audio channels 5 to 8 will be demultiplexed.		2	R/W	1
	CTRIDB[1:0]	Ch5-8 audio control packet DID setting. Designates the audio control packet DID for audio channels 5 to 8. *See Table 13*. The default setting is audio group 2.		1-0	R/W	10b
	AF_NOB[8:0]	Ch5-8 audio frame number. Designates the audio frame number for audio channels 5 to 8.	021 022	0 7-0	R/W	0
	RATEB[2:0]	Ch5-8 sampling frequency. Designates the audio sampling frequency for audio channels 5 to 8, taken from the RATE word of the audio control packet as defined in SMPTE 299M.	023	3-1	R/W	0
	ASXB	Ch5-8 synchronization. When set HIGH, the "asx" bit of the audio control packet RATE word designates audio channels 5 to 8 as asynchronous, as per SMPTE 299M. When set LOW, the "asx" bit of the audio control packet RATE word designates synchronous audio.		0	R/W	0
	DEL1-2B[26:0]	Ch5/6 delay data. Designates the accumulated audio processing delay relative to video for audio channels 5 and 6.	024 025 026 027	1-0 7-0 7-0 7-0	R/W	0
	DEL3-4B[26:0]	Ch7/8 delay data. Designates the accumulated audio processing delay relative to video for audio channels 7 and 8.	028 029 02A 02B	1-0 7-0 7-0 7-0	R/W	0
	RSRVB[17:0]	Ch5-8 reserve words. Designates the value set in the RSRV words of the audio control packet for audio channels 5 to 8, as per SMPTE 299M.	02C 02D 02E	1-0 7-0 7-0	R/W	0

Table 14: Demultiplex Mode Host Interface Registers (Continued)

CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	RSV	Not used.	02F	7-3	-	0
	CTRONA	Ch1-4 audio control packet demultiplex enable. When set HIGH, the audio control packets in the Luma channel of the video data stream for audio channels 1 to 4 will be demultiplexed.		2	R/W	1
	CTRIDA[1:0]	Ch1-4 audio control packet DID setting. Designates the audio control packet DID for audio channels 1 to 4. *See Table 13*. The default setting is audio group 1.		1-0	R/W	11b
	AF_NOA[8:0]	Ch1-4 audio frame number. Designates the audio frame number for audio channels 1 to 4.	030 031	0 7-0	R/W	0
	RATEA[2:0]	Ch1-4 sampling frequency. Designates the audio sampling frequency for audio channels 1 to 4, taken from the RATE word of the audio control packet as defined in SMPTE 299M.	032	3-1	R/W	0
	ASXA	Ch1-4 synchronization. When set HIGH, the "asx" bit of the audio control packet RATE word designates audio channels 1 to 4 as asynchronous, as per SMPTE 299M. When set LOW, the "asx" bit of the audio control packet RATE word designates synchronous audio.		0	R/W	0
	DEL1-2A[26:0]	Ch1/2 delay data. Designates the accumulated audio processing delay relative to video for audio channels 1 and 2.	033 034 035 036	1-0 7-0 7-0 7-0	R/W	0
	DEL3-4A[26:0]	Ch3/4 delay data. Designates the accumulated audio processing delay relative to video for audio channels 3 and 4.	037 038 039 03A	1-0 7-0 7-0 7-0	R/W	0
	RSRVA[17:0]	Ch1-4 reserve words. Designates the value set in the RSRV words of the audio control packet for audio channels 1 to 4, as per SMPTE 299M.	03B 03C 03D	1-0 7-0 7-0	R/W	0
Packet Delete	RSV	Not used.	040	7-2	-	0
	ANCI	Ancillary data delete. When set HIGH, all ancillary data packets ("DEL_SEL" is LOW) or ancillary data packets with DIDs designated in Host Interface registers 041h and 042h ("DEL_SEL" is HIGH) are removed from the video signal. The ancillary data packets are replaced with blanking codes. The data contained in the packets are output at the corresponding pins. When set LOW, all ancillary data packets remain in the video signal. NOTE: The status of the ANCI external pin is not updated in this register. The value programmed in this register is logical OR'd with the ANCI external pin setting		1	R/W	0
	DEL_SEL	Ancillary data delete mode select. When set HIGH, individual audio groups can be deleted from the video signal by programming Host Interface register 041h. When set LOW, all ancillary data packets are deleted from the video signal.		0	R/W	0

Table 14: Demultiplex Mode Host Interface Registers (Continued)

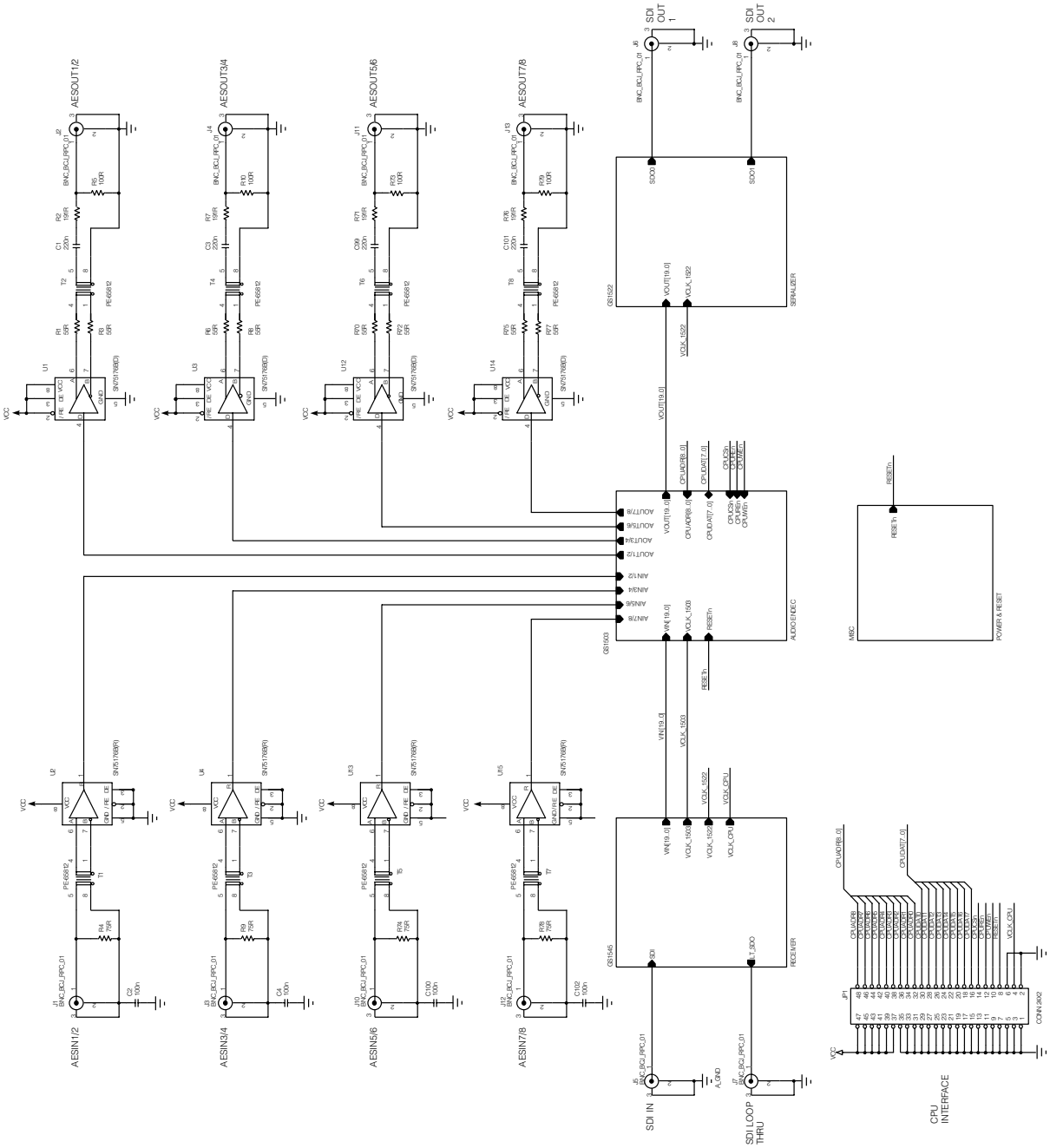
CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
	ADPG4_DEL	Audio group 4 data packet delete. When set HIGH, all audio data packets with group 4 DID will be deleted from the Chroma video data stream. Valid only when "DEL_SEL" is HIGH.	041	7	R/W	0
	ADPG3_DEL	Audio group 3 data packet delete. When set HIGH, all audio data packets with group 3 DID will be deleted from the Chroma video data stream. Valid only when "DEL_SEL" is HIGH.		6	R/W	0
	ADPG2_DEL	Audio group 2 data packet delete. When set HIGH, all audio data packets with group 2 DID will be deleted from the Chroma video data stream. Valid only when "DEL_SEL" is HIGH.		5	R/W	0
	ADPG1_DEL	Audio group 1 data packet delete. When set HIGH, all audio data packets with group 1 DID will be deleted from the Chroma video data stream. Valid only when "DEL_SEL" is HIGH.		4	R/W	0
	ACPG4_DEL	Audio group 4 control packet delete. When set HIGH, all audio control packets with group 4 DID will be deleted from the Luma video data stream. Valid only when "DEL_SEL" is set HIGH. To be fixed.		3	R/W	0
	ACPG3_DEL	Audio group 3 control packet delete. When set HIGH, all audio control packets with group 3 DID will be deleted from the Luma video data stream. Valid only when "DEL_SEL" is HIGH. To be fixed.		2	R/W	0
	ACPG2_DEL	Audio group 2 control packet delete. When set HIGH, all audio control packets with group 2 DID will be deleted from the Luma video data stream. Valid only when "DEL_SEL" is HIGH. To be fixed.		1	R/W	0
	ACPG1_DEL	Audio group 1 control packet delete. When set HIGH, all audio control packets with group 1 DID will be deleted from the Luma video data stream. Valid only when "DEL_SEL" is HIGH. To be fixed.		0	R/W	0
	NDID[7:0]	Arbitrary data packet delete. Designates the DID for the arbitrary data packets to be deleted from the Luma video data stream. Valid only when "DEL_SEL" is HIGH.	042	7-0	R/W	0

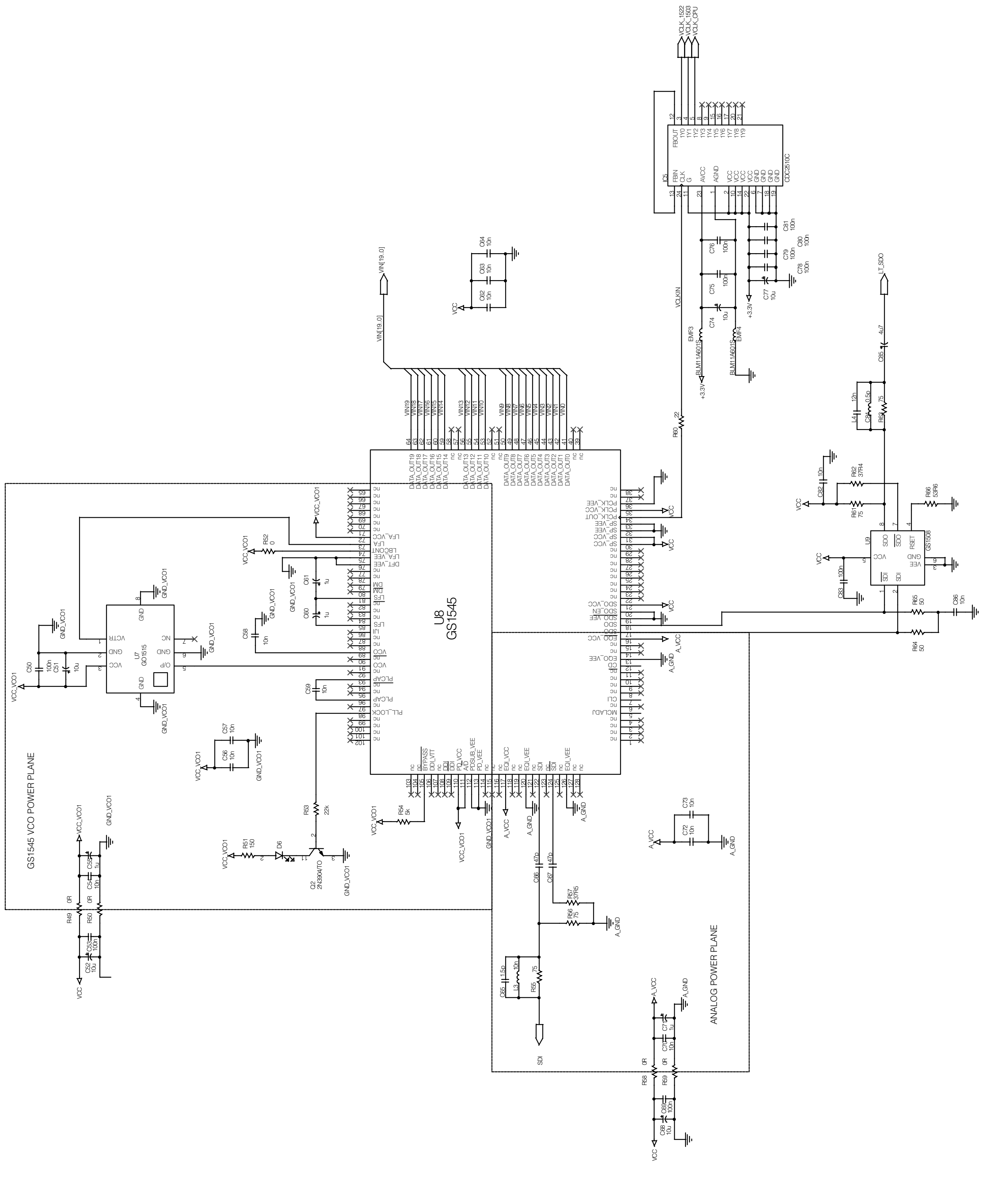
Table 14: Demultiplex Mode Host Interface Registers (Continued)

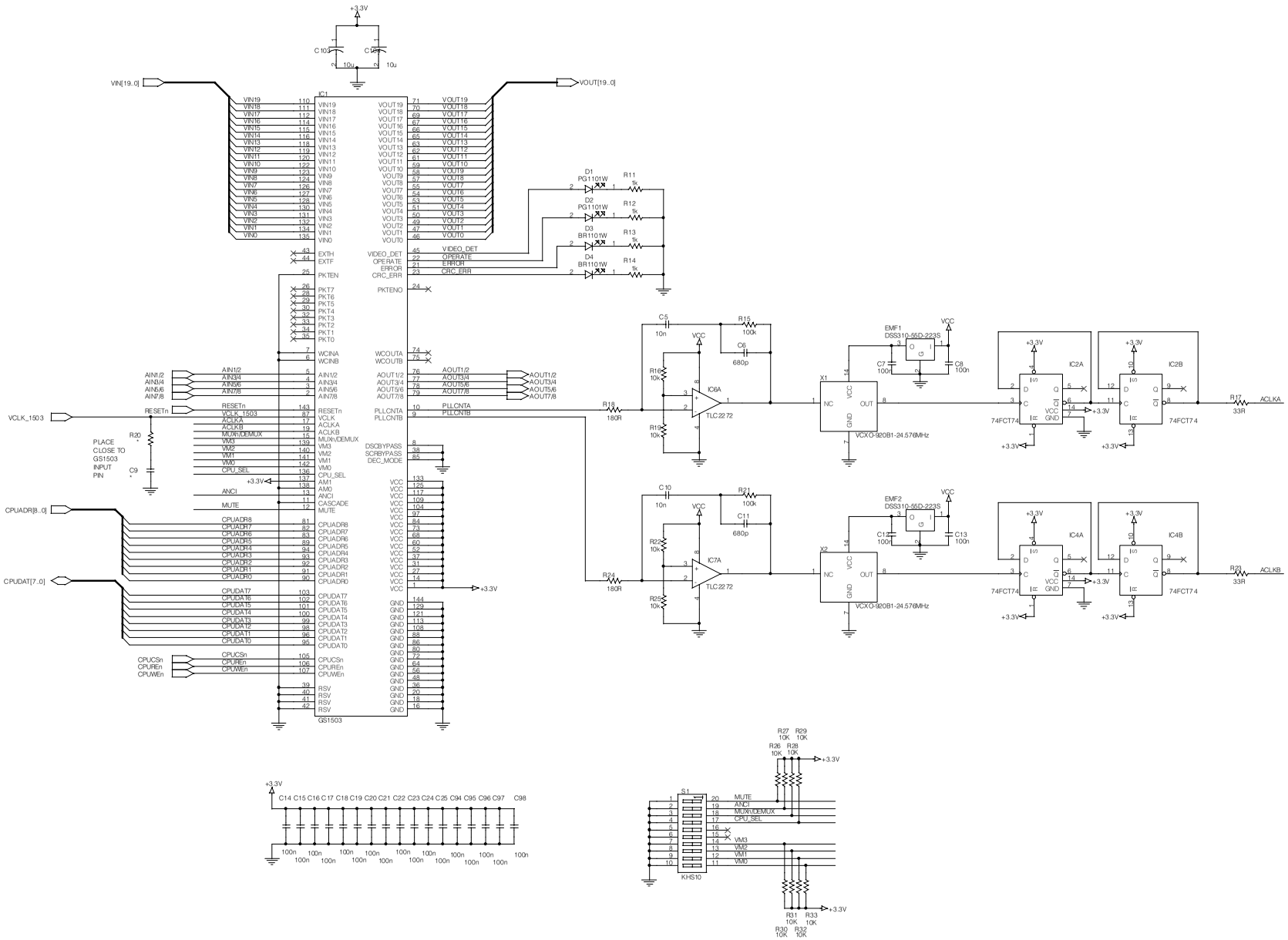
CONTROL ITEM	NAME	DESCRIPTION	ADDRESS	BIT	R/W	DEFAULT
Arbitrary Data Packet	ARBITON	Arbitrary data packet demultiplex. Valid only when "ARBITMODE" is HIGH. When set HIGH, arbitrary data packets will be demultiplexed from the Luma video data stream. Must be set LOW again to access valid data in the "ARBITUDW" registers.	050	1	R/W	0
	ARBITMODE	Arbitrary packet mode select. When set HIGH, arbitrary data packets are demultiplexed and the User Data Words are stored in Host Interface registers 100h to 1FEh. No data will be output on the PKT[7:0] external pins and PTKTEN will be LOW. When set LOW, arbitrary data packets are demultiplexed and output at the PKT[7:0] external pins.		0	R/W	0
	ARBITDID[7:0]	Arbitrary packet Data ID setting. Designates the 8 LSBs of the DID word of the arbitrary data packet to be demultiplexed. The 2 MSBs are internally generated. "ARBITDID[7]" is the MSB and "ARBITDID[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	051	7-0	R/W	0
	ARBITSDID[7:0]	Arbitrary packet Secondary Data ID setting. Designates the 8 LSBs of the secondary DID word of the arbitrary data packet to be demultiplexed. The 2 MSBs are internally generated. "ARBITSDID[7]" is the MSB and "ARBITSDID[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	052	7-0	R/W	0
	ARBITDC[7:0]	Arbitrary packet DC setting. Designates the 8 LSBs of the Data Count word of the arbitrary data packet to be demultiplexed. The 2 MSBs are internally generated. "ARBITDC[7]" is the MSB and "ARBITDC[0]" is the LSB. Valid only when "ARBITMODE" is HIGH.	053	7-0	R/W	0
	ARBITLINEB [12:0]	Field 2 arbitrary packet demultiplex line number setting. Designates the field 2 video line from which the arbitrary data packets will be demultiplexed. Valid only when "ARBITMODE" is HIGH.	054 055	3-0 7-0	R/W	0
	ARBITLINEA [12:0]	Field 1 arbitrary packet demultiplex line number setting. Designates the field 1 video line from which the arbitrary data packets will be demultiplexed. Valid only when "ARBITMODE" is HIGH.	056 057	3-0 7-0	R/W	0
	ARBITUDW0 : ARBITUDW254	Arbitrary packet User Data Word. Designates the 8 LSBs for up to 255 arbitrary packet User Data Words. Arbitrary data can be read from these registers once "ARBITON" has been set HIGH to LOW. Valid only when "ARBITMODE" is HIGH.	100 : 1FE	7-0 : 7-0	R/W	0

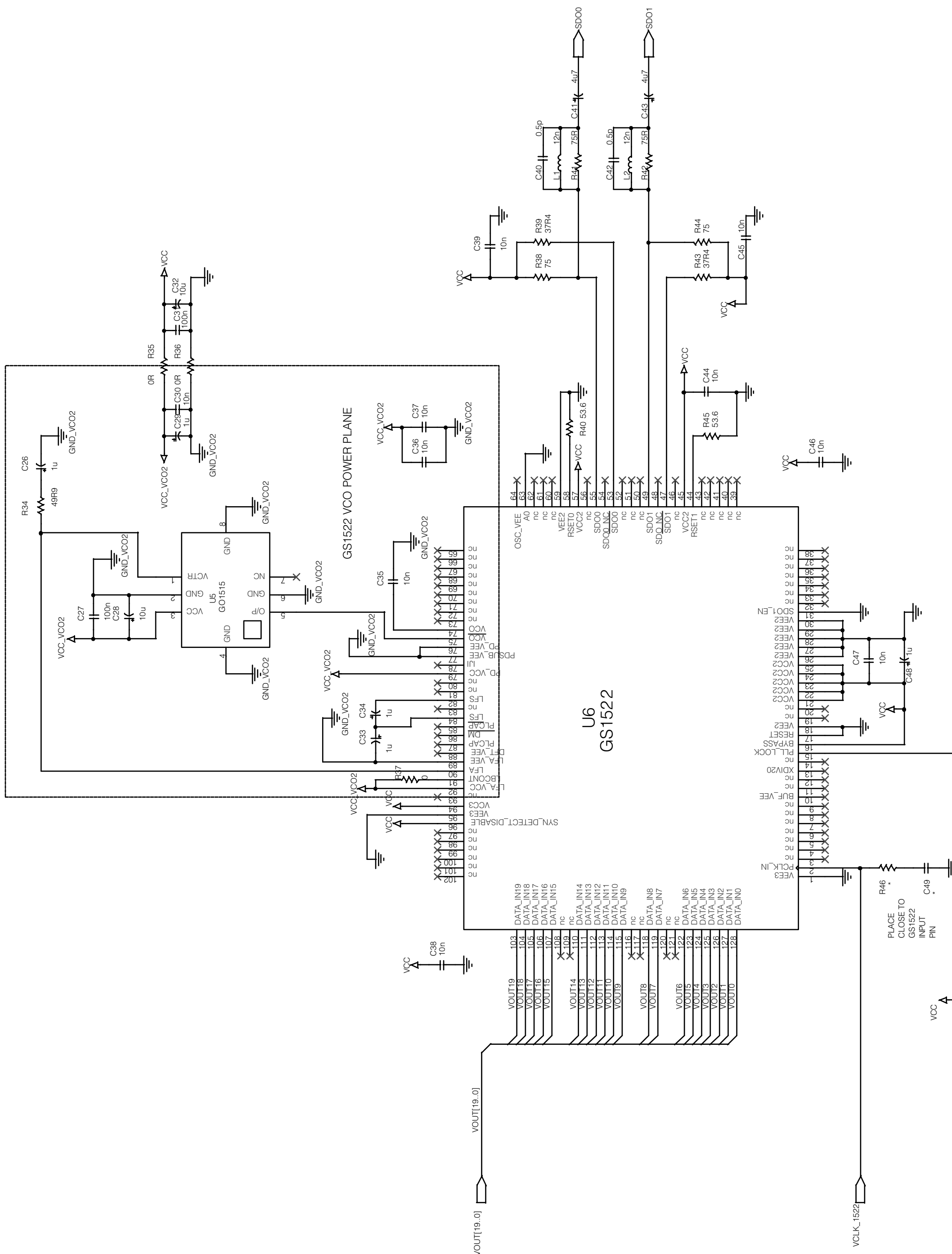
3. REFERENCE DESIGN

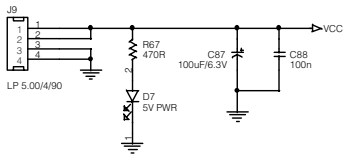
3.1 CIRCUIT SCHEMATICS

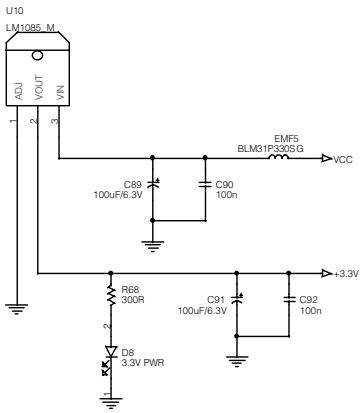


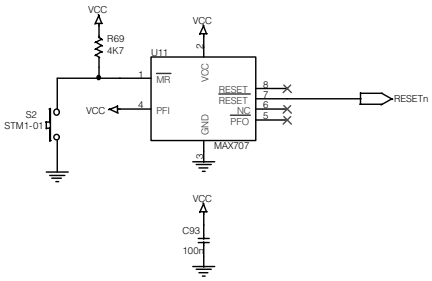

U8
GS1545
GS1545 VCO POWER PLANE
ANALOG POWER PLANE


GS1503
IC1
+3.3V
VIN[19..0]
VOUT[19..0]
VCLK_150:3
RESETn
CPUADR[8..0]
CPUDAT[7..0]
PLACE CLOSE TO GS1503 INPUT PIN
TLC2272
VCXO-920B1-24.576MHz
74FCT74
ACLKA
ACLKB
33R
10K
100n
680p
KHS10

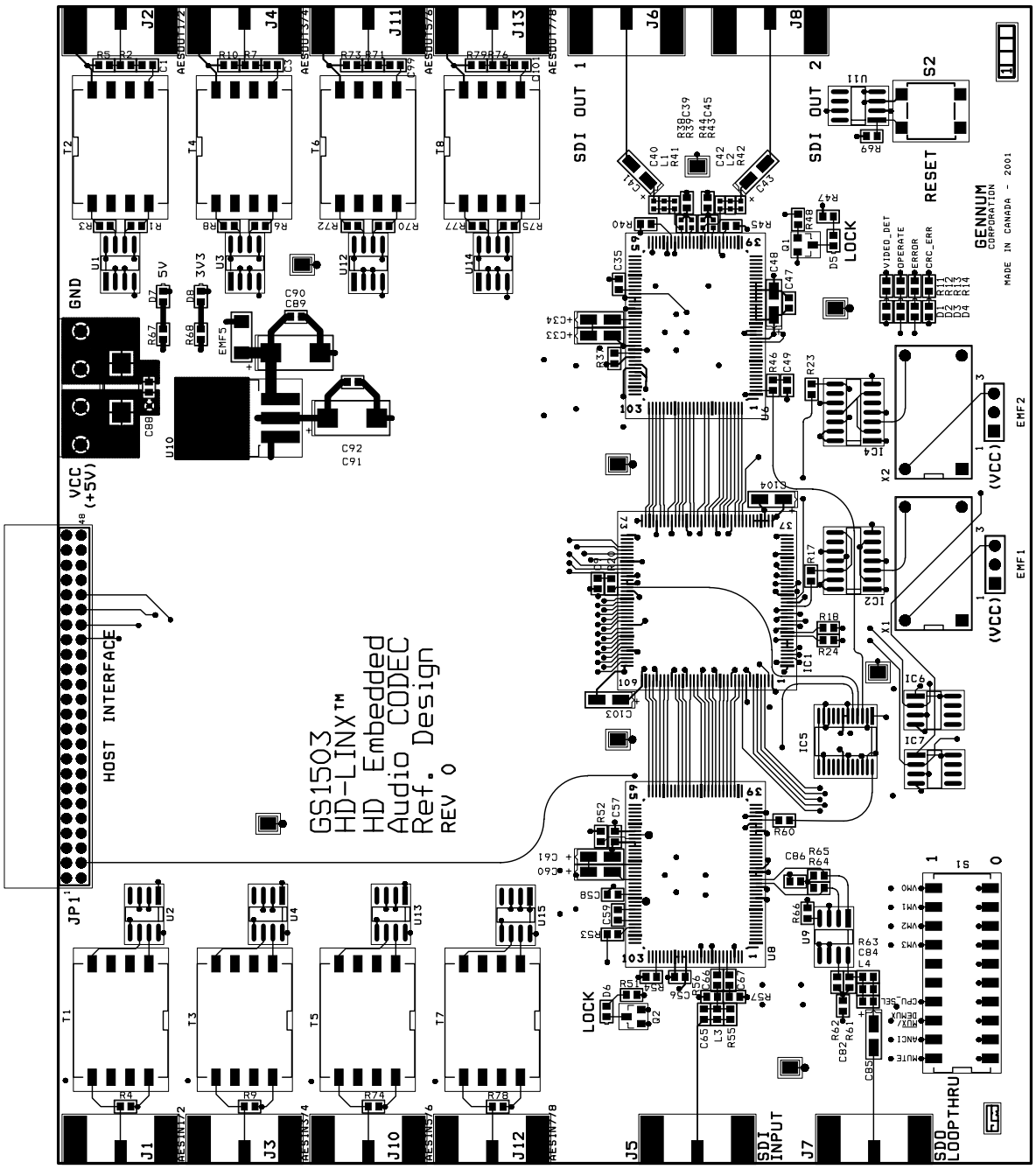

GS1522 VCO POWER PLANE
U6
GS1522
U5
GO1515
VOUT[19..0]
VCLK_1522
SDO0
SDO1
LOCK_DETECT
PLACE CLOSE TO GS1522 INPUT PIN
Q1
2N3904/TO

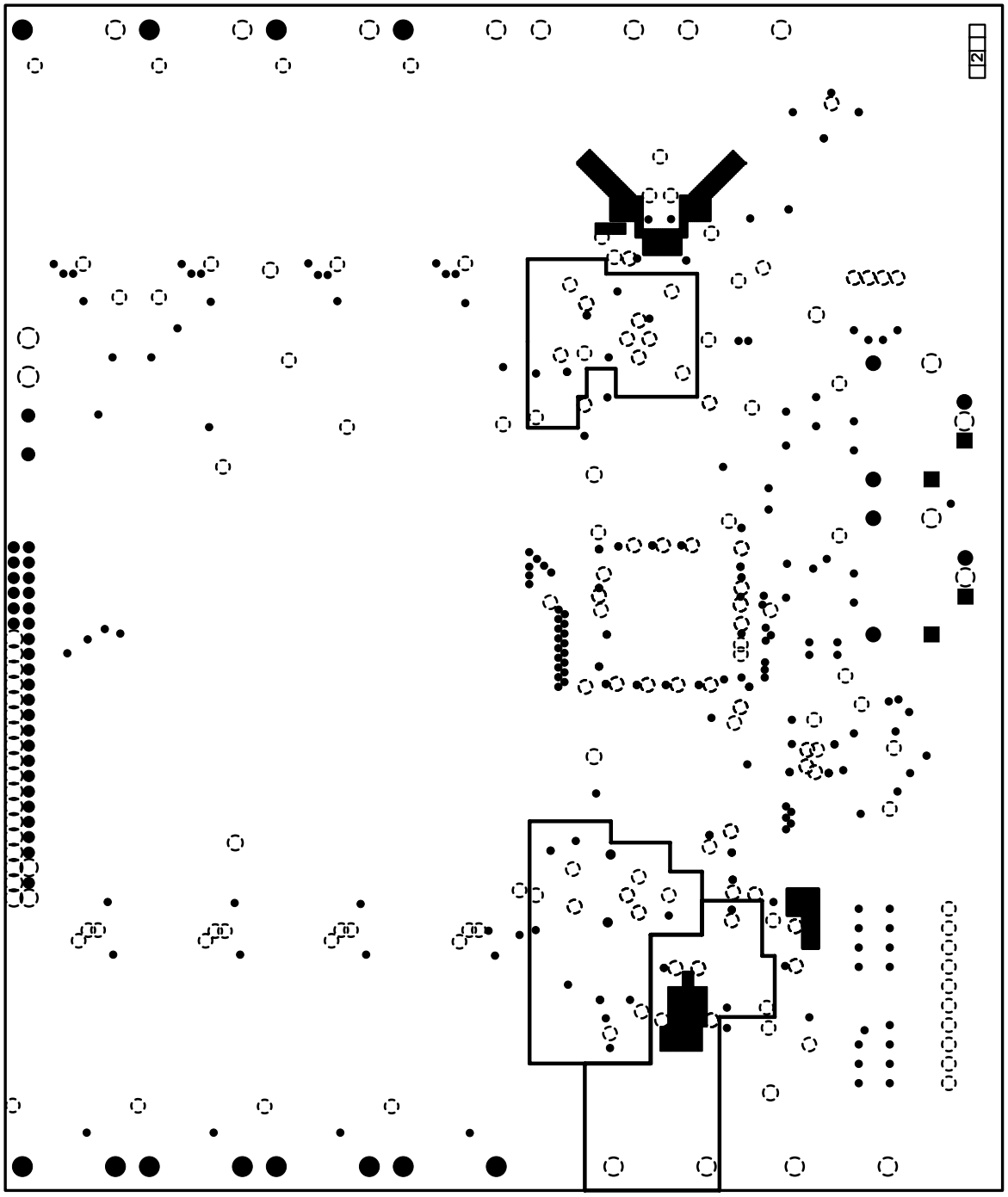

J9
1
2
3
4
LP 5.00/4/90
R67
470R
D7
5V PWR
C87
100uF/6.3V
C88
100n
VCC

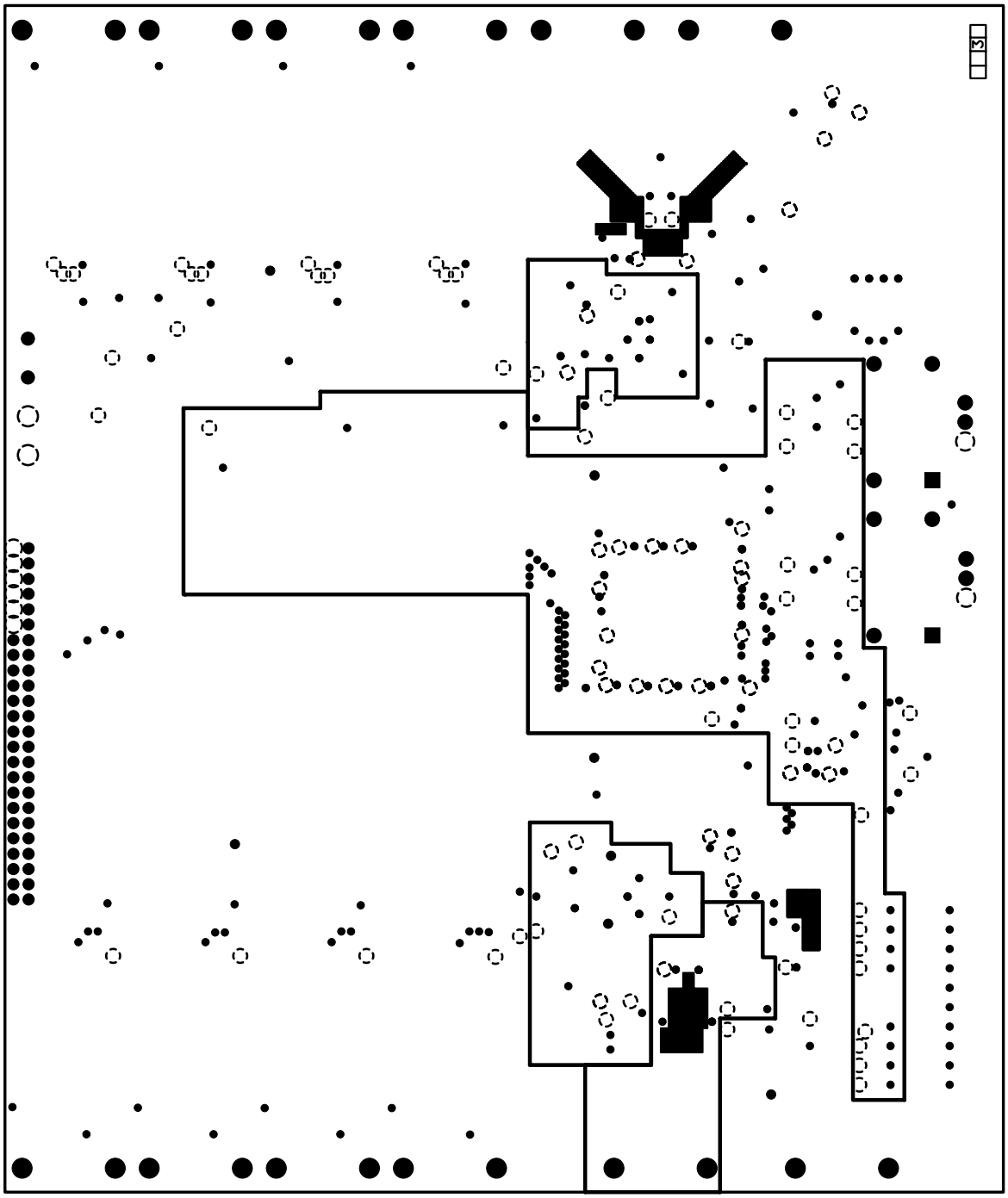

U10
LM1085_M
ADJ
VOUT
VIN
EMF5
BLM31P330SG
VCC
C89
100uF/6.3V
C90
100n
+3.3V
R68
300R
D8
3.3V PWR
C91
100uF/6.3V
C92
100n

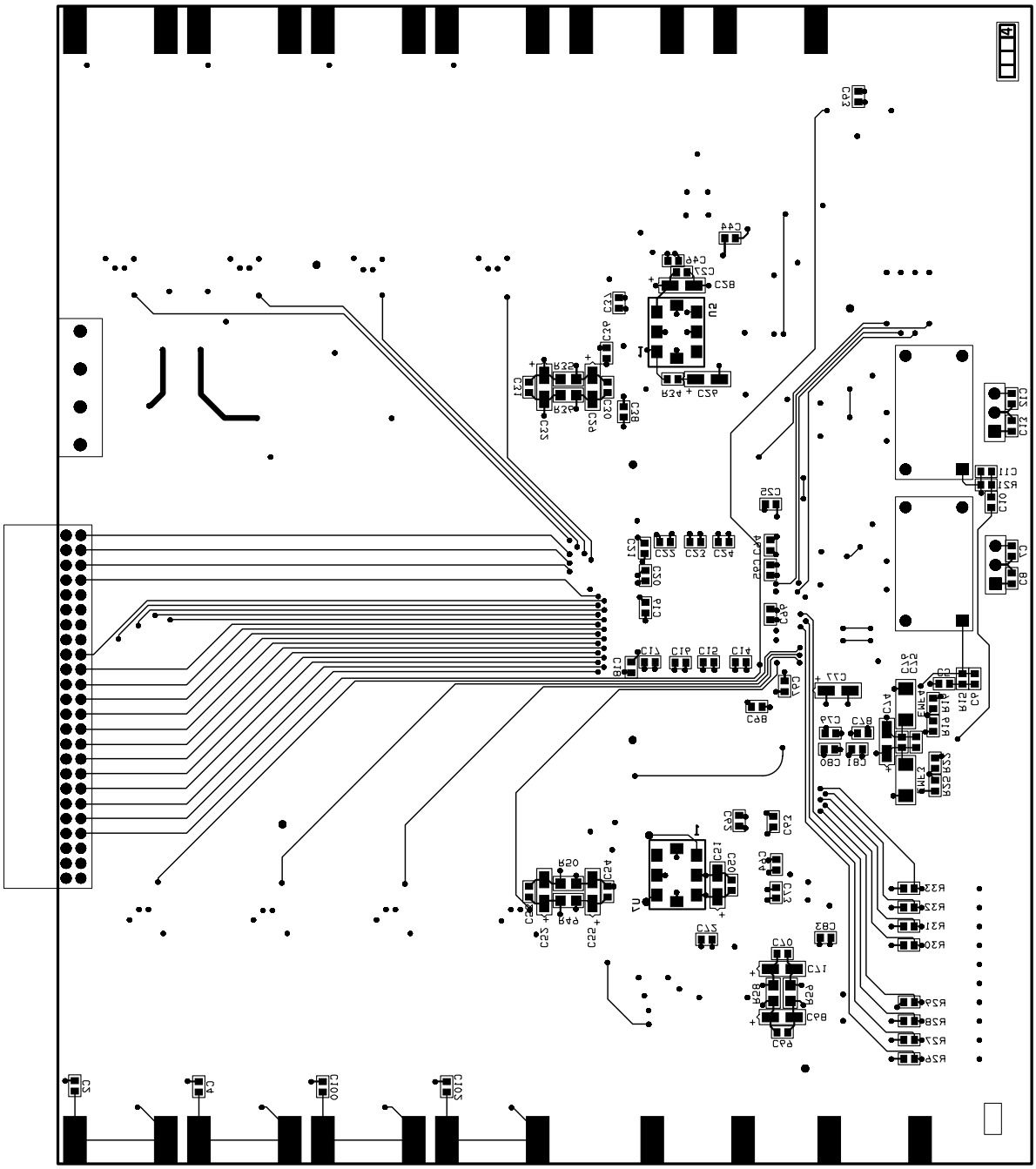

VCC
R69
4K7
S2
STM1-01
U11
MR
PFI
VCC
GND
RESET
RESET
NC
PFO
MAX707
RESETn
C93
100n

3.2 BOARD LAYOUTS









3.3 BILL OF MATERIALS

ITEM	QUANTITY	REFERENCE	PART
1	4	C1,C3,C99,C101	220n
2	41	C2,C4,C7,C8, C12,C13,C14, C15,C16,C17, C18,C19,C20, C21,C22,C23, C24,C25,C27, C31,C50,C53, C69,C75,C76, C78,C79,C80, C81,C83,C88, C90,C92,C93,C94,C95,C96, C97,C98,C100, C102	100n
3	26	L3,C5,C10,C30,C35,C36, C37,C38,C39,C44,C45,C46, C47,C54,C56,C57,C58,C59, C62,C63,C64,C70,C72,C73, C82,C86	10n
4	2	C6,C11	680p
5	4	C9,R20,R46,C49	*
6	9	C26,C29,C33,C34,C48,C55, C60,C61,C71	1u
7	9	C28,C32,C51,C52,C68,C74, C77,C103,C104	10u
8	3	C40,C42,C84	0.5p
9	3	C41,C43,C85	4u7
10	1	C65	1.5p
11	2	C66,C67	47p
12	3	C87,C89,C91	100uF/6.3V
13	4	D1,D2,D3,D4,D5,D6,D7,D8	PG1101W
14	2	EMF1,EMF2	DSS310-55D-223S
15	2	EMF3,EMF4	BLM11A601S
16	1	EMF5	BLM31P330SG
17	1	IC1	GS1503
18	2	IC2,IC4	74FCT74
19	1	IC5	CDC2510C
20	2	IC6,IC7	TLC2272
21	1	JP1	CONN 24X2
22	12	J1,J2,J3,J4,J5,J6,J7,J8, J10,J11,J12,J13	BNC_BCJ_RPC_01
23	1	J9	LP 5.00/4/90
24	3	L1,L2,L4	12n
25	2	Q2,Q1	2N3904/TO
26	8	R1,R3,R6,R8,R70,R72,R75, R77	55R
27	4	R2,R7,R71,R76	191R
28	6	R4,R9,R41,R42,R74,R78	75R
29	4	R5,R10,R73,R79	100R
30	4	R11,R12,R13,R14	1k
31	2	R21,R15	100k

3.3 BILL OF MATERIALS (Continued)

ITEM	QUANTITY	REFERENCE	PART
32	12	R16,R19,R22,R25,R26,R27, R28,R29,R30,R31,R32,R33	10K
33	2	R17,R23	33R
34	2	R24,R18	180R
35	3	R34,R64,R65	49R9
36	8	R35,R36,R37,R49,R50,R52,R58, R59	0R
37	6	R38,R44,R55,R56,R61,R63	75R
38	3	R39,R43,R62	37R4
39	3	R40,R45,R66	53R6
40	1	R47	150R
41	2	R53,R48	22k
42	1	R51	150R
43	1	R54	5k
44	1	R57	37R5
45	1	R60	22R
46	1	R67	470R
47	1	R68	300R
48	1	R69	4K7
49	1	S1	KHS10
50	1	S2	STM1-01
51	8	T1,T2,T3,T4,T5,T6,T7,T8	PE-65812
52	4	U1,U3,U12,U14	SN75176B(D)
53	4	U2,U4,U13,U15	SN75176B(R)
54	2	U7,U5	GO1515
55	1	U6	GS1522
56	1	U8	GS1545
57	1	U9	GS1508
58	1	U10	LM1085_M
59	1	U11	MAX707
60	2	X2,X1	VCXO-920B1-24.576MHz

NOTE: This design is recommended for reference only. The AES/EBU inputs do not utilize equalization; therefore cable length performance may be limited. For improved AES/EBU input and output performance, it is recommended that examples in the AES-3id-2001 standard Annex B are consulted. This standard includes alternative schematics for both input and output networks for 75Ω coaxial cable transmission. For the transmission of AES/EBU over balanced 110Ω twisted pair cable, using XLR type connectors, please consult the AES3-1992 standard

4. REFERENCES & BIBLIOGRAPHY

SMPTE 260M-1999 1125/60 High-Definition Production System - Digital Representation and Bit-Parallel Interface

SMPTE 274M-1998 1920 x 1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates

SMPTE 291M-1998 Ancillary Data Packet and Space Formatting

SMPTE 292M-1998 Bit-Serial Digital Interface for High-Definition Television Systems

SMPTE 295M-1997 1920 x 1080 50 Hz - Scanning and Interfaces

SMPTE 296M- 2001 1280 x 720 Scanning, Analog and Digital Representation and Analog Interface

SMPTE 299M-1997 24-Bit Digital Audio Format for HDTV Bit-Serial Interface

SMPTE RP211-2000 Implementation of 24P, 25P and 30P Segmented Frames for 1920 x 1080 Production Format

AES3-1992 (ANSI S4.40-1992) AES Recommended practice for digital audio engineering - Serial transmission format for two-channel linearly represented digital audio data

AES-3id-2001 AES information document for digital audio engineering - Transmission of AES3 formatted data by unbalanced coaxial cable

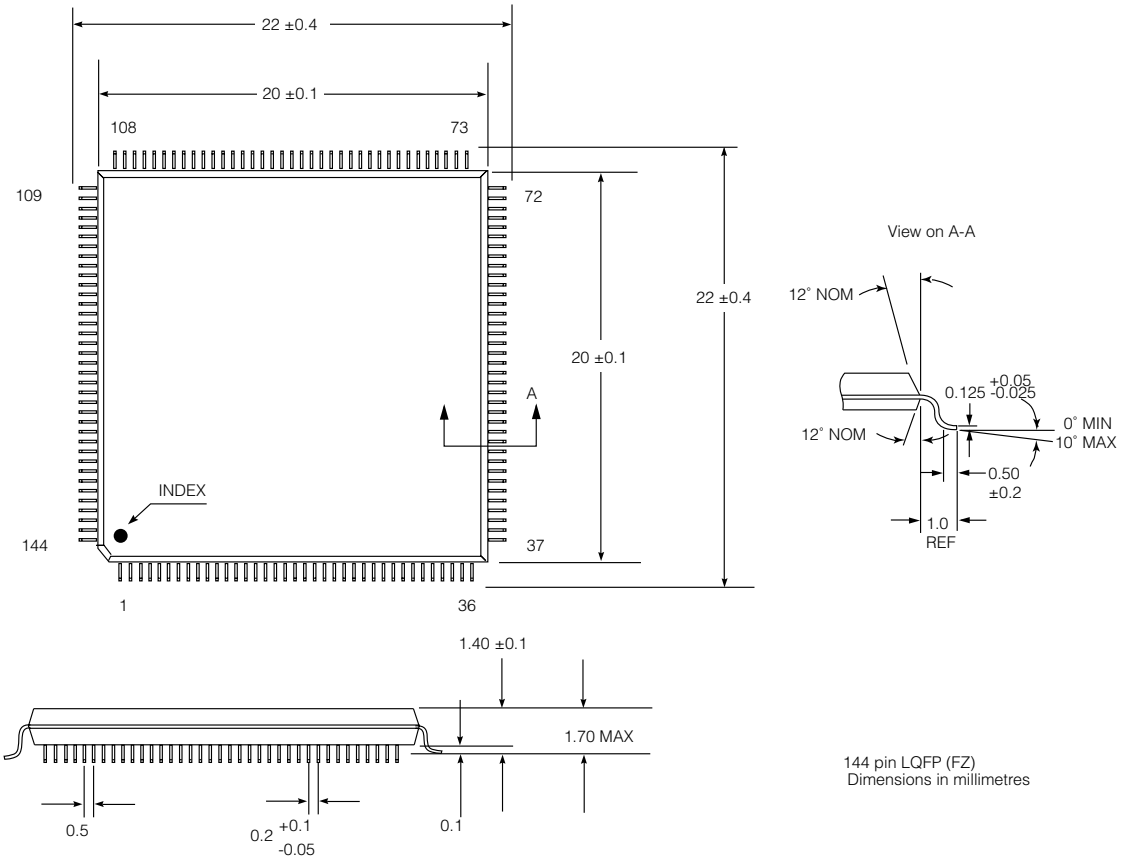
EBU Tech. 3250-E Specification of the Digital Audio Interface (The AES/EBU Interface) (Second Edition 1992)

Society of Motion Picture and Television Engineers: http://www.smpte.org

Audio Engineering Society: http://www.aes.org

European Broadcast Union: http://www.ebu.ch

PACKAGING INFORMATION



144 pin LQFP (FZ)
Dimensions in millimetres

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REVISION NOTES:

Updated to AC & DC tables and doucment info.

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