GS9062
Serial Digital Serializer

PRODUCT BRIEF

FEATURES

- compliant with SMPTE 259M-C
- small footprint compatible with GS1560, GS1532, GS9060
- DVB-ASI support including 8b/10b coding and sync word insertion
- operation at 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s
- SMPTE 292M and SMPTE 259M compliant scrambling and -> NRZI coding (with bypass)
- CRC calculation and insertion
- line number calculation and insertion
- TRS calculation and insertion
- illegal code re-mapping
- 20 bit / 10 bit CMOS parallel input data bus
- TTL compatible PCLK input
- 148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital input
- EDH generation and insertion
- 1.8V core power supply and 3.3V charge pump power supply
- 3.3V digital I/O supply
- JTAG test interface
- low power operation (estimate <425mW)

APPLICATIONS

- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

AVAILABLE PACKAGING

80-pin LQFP

DESCRIPTION

The GS9062 is a dual rate serializer, compliant with SMPTE 259M-C. This device features a fully compliant cable driver output. When used in conjunction with the GO1525 voltage controlled oscillator, a transmit solution can be realized.

In addition to providing robust parallel to serial conversion, the GS9062 includes a range of additional data processing functions such as TRS, line number, and CRC insertion, DVB-ASI and EDH support.

The GS9062 performs the functions of parallel to serial conversion, scrambling as per 259M and NRZ to NRZI conversion. The SMPTE scrambler may optionally be bypassed to support the transmission of other coding schemes.

In addition, the device can insert TRS signals, calculate / insert line numbers and CRC's, re-map illegal code words and insert SMPTE 352M payload identifier packets if programmed by the host interface.

The GS9062 may also be used in data pass-through mode where no processing of the data is performed.

All of the processing features are optional and may be enabled/disabled via external control pin(s) and / or host interface programming.

Parallel data inputs are provided in both 10 bit multiplexed and 20 bit de-multiplexed format. An associated parallel clock input signal is provided operating at 27MHz (10 bit multiplexed input) and 13.5MHz (20 bit de-multiplexed input).

The integrated SMPTE 259M-C cable driver features an output mute on loss of signal, high impedance mode, adjustable signal swing.

The device may be configured for DVB-ASI operation where it will insert K28.5 sync words and 8b/10b encode the data stream prior to transmission.

Generation and insertion of EDH AP / FF CRC's and EDH error flags is also supported by the device.

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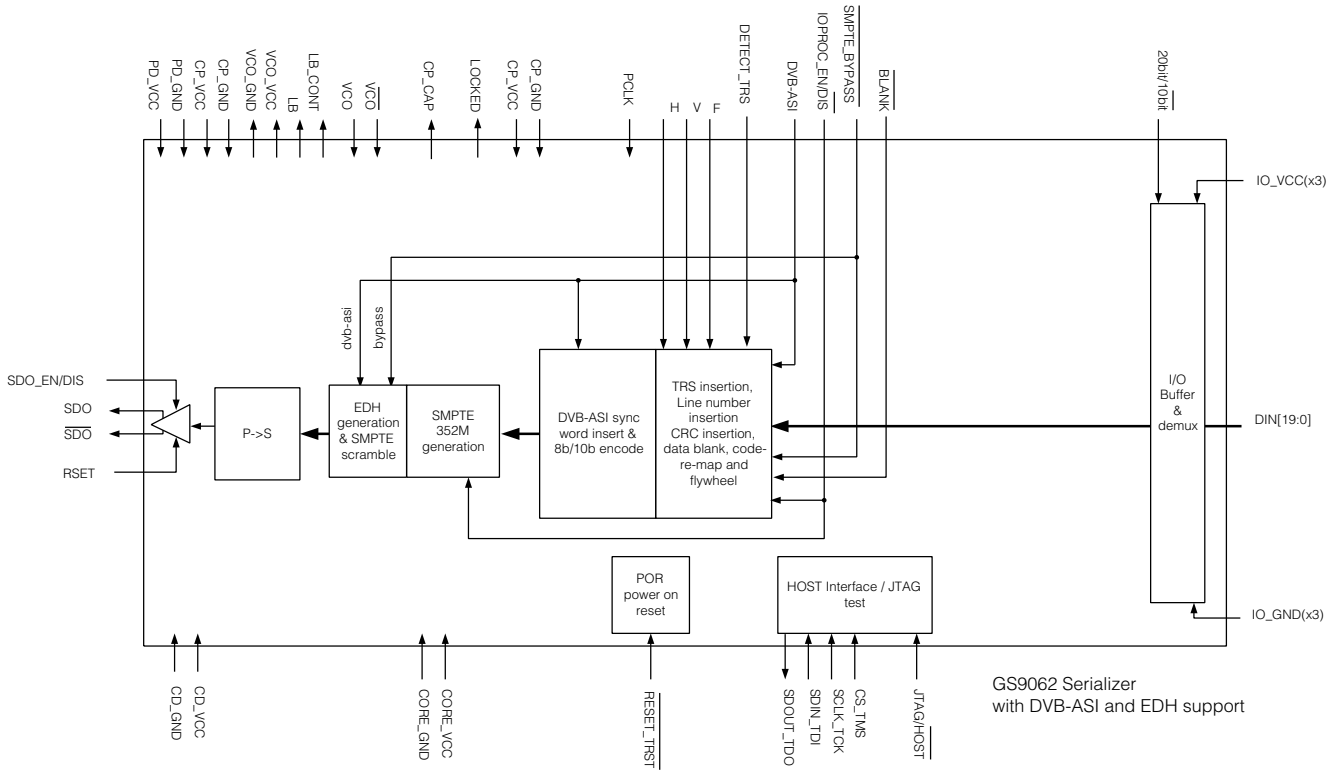

GS9062 Serializer
with DVB-ASI and EDH support

GS9062 FUNCTIONAL BLOCK DIAGRAM

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
PRODUCT BRIEF

REVISION NOTES:
New Document.

GENNUM CORPORATION

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