1.8 Volt Intel® Wireless Flash Memory

28F320W18, 28F640W18, 28F128W18

Datasheet

Product Features

- **High Performance Read-While-Write/ Erase**
  - —Burst frequency at 66 MHz with zero Wait state
  - —60 ns Initial Access Read Speed
  - —11 ns Burst-Mode Read Speed
  - —20 ns Page-Mode Read Speed
  - —4-, 8-, 16-, and Continuous-Word Burst Mode Reads
  - —Burst and Page Mode Reads in all Blocks
  - —Burst Suspend Feature
  - —Enhanced Factory Programming at 3.1 µs/word (typ.)
- Security
  - —128-bit Protection Register
  - —64-bits Unique Programmed by Intel
  - —64-bits User-Programmable
  - —Absolute “Code + Data” protection with V_{PP} = 0.0 V
  - —Individual and Instantaneous Block Locking with Lock-Down Capability
- Quality and Reliability
  - —Temperature Range: –40 °C to +85 °C
  - —100k Erase Cycles per Block
  - —0.13 µm ETOX™ VIII Process
- Architecture
  - —Multiple Partitions, Dual Operation
  - —4Mbit per Partition
  - —Read-While-Write or Read-While-Erase
  - —8KB parameter blocks
  - —64KB main blocks
  - —Top or Bottom Boot Devices
  - —16-bit wide data bus
- Software
  - —5 µs (typ.) Program and Erase Suspend Latency Time
  - —Flash Data Integrator (FDI) and Common Flash Interface (CFI) Compatible
  - —Programmable WAIT Signal Polarity
- Packaging and Power
  - —32-, 64-, and 128-Mbit in a VF BGA package
  - —V_{CC} = 1.70 V to 1.95 V
  - —V_{CCQ} = 1.70 V to 2.24 V or 1.35 V to 1.70 V
  - —Standby current: 5 µA (typ.)
  - —Read current: 7mA (typ.)

The 1.8 Volt Intel Wireless Flash memory with flexible multi-partition dual operation, provides high-performance asynchronous and synchronous burst reads. It is an ideal memory for low-voltage burst CPUs. Combining high read performance with flash memory’s intrinsic non-volatility, 1.8 Volt Intel Wireless Flash memory eliminates the traditional system-performance paradigm of shadowing redundant code memory from slow nonvolatile storage to faster execution memory. It reduces the total memory requirement that increases reliability and reduces overall system power consumption and cost.

The 1.8 Volt Intel Wireless Flash memory’s flexible multi-partition architecture allows programming or erasing to occur in one partition while reading from another partition. This allows for higher data write throughput compared to single partition architectures. The dual-operation architecture also allows two processors to interleave code operations while program and erase operations take place in the background. The designer can also choose the size of the code and data partitions via the flexible multi-partition architecture.

Notice: This document contains information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

290701-004
April 2002

Contents

Revision History

Date of Revision	Version	Description
09/13/00	290701-001	Original Version

Date of Revision	Version	Description
01/29/01	290701-002	Deleted 16-Mbit density Revised *ADV#,* Section 2.2 Revised *Protection Registers*, Section 4.16 Revised *Program Protection Register*, Section 4.18 Revised Example in *First Access Latency Count*, Section 5.0.2 Revised Figure 5, *Data Output with LC Setting at Code 3* Added *WAIT Signal Function*, Section 5.0.3 Revised *WAIT Signal Polarity*, Section 5.0.4 Revised *Data Output Configuration*, Section 5.0.5 Added Figure 7, *Data Output Configuration with WAIT Signal Delay* Revised *WAIT Delay Configuration*, Section 5.0.6 Changed V_{CCQ} Spec from 1.7 V – 1.95 V to 1.7 V – 2.24 V in Section 8.2, *Extended Temperature Operation* Changed I_{CCS} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed I_{CCR} Spec from 10 mA (CLK = 40 MHz, burst length = 4) and 13 mA (CLK = 52 MHz, burst length = 4) to 13 mA, and 16 mA respectively in Section 8.4, *DC Characteristics* Changed I_{CCWS} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed I_{CCES} Spec from 15 µA to 18 µA in Section 8.4, *DC Characteristics* Changed t_{CHQX} Spec from 5ns to 3ns in Section 8.6, *AC Read Characteristics* Added Figure 25, WAIT Signal in Synchronous Non-Read Array Operation Waveform Added Figure 26, *WAIT Signal in Asynchronous Page Mode Read Operation Waveform* Added Figure 27, *WAIT Signal in Asynchronous Single Word Read Operation Waveform* Revised Appendix E, *Ordering Information*
06/12/01	290701-003	Revised entire Section 4.10, *Enhanced Factory Program Command (EFP)* and Figure 6, *Enhanced Factory Program Flowchart* Revised Section 4.13, *Protection Register* Revised Section 4.15, *Program Protection Register* Revised Section 7.3, *Capacitance,* to include 128-Mbit specs Revised Section 7.4, *DC Characteristics,* to include 128-Mbit specs Revised Section 7.6, *AC Read Characteristics,* to include 128-Mbit device specifications Added t_{VHGL} Spec in Section 7.6, *AC Read Characteristics* Revised Section 7.7, *AC Write Characteristics*, to include 128-Mbit device specifications Minor text edits

Date of Revision	Version	Description
04/05/02	290701-004	New Sections Organization Added 16 Word Burst Feature Added Burst Suspend Section Revised Block Locking State Diagram Revised Active Power Section Revised Automatic Power Savings Section Revised Power-Up/Down Operation Section Revised Extended Temperature Operation Added 128Mb DC Characteristics Table Added 128 Mb AC Read Characteristics Revised Table 17. Test Configuration Component Values for Worst Case Speed Conditions Added .13 µ Product DC and AC Read Characteristics Revised AC Write Characteristics Added Read to Write and Write to Read Transition Waveforms Revised Reset Specifications Various text edits

1.0 Introduction

1.1 Document Purpose

This datasheet contains information about the 1.8 Volt Intel® Wireless Flash memory family. Section 1.0 provides a flash memory overview. Section 2.0 through Section 9.0 describe the memory functionality. Section 10.0 describes the electrical specifications for extended temperature product offerings. Packaging specifications and order information can be found in Appendix C and Appendix D, respectively.

1.2 Nomenclature

Many acronyms that describe product features or usage are defined here:

- **APS**Automatic Power Savings
- **BBA** Block Base Address
- **CFI** Common Flash Interface
- **CUI** Command User Interface
- **EFP** Enhanced Factory Programming
- **FDI** Flash Data Integrator
- **NC**No Connect
- **OTP** One-Time Programmable
- **PBA** Partition Base Address
- **RWE** Read-While-Erase
- **RWW**Read-While-Write
- **SRD**Status Register Data
- **VF BGA**Very thin, Fine pitch, Ball Grid Array
- **WSM**Write State Machine

1.3 Conventions

Many abbreviated terms and phrases are used throughout this document:

- The term “1.8 V” refers to the full VCC voltage range of 1.7 V – 1.95 V (except where noted) and “V_{PP} = 12 V” refers to 12 V ±5%.
- When referring to registers, the term **set** means the bit is a logical 1, and **clear** means the bit is a logical 0.
- The terms **pin** and **signal** are often used interchangeably to refer to the external signal connections on the package. (*ball* is the term used for VF BGA).
- A **word** is 2 bytes, or 16 bits.

- **Signal** names are in all CAPS (see Section 2.3, “Signal Descriptions” on page 13.)
- **Voltage** applied to the signal is subscripted, for example, V_{PP}.

Throughout this document, references are made to top, bottom, parameter, and partition. To clarify these references, the following conventions have been adopted:

- A **block** is a group of bits (or words) that erase simultaneously with one block erase instruction.
- A **main block** contains 32 Kwords.
- A **parameter block** contains 4 Kwords.
- The **Block Base Address** (BBA) is the first address of a block.
- A **partition** is a group of blocks that share erase and program circuitry and a common status register.
- The **Partition Base Address** (PBA) is the first address of a partition. For example, on a 32-Mbit top-parameter device, partition number 5 has a PBA of 140000h.
- The **top partition** is located at the highest physical device address. This partition may be a main partition or a parameter partition.
- The **bottom partition** is located at the lowest physical device address. This partition may be a main partition or a parameter partition.
- A **main partition** contains only main blocks.
- A **parameter partition** contains a mixture of main blocks and parameter blocks.
- A **top parameter device** (**TPD**) has the parameter partition at the top of the memory map with the parameter blocks at the top of that partition. This was formerly referred to as top-boot device.
- A **bottom parameter device** (**BPD**) has the parameter partition at the bottom of the memory map with the parameter blocks at the bottom of that partition. This was formerly referred to as bottom-boot block flash device.

2.0 Device Description

This section provides an overview of the 1.8 Volt Intel Wireless Flash memory features, packaging, signal naming, and device architecture.

2.1 Product Overview

The 1.8 Volt Intel Wireless Flash memory provides Read-While-Write (RWW) and Read-White-Erase (RWE) capability with high-performance synchronous and asynchronous reads on package-compatible densities with a 16-bit data bus. Individually-erasable memory blocks are optimally sized for code and data storage. Eight 4-Kword parameter blocks are located in the parameter partition at either the top or bottom of the memory map. The rest of the memory array is grouped into 32-Kword main blocks.

The memory architecture for the 1.8 Volt Intel Wireless Flash memory consists of multiple 4-Mbit partitions, the exact number depending on device density. By dividing the memory array into partitions, program or erase operations can take place simultaneously during read operations. Burst reads can traverse partition boundaries, but user application code is responsible for ensuring that they don't extend into a partition that is actively programming or erasing. Although each partition has burst-read, write, and erase capabilities, simultaneous operation is limited to write or erase in one partition while other partitions are in a read mode.

Augmented erase-suspend functionality further enhances the RWW capabilities of this device. An erase can be suspended to perform a program or read operation within any block, except that which is erase-suspended. A program operation nested within a suspended erase can subsequently be suspended to read yet another memory location.

After device power-up or reset, the 1.8 Volt Intel Wireless Flash memory defaults to asynchronous read configuration. Writing to the device's configuration register enables synchronous burst-mode read operation. In synchronous mode, the CLK input increments an internal burst address generator. CLK also synchronizes the flash memory with the host CPU and outputs data on every, or on every other, valid CLK cycle after an initial latency. A programmable WAIT output signals to the CPU when data from the flash memory device is ready.

In addition to its improved architecture and interface, the 1.8 Volt Intel Wireless Flash memory incorporates Enhanced Factory Programming (EFP), a feature that enables fast programming and low-power designs. The EFP feature provides the fastest currently-available program performance, which can increase a factory's manufacturing throughput.

The device supports read operations at 1.8 V and erase and program operations at 1.8 V or 12 V. With the 1.8-V option, VCC and VPP can be tied together for a simple, ultra-low-power design. In addition to voltage flexibility, the dedicated VPP input provides complete data protection when $V_{PP} \leq V_{PPLK}$.

This device allows I/O operation at voltages even lower than the minimum V_{CCQ} of 1.7 V. This Extended V_{CCQ} range, 1.35 V – 1.8 V, permits even greater system design flexibility.

A 128-bit protection register enhances the user's ability to implement new security techniques and data protection schemes. Unique flash device identification and fraud-, cloning-, or content-protection schemes are possible through a combination of factory-programmed and user-OTP data cells. Zero-latency locking/unlocking on any memory block provides instant and complete protection for critical system code and data. An additional block lock-down capability provides hardware protection where software commands alone cannot change the block's protection status.

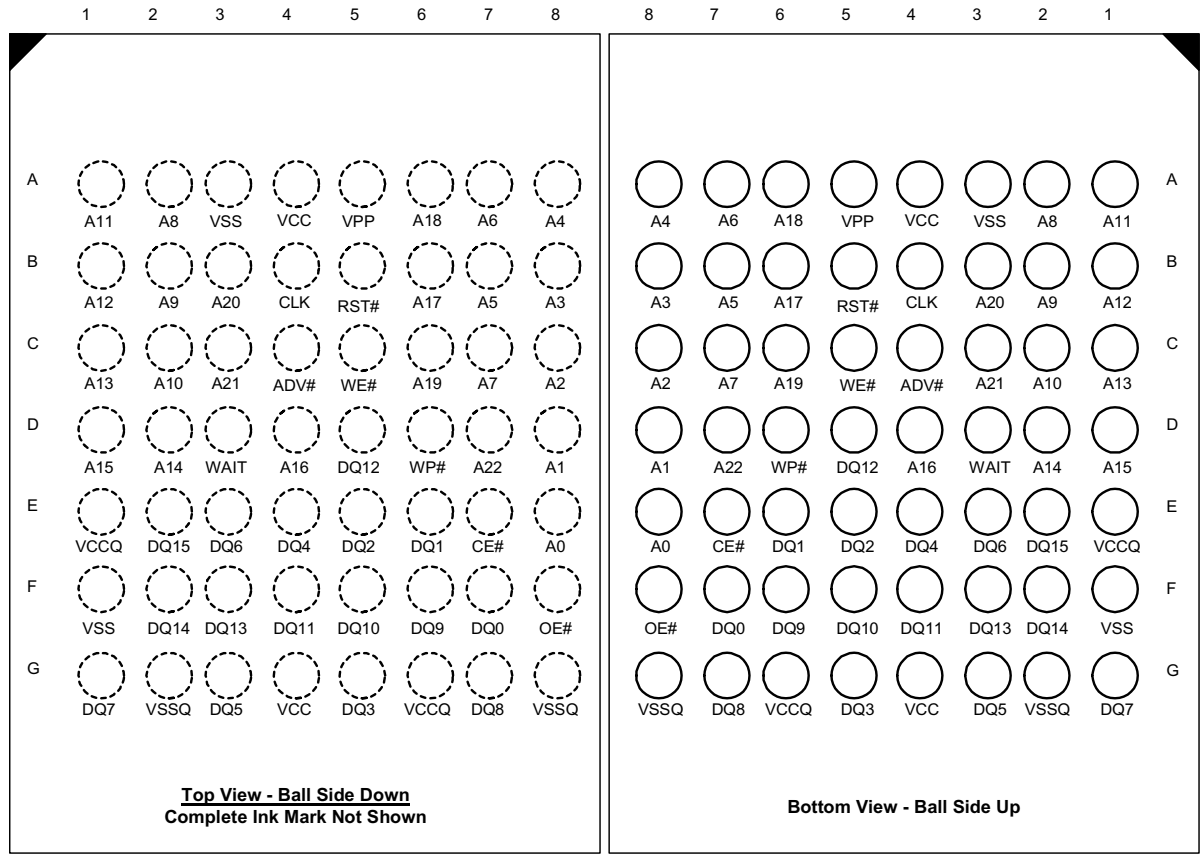
The device's Command User Interface (CUI) is the system processor's link to internal flash memory operation. A valid command sequence written to the CUI initiates device Write State Machine (WSM) operation that automatically executes the algorithms, timings, and verifications necessary to manage flash memory program and erase. An internal status register provides ready/busy indication results of the operation (success, fail, and so on).

Three power-saving features– Automatic Power Savings (APS), standby, and RST#– can significantly reduce power consumption. The device automatically enters APS mode following read cycle completion. Standby mode begins when the system deselects the flash memory by de-asserting CE#. Driving RST# low produces power savings similar to standby mode. It also resets the part to read-array mode (important for system-level reset), clears internal status registers, and provides an additional level of flash write protection.

2.2 Package Diagram

The 1.8 Volt Intel® Wireless Flash memory is available in a 56 active-ball matrix VF BGA Chip Scale Package with 0.75 mm ball pitch that is ideal for board-constrained applications. Figure 1 shows device ballout.

Figure 1. 56 Active-Ball Matrix, VF BGA Package



NOTES:
1. On lower density devices, upper address balls can be treated as NC. (Example: For 32-Mbit density, A21 and A22 will be NC).
2. See Appendix C, “Mechanical Specifications” on page 92 for mechanical specifications for the package.

2.3 Signal Descriptions

Table 1 describes ball usage.

Table 1. Signal Descriptions

Symbol	Type	Name and Function
A[22:0]	I	**ADDRESS INPUTS:** For memory addresses. 32 Mbit: A[20:0]; 64 Mbit: A[21:0]; 128 Mbit: A[22:0]
D[15:0]	I/O	**DATA INPUTS/OUTPUTS:** Inputs data and commands during write cycles; outputs data during memory, status register, protection register, and configuration code reads. Data pins float when the chip or outputs are deselected. Data is internally latched during writes.
ADV#	I	**ADDRESS VALID:** ADV# indicates valid address presence on address inputs. During synchronous read operations, all addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
CE#	I	**CHIP ENABLE:** Asserting CE# activates internal control logic, I/O buffers, decoders, and sense amps. De-asserting CE# deselects the device, places it in standby mode, and tri-states all outputs.
CLK	I	**CLOCK:** CLK synchronizes the device to the system bus frequency during synchronous reads and increments an internal address generator. During synchronous read operations, addresses are latched on ADV#'s rising edge or CLK's rising (or falling) edge, whichever occurs first.
OE#	I	**OUTPUT ENABLE:** When asserted, OE# enables the device's output data buffers during a read cycle. When OE# is deasserted, data outputs are placed in a high-impedance state.
RST#	I	**RESET:** When low, RST# resets internal automation and inhibits write operations. This provides data protection during power transitions. de-asserting RST# enables normal operation and places the device in asynchronous read-array mode.
WAIT	O	**WAIT:** The WAIT signal indicates valid data during synchronous read modes. It can be configured to be asserted-high or asserted-low based on bit 10 of the Configuration Register. WAIT is tri-stated if CE# is deasserted. WAIT is not gated by OE#.
WE#	I	**WRITE ENABLE:** WE# controls writes to the CUI and array. Addresses and data are latched on the rising edge of WE#.
WP#	I	**WRITE PROTECT:** Disables/enables the lock-down function. When WP# is asserted, the lock-down mechanism is enabled and blocks marked lock-down cannot be unlocked through software. See Section 7.1, "Block Lock Operations" on page 38 for details on block locking.
VPP	Pwr/I	**ERASE AND PROGRAM POWER:** A valid voltage on this pin allows erasing or programming. Memory contents cannot be altered when $V_{PP} \le V_{PPLK}$. Block erase and program at invalid V_{PP} voltages should not be attempted. Set $V_{PP} = V_{CC}$ for in-system program and erase operations. To accommodate resistor or diode drops from the system supply, the V_{IH} level of V_{PP} can be as low as V_{PP1} min. V_{PP} must remain above V_{PP1} min to perform in-system flash modification. VPP may be 0 V during read operations. V_{PP2} can be applied to main blocks for 1000 cycles maximum and to parameter blocks for 2500 cycles. VPP can be connected to 12 V for a cumulative total not to exceed 80 hours. Extended use of this pin at 12 V may reduce block cycling capability.
VCC	Pwr	**DEVICE POWER SUPPLY:** Writes are inhibited at $V_{CC} \le V_{LKO}$. Device operations at invalid V_{CC} voltages should not be attempted.
VCCQ	Pwr	**OUTPUT POWER SUPPLY:** Enables all outputs to be driven at V_{CCQ}. This input may be tied directly to VCC.
VSS	Pwr	**GROUND:** Pins for all internal device circuitry must be connected to system ground.
VSSQ	Pwr	**OUTPUT GROUND**: Provides ground to all outputs which are driven by VCCQ. This signal may be tied directly to VSS.
DU		**DON'T USE:** Do not use this pin. This pin should not be connected to any power supplies, signals or other pins and must be floated.
NC		**NO CONNECT:** No internal connection; can be driven or floated.

2.4 Memory Map and Partitioning

The 1.8 Volt Intel Wireless Flash memory is divided into 4-Mbit physical partitions, which allows simultaneous RWW or RWE operations and allows users to segment code and data areas on 4-Mbit boundaries. The device's memory array is asymmetrically blocked, which enables system code and data integration within a single flash device. Each block can be erased independently in block erase mode. Simultaneous program and erase operations are not allowed; only one partition at a time can be actively programming or erasing. See Table 2, "Bottom Parameter Memory Map" on page 15 and Table 3, "Top Parameter Memory Map" on page 16.

The 32-Mbit device has eight partitions, the 64-Mbit device has 16 partitions, and the 128-Mbit device has 32 partitions. Each device density contains one parameter partition and several main partitions. The 4-Mbit parameter partition contains eight 4-Kword parameter blocks and seven 32-Kword main blocks. Each 4-Mbit main partition contains eight 32-Kword blocks each.

The bulk of the array is divided into main blocks that can store code or data, and parameter blocks that allow storage of frequently updated small parameters that are normally stored in EEPROM. By using software techniques, the word-rewrite functionality of EEPROMs can be emulated.

Table 2. Bottom Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Main Partitions	Sixteen Partitions	32					262	7F8000-7FFFFF
		: ·					: ·	: ·
		32					135	400000-407FFF
	Eight Partitions	32			134	3F8000-3FFFFF	134	3F8000-3FFFFF
		: ·			: ·	: ·	: ·	: ·
		32			71	200000-207FFF	71	200000-207FFF
	Four Partitions	32	70	1F8000-1FFFFF	70	1F8000-1FFFFF	70	1F8000-1FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	39	100000-107FFF	39	100000-107FFF	39	100000-107FFF
	One Partition	32	38	0F8000-0FFFFF	38	0F8000-0FFFFF	38	0F8000-0FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	31	0C0000-0C7FFF	31	0C0000-0C7FFF	31	0C0000-0C7FFF
	One Partition	32	30	0B8000-0BFFFF	30	0B8000-0BFFFF	30	0B8000-0BFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	23	080000-087FFF	23	080000-087FFF	23	080000-087FFF
	One Partition	32	22	078000-07FFFF	22	078000-07FFFF	22	078000-07FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	15	040000-047FFF	15	040000-047FFF	15	040000-047FFF
Parameter Partition	One Partition	32	14	038000-03FFFF	14	038000-03FFFF	14	038000-03FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	8	008000-00FFFF	8	008000-00FFFF	8	008000-00FFFF
		4	7	007000-007FFF	7	007000-007FFF	7	007000-007FFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		4	0	000000-000FFF	0	000000-000FFF	0	000000-000FFF

Table 3. Top Parameter Memory Map

		Size (KW)	Blk #	32 Mbit	Blk #	64 Mbit	Blk #	128 Mbit
Parameter Partition	One Partition	4	70	1FF000-1FFFFF	134	3FF000-3FFFFF	262	7FF000-7FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		4	63	1F8000-1F8FFF	127	3F8000-3F8FFF	255	7F8000-7F8FFF
		32	62	1F0000-1F7FFF	126	3F0000-3F7FFF	254	7F0000-7F7FFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	56	1C0000-1C7FFF	120	3C0000-3C7FFF	248	7C0000-7C7FFF
Main Partitions	One Partition	32	55	1B8000-1BFFFF	119	3B8000-3BFFFF	247	7B8000-7BFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	48	18000-187FFF	112	380000-387FFF	240	780000-787FFF
	One Partition	32	47	178000-17FFFF	111	378000-37FFFF	239	778000-77FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	40	140000-147FFF	104	340000-347FFF	232	740000-747FFF
	One Partition	32	39	138000-13FFFF	103	338000-33FFFF	231	738000-73FFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	32	100000-107FFF	96	300000-307FFF	224	700000-707FFF
	Four Partitions	32	31	0F8000-0FFFFF	95	2F8000-2FFFFF	223	6F8000-6FFFFF
		: ·	: ·	: ·	: ·	: ·	: ·	: ·
		32	0	000000-007FFF	64	200000-207FFF	192	600000-607FFF
	Eight Partitions	32			63	1F8000-1FFFFF	191	5F8000-5FFFFF
		: ·			: ·	: ·	: ·	: ·
		32			0	000000-007FFF	128	400000-407FFF
	Sixteen Partitions	32					127	3F8000-3FFFFF
		: ·					: ·	: ·
		32					0	000000-007FFF

3.0 Device Operations

This section provides an overview of device operations. The 1.8 Volt Intel® Wireless Flash memory family includes an on-chip WSM to manage block erase and program algorithms. Its CUI allows minimal processor overhead with RAM-like interface timings.

3.1 Bus Operations

Table 4. Bus Operations

Mode	Notes	RST#	CE#	OE#	WE#	ADV#	WAIT	D[15:0]
Read	4	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	See Note	D_{OUT}
Output Disable	1	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z	High-Z
Standby	1	V_{IH}	V_{IH}	X	X	X	High-Z	High-Z
Reset	1,2	V_{IL}	X	X	X	X	High-Z	High-Z
Write	3	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	High-Z	D_{IN}

NOTES:
1. X must be V_{IL} or V_{IH} for control pins and addresses.
2. RST# must be at V_{SS} ± 0.2 V to meet the maximum specified power-down current.
3. Refer to the Table 6, "Bus Cycle Definitions" on page 21 for valid D_{IN} during a write operation.
4. WAIT is only valid during synchronous array read operations.

3.1.1 Read

The 1.8 Volt Intel Wireless Flash memory has several read configurations:

- Asynchronous page mode read.
- Synchronous burst mode read — outputs four, eight, sixteen, or continuous words, from main blocks and parameter blocks.

Several read modes are available in each partition:

- **Read-array mode:** read accesses return flash array data from the addressed locations.
- **Read identifier mode:** reads return manufacturer and device identifier data, block lock status, and protection register data. Identifier information can be accessed starting at 4-Mbit partition base addresses; the flash array is not accessible in read identifier mode.
- **Read query mode:** reads return device CFI data. CFI information can be accessed starting at 4-Mbit partition base addresses; the flash array is not accessible in read query mode.
- **Read status register mode:** reads return status register data from the addressed partition. That partition's array data is not accessible. A system processor can check the status register to determine an addressed partition's state or monitor program and erase progress.

All partitions support the synchronous burst mode that internally sequences addresses with respect to the input CLK to select and supply data to the outputs.

Identifier codes, query data, and status register read operations execute as single-synchronous or asynchronous read cycles. WAIT is asserted during these reads.

Access to the modes listed above is independent of V_{PP}. An appropriate CUI command places the device in a read mode. At initial power-up or after reset, the device defaults to asynchronous read-array mode.

Asserting CE# enables device read operations. The device internally decodes upper address inputs to determine which partition is accessed. Asserting ADV# opens the internal address latches. Asserting OE# activates the outputs and gates selected data onto the I/O bus. In asynchronous mode, the address is latched when ADV# is deasserted (when the device is configured to use

ADV#). In synchronous mode, the address is latched by either the rising edge of ADV# or the rising (or falling) CLK edge while ADV# remains asserted, whichever occurs first. WE# and RST# must be at deasserted during read operations.

3.1.2 Burst Suspend

The Burst Suspend feature allows the system to temporarily suspend a synchronous burst operation if the system needs to use the flash address and data bus for other purposes. Burst accesses can be suspended during the initial latency (before data is received) or after the device has output data. When a burst access is suspended, internal array sensing continues and any previously latched internal data is retained.

Burst Suspend occurs when CE# is asserted, the current address has been latched (either ADV# rising edge or valid CLK edge), CLK is halted, and OE# is deasserted. CLK can be halted when it is at V_{IH} or V_{IL}. To resume the burst access, OE# is reasserted and CLK is restarted. Subsequent CLK edges resume the burst sequence where it left off.

Within the device, CE# gates WAIT. Therefore, during Burst Suspend WAIT remains asserted and does not revert to a high-impedance state when OE# is deasserted. This can cause contention with another device attempting to control the system's READY signal during a Burst Suspend. System using the Burst Suspend feature should not connect the device's WAIT signal directly to the system's READY signal.

Refer to Figure 26, "Burst Suspend" on page 71.

3.1.3 Standby

De-asserting CE# deselects the device and places it in standby mode, substantially reducing device power consumption. In standby mode, outputs are placed in a high-impedance state independent of OE#. If deselected during a program or erase algorithm, the device shall consume active power until the program or erase operation completes.

3.1.4 Reset

The device enters a reset mode when RST# is asserted. In reset mode, internal circuitry is turned off and outputs are placed in a high-impedance state.

After returning from reset, a time t_{PHQV} is required until outputs are valid, and a delay (t_{PHWV}) is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored. The device defaults to read-array mode, the status register is set to 80h, and the configuration register defaults to asynchronous page-mode reads.

If RST# is asserted during an erase or program operation, the operation aborts and the memory contents at the aborted block or address are invalid. See Figure 32, "Reset Operations Waveforms" on page 77 for detailed information regarding reset timings.

Like any automated device, it is important to assert RST# during system reset. When the system comes out of reset, the processor expects to read from the flash memory array. Automated flash memories provide status information when read during program or erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. 1.8 Volt Intel Flash memories allow proper CPU initialization following a system reset through the use of the RST# input. In this application, RST# is controlled by the same CPU reset signal, RESET#.

3.1.5 Write

A write occurs when CE# and WE# are asserted and OE# is deasserted. Flash control commands are written to the CUI using standard microprocessor write timings. Proper use of the ADV# input is needed for proper latching of the addresses. Refer to Section 11.3, "AC Write Characteristics" on page 72 for details. The address and data are latched on the rising edge of WE#. Write operations are asynchronous; CLK is ignored (but still may be kept active/toggling).

The CUI does not occupy an addressable memory location within any partition. The system processor must access it at the correct address range depending on the kind of command executed. Programming or erasing may occur in only one partition at a time. Other partitions must be in one of the read modes or erase suspend mode.

Table 5, "Command Codes and Descriptions" on page 19 shows the available commands. Appendix A, "Write State Machine States" on page 80 provides information on moving between different operating modes using CUI commands.

3.2 Device Commands

The device's on-chip WSM manages erase and program algorithms. This local CPU (WSM) controls the device's in-system read, program, and erase operations. Bus cycles to or from the flash memory conform to standard microprocessor bus cycles. RST#, CE#, OE#, WE#, and ADV# control signals dictate data flow into and out of the device. WAIT informs the CPU of valid data during burst reads. Table 4, "Bus Operations" on page 17 summarizes bus operations.

Device operations are selected by writing specific commands into the device's CUI. Table 5, "Command Codes and Descriptions" on page 19 lists all possible command codes and descriptions. Table 6, "Bus Cycle Definitions" on page 21 lists command definitions. Because commands are partition-specific, it is important to issue write commands within the target address range.

Table 5. Command Codes and Descriptions (Sheet 1 of 2)

Operation	Code	Device Command	Description
Read	FFh	Read Array	Places selected partition in read-array mode.
	70h	Read Status Register	Places selected partition in status register read mode. The partition enters this mode after a Program or Erase command is issued to it.
	90h	Read Identifier	Puts the selected partition in read identifier mode. Device reads from partition addresses output manufacturer/device codes, configuration register data, block lock status, or protection register data on D[15:0].
	98h	Read Query	Puts the addressed partition in read query mode. Device reads from the partition addresses output CFI information on D[7:0].
	50h	Clear Status Register	The WSM can set the status register's block lock (SR[1]), V_{PP} (SR[3]), program (SR[4]), and erase (SR[5]) status bits, but it cannot clear them. SR[5:3,1] can only be cleared by a device reset or through the Clear Status Register command.

Table 5. Command Codes and Descriptions (Sheet 2 of 2)

Operation	Code	Device Command	Description
Program	40h	Word Program Setup	This preferred program command's first cycle prepares the CUI for a program operation. The second cycle latches address and data, and executes the WSM program algorithm at this location. Status register updates occur when CE# or OE# is toggled. A Read Array command is required to read array data after programming.
	10h	Alternate Setup	Equivalent to a Program Setup command (40h).
	30h	EFP Setup	This program command activates EFP mode. The first write cycle sets up the command. If the second cycle is an EFP Confirm command (D0h), subsequent writes provide program data. All other commands are ignored after EFP mode begins.
	D0h	EFP Confirm	If the first command was EFP Setup (30h), the CUI latches the address and data, and prepares the device for EFP mode.
Erase	20h	Erase Setup	This command prepares the CUI for Block Erase. The device erases the block addressed by the Erase Confirm command. If the next command is not Erase Confirm, the CUI sets status register bits SR[5:4] to indicate command sequence error and places the partition in the read status register mode.
	D0h	Erase Confirm	If the first command was Erase Setup (20h), the CUI latches address and data, and erases the block indicated by the erase confirm cycle address. During program or erase, the partition responds only to Read Status Register, Program Suspend, and Erase Suspend commands. CE# or OE# toggle updates status register data.
Suspend	B0h	Program Suspend or Erase Suspend	This command, issued at any device address, suspends the currently executing program or erase operation. Status register data indicates the operation was successfully suspended if SR[2] (program suspend) or SR[6] (erase suspend) and SR[7] are set. The WSM remains in the suspended state regardless of control signal states (except RST#).
	D0h	Suspend Resume	This command, issued at any device address, resumes the suspended program or erase operation.
Block Locking	60h	Lock Setup	This command prepares the CUI lock configuration. If the next command is not Lock Block, Unlock Block, or Lock-Down, the CUI sets SR[5:4] to indicate command sequence error.
	01h	Lock Block	If the previous command was Lock Setup (60h), the CUI locks the addressed block.
	D0h	Unlock Block	If the previous command was Lock Setup (60h), the CUI latches the address and unlocks the addressed block. If previously locked-down, the operation has no effect.
	2Fh	Lock-Down	If the previous command was Lock Setup (60h), the CUI latches the address and locks-down the addressed block.
Protection	C0h	Protection Program Setup	This command prepares the CUI for a protection register program operation. The second cycle latches address and data, and starts the WSM's protection register program or lock algorithm. Toggling CE# or OE# updates the flash status register data. To read array data after programming, issue a Read Array command.
Configuration	60h	Configuration Setup	This command prepares the CUI for device configuration. If Set Configuration Register is not the next command, the CUI sets SR[5:4] to indicate command sequence error.
	03h	Set Configuration Register	If the previous command was Configuration Setup (60h), the CUI latches the address and writes the data from A[15:0] into the configuration register. Subsequent read operations access array data.

NOTE: Do not use unassigned commands. Intel reserves the right to redefine these codes for future functions.

Table 6. Bus Cycle Definitions

Operation	Command	Bus Cycles	First Bus Cycle			Second Bus Cycle		
			Oper	Addr[1]	Data[2,3]	Oper	Addr[1]	Data[2,3]
Read	Read Array/Reset	≥1	Write	PnA	FFh	Read	Read Address	Array Data
	Read Identifier	≥ 2	Write	PnA	90h	Read	PBA+IA	IC
	Read Query	≥ 2	Write	PnA	98h	Read	PBA+QA	QD
	Read Status Register	2	Write	PnA	70h	Read	PnA	SRD
	Clear Status Register	1	Write	XX	50h			
Program and Erase	Block Erase	2	Write	BA	20h	Write	BA	D0h
	Word Program	2	Write	WA	40h/10h	Write	WA	WD
	EFP	≥2	Write	WA	30h	Write	WA	D0h
	Program/Erase Suspend	1	Write	XX	B0h			
	Program/Erase Resume	1	Write	XX	D0h			
Lock	Lock Block	2	Write	BA	60h	Write	BA	01h
	Unlock Block	2	Write	BA	60h	Write	BA	D0h
	Lock-Down Block	2	Write	BA	60h	Write	BA	2Fh
Protection	Protection Program	2	Write	PA	C0h	Write	PA	PD
	Lock Protection Program	2	Write	LPA	C0h	Write	LPA	FFFDh
Configuration	Set Configuration Register	2	Write	CD	60h	Write	CD	03h
Configuration	Set Configuration Register	2	Write	CD	60h	Write	CD	03h

NOTES:

1. First-cycle command addresses should be the same as the operation's target address. Examples: the first-cycle address for the Read Identifier command should be the same as the Identification code address (IA); the first-cycle address for the Word Program command should be the same as the word address (WA) to be programmed; the first-cycle address for the Erase/Program Suspend command should be the same as the address within the block to be suspended; etc.
   XX = Any valid address within the device.
   IA = Identification code address.
   BA = Block Address. Any address within a specific block.
   LPA = Lock Protection Address is obtained from the CFI (through the Read Query command). The 1.8 Volt Intel Wireless Flash memory family's LPA is at 0080h.
   PA = User programmable 4-word protection address.
   PnA = Any address within a specific partition.

PBA = Partition Base Address. The very first address of a particular partition.
QA = Query code address.
WA = Word address of memory location to be written.

2. SRD = Status register data.
   WD = Data to be written at location WA.
   IC = Identifier code data.
   PD = User programmable 4-word protection data.
   QD = Query code data on D[7:0].
   CD = Configuration register code data presented on device addresses A[15:0]. A[MAX:16] address bits can select any partition. See Table 13, "Configuration Register Definitions" on page 46 for configuration register bits descriptions.
3. Commands other than those shown above are reserved by Intel for future device implementations and should not be used.

3.3 Command Sequencing

When issuing a 2-cycle write sequence to the flash device, a read operation is allowed to occur *between* the two write cycles. The setup phase of a 2-cycle write sequence places the addressed partition into read-status mode, so if the same partition is read before the second "confirm" write cycle is issued, status register data will be returned. Reads from other partitions, however, can return actual array data assuming the addressed partition is already in read-array mode. Figure 2 on page 22 and Figure 3 on page 22 illustrate these two conditions.

Figure 2. Normal Write and Read Cycles

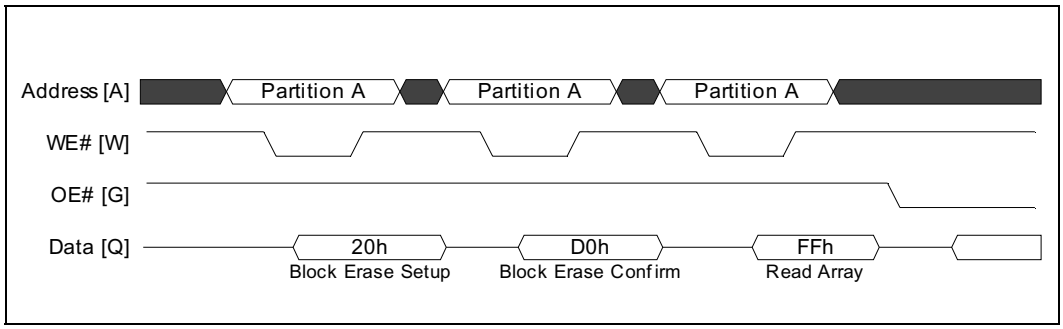
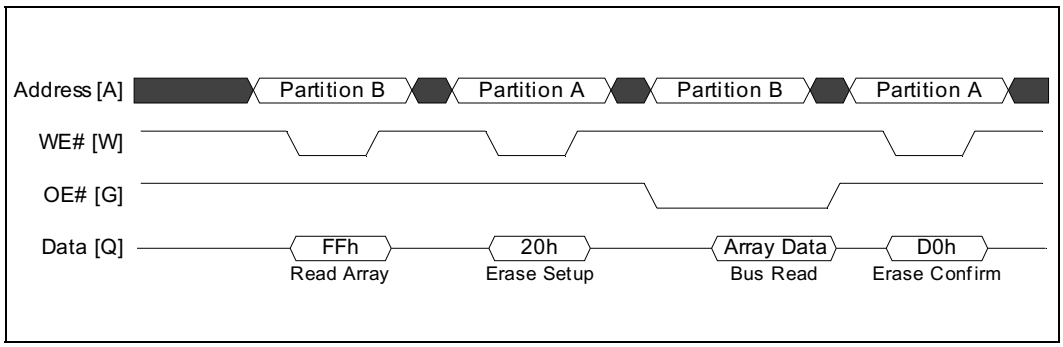
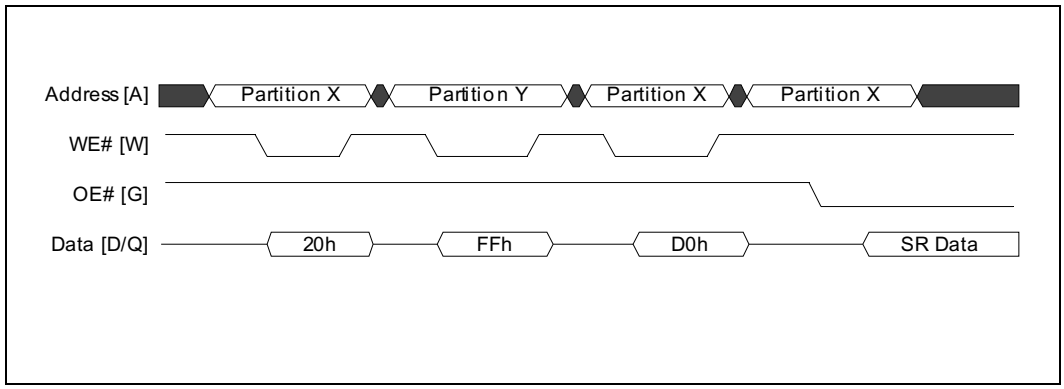


Figure 3. Interleaving a 2-Cycle Write Sequence with an Array Read



By contrast, a write bus cycle may not interrupt a 2-cycle write sequence. Doing so causes a command sequence error to appear in the status register. Figure 4 illustrates a command sequence error.

Figure 4. Improper Command Sequencing



4.0 Read Operations

4.1 Read Array

The Read Array command places (or resets) the partition in read-array mode and is used to read data from the flash memory array. Upon initial device power-up, or after reset (RST# transitions from V_{IL} to V_{IH}), all partitions default to asynchronous read-array mode. To read array data from the flash device, first write the Read Array command (FFh) to the CUI and specify the desired word address. Then read from that address. If a partition is already in read-array mode, issuing the Read Array command is not required to read from that partition.

If the Read Array command is written to a partition that is erasing or programming, the device presents invalid data on the bus until the program or erase operation completes. After the program or erase finishes in that partition, valid array data can then be read. If an Erase Suspend or Program Suspend command suspends the WSM, a subsequent Read Array command places the addressed partition in read-array mode. The Read Array command functions independently of V_{PP}.

4.2 Read Device ID

The read identifier mode outputs the manufacturer/device identifier, block lock status, protection register codes, and configuration register data. The identifier information is contained within a separate memory space on the device and can be accessed along the 4-Mbit partition address range supplied by the Read Identifier command (90h) address. Reads from addresses in Table 7 retrieve ID information. Issuing a Read Identifier command to a partition that is programming or erasing places that partition's outputs in read ID mode while the partition continues to program or erase in the background.

Table 7. Device Identification Codes

Item	Address[1]		Data	Description
	Base	Offset		
Manufacturer ID	Partition	00h	0089h	
Device ID	Partition	01h	8862h	32-Mbit TPD
			8863h	32-Mbit BPD
			8864h	64-Mbit TPD
			8865h	64-Mbit BPD
			8866h	128-Mbit TPD
			8867h	128-Mbit BPD
Block Lock Status(2)	Block	02h	D0 = 0	Block is unlocked
			D0 = 1	Block is locked
Block Lock-Down Status(2)	Block	02h	D1 = 0	Block is not locked-down
			D1 = 1	Block is locked down
Configuration Register	Partition	05h	Register Data	
Protection Register Lock Status	Partition	80h	Lock Data	
Protection Register	Partition	81h - 88h	Register Data	Multiple reads required to read the entire 128-bit Protection Register.

NOTES:
1. The address is constructed from a base address plus an offset. For example, to read the Block Lock Status for block number 38 in a BPD, set the address to the BBA (0F8000h) plus the *offset* (02h), i.e. 0F8002h. Then examine bit 0 of the data to determine if the block is locked.
2. See Section 7.1.4, "Block Lock Status" on page 40 for valid lock status.

4.3 Read Query (CFI)

This device contains a separate CFI query *database* that acts as an "on-chip datasheet." The CFI information within this device can be accessed by issuing the Read Query command and supplying a specific address. The address is constructed from the base address of a partition plus a particular offset corresponding to the desired CFI field. Appendix B, "Common Flash Interface" on page 83 shows accessible CFI fields and their address offsets. Issuing the Read Query command to a partition that is programming or erasing puts that partition in read query mode while the partition continues to program or erase in the background.

4.4 Read Status Register

The device's status register displays program and erase operation status. A partition's status can be read after writing the Read Status Register command to any location within the partition's address range. Read-status mode is the default read mode following a Program, Erase, or Lock Block command sequence. Subsequent single reads from that partition will return its status until another valid command is written.

The read-status mode supports single synchronous and single asynchronous reads only; it doesn't support burst reads. The first falling edge of OE# or CE# latches and updates status register data. The operation doesn't affect other partitions' modes. Because the status register is 8 bits wide, only DQ [7:0] contains valid status register data; DQ [15:8] contains zeros. See Table 8, "Status Register Definitions" on page 25 and Table 9, "Status Register Descriptions" on page 25.

Each 4-Mbit partition contains its own status register. Bits SR[6:0] are unique to each partition, but SR[7], the Device WSM Status (DWS) bit, pertains to the entire device. SR[7] provides program and erase status of the entire device. By contrast, the Partition WSM Status (PWS) bit, SR[0], provides program and erase status of the *addressed partition* only. Status register bits SR[6:1] present information about partition-specific program, erase, suspend, V_{PP}, and block-lock states. Table 10, "Status Register Device WSM and Partition Write Status Description" on page 26 presents descriptions of DWS (SR[7]) and PWS (SR[0]) combinations.

Table 8. Status Register Definitions

DWS	ESS	ES	PS	VPPS	PSS	DPS	PWS
7	6	5	4	3	2	1	0

Table 9. Status Register Descriptions

Bit	Name	State	Description
7	**DWS** Device WSM Status	0 = Device WSM is Busy 1 = Device WSM is Ready	SR[7] indicates erase or program completion in the device. SR[6:1] are invalid while SR[7] = 0. See Table 10 for valid SR[7] and SR[0] combinations.
6	**ESS** Erase Suspend Status	0 = Erase in progress/completed 1 = Erase suspended	After issuing an Erase Suspend command, the WSM halts and sets SR[7] and SR[6]. SR[6] remains set until the device receives an Erase Resume command.
5	**ES** Erase Status	0 = Erase successful 1 = Erase error	SR[5] is set if an attempted erase failed. A Command Sequence Error is indicated when SR[7,5:4] are set.
4	**PS** Program Status	0 = Program successful 1 = Program error	SR[4] is set if the WSM failed to program a word.
3	**VPPS** VPP Status	0 = V_{PP} OK 1 = V_{PP} low detect, operation aborted	The WSM indicates the V_{PP} level after program or erase completes. SR[3] does not provide continuous V_{PP} feedback and isn't guaranteed when $V_{PP} \neq V_{PP1/2}$.
2	**PSS** Program Suspend Status	0 = Program in progress/completed 1 = Program suspended	After receiving a Program Suspend command, the WSM halts execution and sets SR[7] and SR[2]. They remain set until a Resume command is received.
1	**DPS** Device Protect Status	0 = Unlocked 1 = Aborted erase/program attempt on locked block	If an erase or program operation is attempted to a locked block (if WP# = V_{IL}), the WSM sets SR[1] and aborts the operation.
0	**PWS** Partition Write Status	0 = This partition is busy, but only if SR[7]=0 1 = Another partition is busy, but only if SR[7]=0	Addressed partition is erasing or programming. In EFP mode, SR[0] indicates that a data-stream word has finished programming or verifying depending on the particular EFP phase. See Table 10 for valid SR[7] and SR[0] combinations.

Table 10. Status Register Device WSM and Partition Write Status Description

DWS (SR[7])	PWS (SR[0])	Description
0	0	The addressed partition is performing a program/erase operation. EFP: device has finished programming or verifying data, or is ready for data.
0	1	A partition other than the one currently addressed is performing a program/erase operation. EFP: the device is either programming or verifying data.
1	0	No program/erase operation is in progress in any partition. Erase and Program suspend bits (SR[6,2]) indicate whether other partitions are suspended. EFP: the device has exited EFP mode.
1	1	Won't occur in standard program or erase modes. EFP: this combination does not occur.

4.5 Clear Status Register

The Clear Status Register command clears the status register and leaves all partition output states unchanged. The WSM can set all status register bits and clear bits SR[7:6,2,0]. Because bits SR[5,4,3,1] indicate various error conditions, they can only be cleared by the Clear Status Register command. By allowing system software to reset these bits, several operations (such as cumulatively programming several addresses or erasing multiple blocks in sequence) can be performed before reading the status register to determine error occurrence. If an error is detected, the Status Register must be cleared before beginning another command or sequence. Device reset (RST# = V_{IL}) also clears the status register. This command functions independently of V_{PP}.

5.0 Program Operations

5.1 Word Program

When the Word Program command is issued, the WSM executes a sequence of internally timed events to program a word at the desired address and verify that the bits are sufficiently programmed. Programming the flash array changes specifically addressed bits to 0; 1 bits do not change the memory cell contents.

Programming can occur in only one partition at a time. All other partitions must be in either a read mode or erase suspend mode. Only one partition can be in erase suspend mode at a time.

The status register can be examined for program progress by reading any address within the partition that is busy programming. However, while most status register bits are partition-specific, the Device WSM Status bit, SR[7], is *device*-specific; that is, if the status register is read from any other partition, SR[7] indicates program status of the entire device. This permits the system CPU to monitor program progress while reading the status of other partitions.

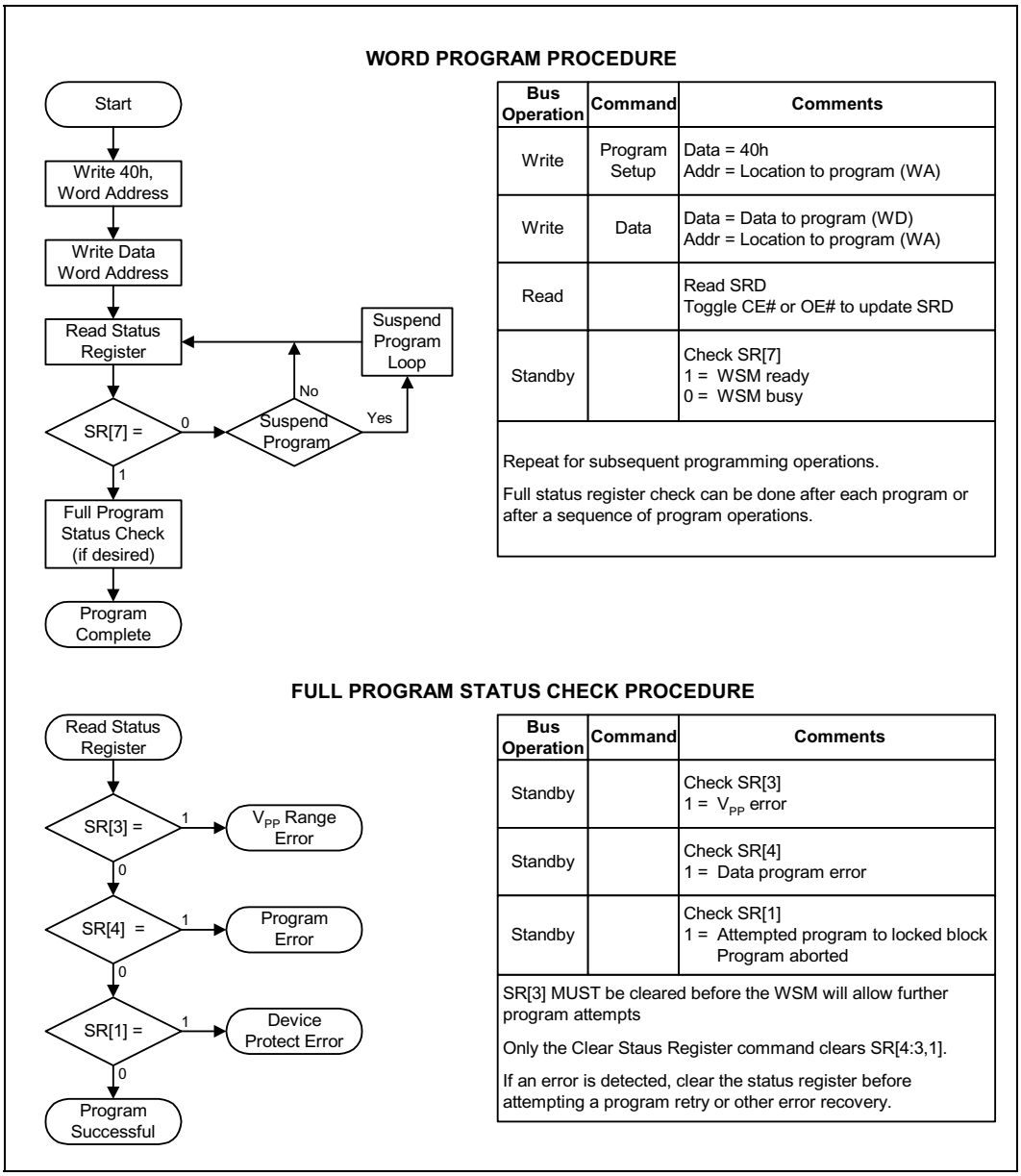
CE# or OE# toggle (during polling) updates the status register. Several commands can be issued to a partition that is programming: Read Status Register, Program Suspend, Read Identifier, and Read Query. The Read Array command can also be issued, but the read data is indeterminate.

After programming completes, three status register bits can signify various possible error conditions. SR[4] indicates a program failure if set. If SR[3] is set, the WSM couldn't execute the Word Program command because V_{PP} was outside acceptable limits. If SR[1] is set, the program was aborted because the WSM attempted to program a locked block.

After the status register data is examined, clear it with the Clear Status Register command before a new command is issued. The partition remains in status register mode until another command is written to that partition. Any command can be issued after the status register indicates program completion.

If CE# is deasserted while the device is programming, the devices will not enter standby mode until the program operation completes.

Figure 5. Word Program Flowchart



5.2 Factory Programming

The standard factory programming mode uses the same commands and algorithm as the Word Program mode (40h/10h). When V_{PP} is at V_{PP1}, program and erase currents are drawn through VCC. If VPP is driven by a logic signal, V_{PP1} must remain above the V_{PP1}Min value to perform in-system flash modifications. When VPP is connected to a 12 V power supply, the device draws program and erase current directly from VPP. This eliminates the need for an external switching transistor to control the V_{PP} voltage. Figure 14, “Examples of VPP Power Supply Configurations” on page 44 shows examples of flash power supply usage in various configurations.

The 12-V V_{PP} mode enhances programming performance during the short time period typically found in manufacturing processes; however, it is not intended for extended use.12 V may be applied to V_{PP} during program and erase operations as specified in Section 10.2, "Operating Conditions" on page 56. VPP may be connected to 12 V for a total of t_{PPH} hours maximum. Stressing the device beyond these limits may cause permanent damage.

5.3 Enhanced Factory Program (EFP)

EFP substantially improves device programming performance through a number of enhancements to the conventional 12 Volt word program algorithm. EFP's more efficient WSM algorithm eliminates the traditional overhead delays of the conventional word program mode in both the host programming system and the flash device. Changes to the conventional word programming flowchart and internal WSM routine were developed because of today's beat-rate-sensitive manufacturing environments; a balance between programming speed and cycling performance was attained.

The host programmer writes data to the device and checks the Status Register to determine when the data has completed programming. This modification essentially cuts write bus cycles in half. Following each internal program pulse, the WSM increments the device's address to the next physical location. Now, programming equipment can sequentially stream program data throughout an entire block without having to setup and present each new address. In combination, these enhancements reduce much of the host programmer overhead, enabling more of a data streaming approach to device programming.

EFP further speeds up programming by performing internal code verification. With this, PROM programmers can rely on the device to verify that it has been programmed properly. From the device side, EFP streamlines internal overhead by eliminating the delays previously associated to switch voltages between programming and verify levels at each memory-word location.

EFP consists of four phases: setup, program, verify and exit. Refer to Figure 6, "Enhanced Factory Program Flowchart" on page 32 for a detailed graphical representation of how to implement EFP.

5.3.1 EFP Requirements and Considerations

EFP requirements:

- Ambient temperature: T_A = 25 °C ±5 °C
- V_{CC} within specified operating range
- V_{PP} within specified V_{PP2} range
- Target block unlocked

EFP considerations:

- Block cycling below 100 erase cycles [1]
- RWW not supported[2]
- EFP programs one block at a time
- EFP cannot be suspended

1. Recommended for optimum performance. Some degradation in performance may occur if this limit is exceeded, but the internal algorithm will continue to work properly.
2. Code or data cannot be read from another partition during EFP.

5.3.2 Setup

After receiving the EFP Setup (30h) and EFP Confirm (D0h) command sequence, SR[7] transitions from a 1 to a 0 indicating that the WSM is busy with EFP algorithm startup. A delay before checking SR[7] is required to allow the WSM time to perform all of its setups and checks (V_{PP} level and block lock status). If an error is detected, status register bits SR[4], SR[3], and/or SR[1] are set and EFP operation terminates.

Note: After the EFP Setup and Confirm command sequence, reads from the device automatically output status register data. Do not issue the Read Status Register command; it will be interpreted as data to program at WA_0.

5.3.3 Program

After setup completion, the host programming system must check SR[0] to determine “data-stream ready" status (SR[0]=0). Each subsequent write after this is a program-data write to the flash array. Each cell within the memory word to be programmed to 0 receives one WSM pulse; additional pulses, if required, occur in the verify phase. SR[0]=1 indicates that the WSM is busy applying the program pulse.

The host programmer must poll the device's status register for the "program done" state after each data-stream write. SR[0]=0 indicates that the appropriate cell(s) within the accessed memory location have received their single WSM program pulse, and that the device is now ready for the next word. Although the host may check full status for errors at any time, it is only necessary on a block basis, after EFP exit.

Addresses must remain within the target block. Supplying an address outside the target block immediately terminates the program phase; the WSM then enters the EFP verify phase.

The address can either hold constant or it can increment. The device compares the incoming address to that stored from the setup phase (WA_0); if they match, the WSM programs the new data word at the next sequential memory location. If they differ, the WSM jumps to the new address location.

The program phase concludes when the host programming system writes to a different block address, and data supplied must be FFFFh. Upon program phase completion, the device enters the EFP verify phase.

5.3.4 Verify

A high percentage of the flash bits program on the first WSM pulse. However, for those cells that do not completely program on their first attempt, EFP internal verification identifies them and applies additional pulses as required.

The verify phase is identical in flow to the program phase, except that instead of programming incoming data, the WSM compares the verify-stream data to that which was previously programmed into the block. If the data compares correctly, the host programmer proceeds to the next word. If not, the host waits while the WSM applies an additional pulse(s).

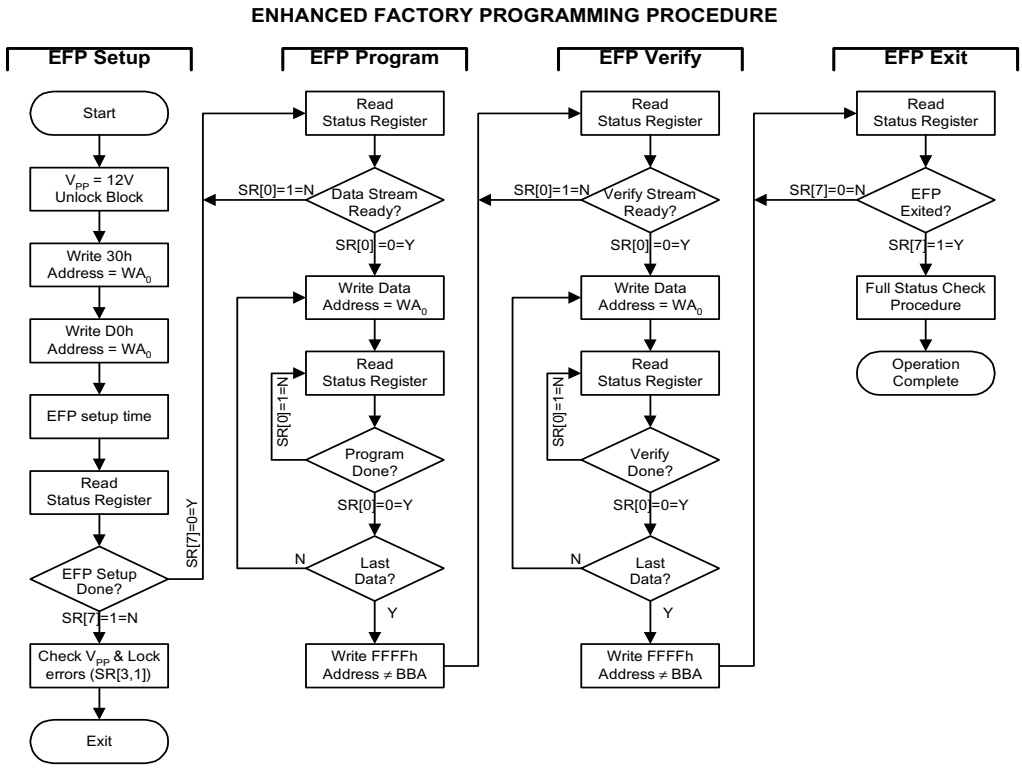
The host programmer must reset its initial verify-word address to the same starting location supplied during the program phase. It then reissues each data word in the same order as during the program phase. Like programming, the host may write each subsequent data word to WA_0 or it may increment up through the block addresses.

The verification phase concludes when the interfacing programmer writes to a different block address; data supplied must be FFFFh. Upon completion of the verify phase, the device enters the EFP exit phase.

5.3.5 Exit

SR[7]=1 indicates that the device has returned to normal operating conditions. A full status check should be performed at this time to ensure the entire block programmed successfully. After EFP exit, any valid CUI command can be issued.

Figure 6. Enhanced Factory Program Flowchart



EFP Setup		
Bus State		**Comments**
Write	Unlock Block	V_{PP} = 12V Unlock block
Write	EFP Setup	Data = 30h Address = WA_0
Write	EFP Confirm	Data = D0h Address = WA_0
Standby		EFP setup time
Read		Status Register
Standby	EFP Setup Done?	Check SR[7] 0 = EFP ready 1 = EFP not ready
Standby	Error Condition Check	If SR[7] = 1: Check SR[3,1] SR[3] = 1 = V_{PP} error SR[1] = 1 = locked block

EFP Program		
Bus State		**Comments**
Read		Status Register
Standby	Data Stream Ready?	Check SR[0] 0 = Ready for data 1 = Not ready for data
Write (note 1)		Data = Data to program Address = WA_0
Read		Status Register
Standby	Program Done?	Check SR[0] 0 = Program done 1 = Program not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Program Phase	Data = FFFFh Address not within same BBA

EFP Verify		
Bus State		**Comments**
Read		Status Register
Standby	Verify Stream Ready?	Check SR[0] 0 = Ready for verify 1 = Not ready for verify
Write (note 2)		Data = Word to verify Address = WA_0
Read		Status Register
Standby (note 3)	Verify Done?	Check SR[0] 0 = Verify done 1 = Verify not done
Standby	Last Data?	Device automatically increments address.
Write	Exit Verify Phase	Data = FFFFh Address not within same BBA

EFP Exit		
Read		Status Register
Standby	EFP Exited?	Check SR[7] 0 = Exit not finished 1 = Exit completed

Repeat for subsequent operations.

After EFP exit, a Full Status Check can determine if any program error occurred.

See the Full Status Check procedure in the Word Program flowchart.

1. WA_0 = first Word Address to be programmed within the target block. The BBA (Block Base Address) must remain constant throughout the program phase data stream; WA can be held constant at the first address location, or it can be written to sequence up through the addresses within the block. Writing to a BBA not equal to that of the block currently being written to terminates the EFP program phase, and instructs the device to enter the EFP verify phase.
2. For proper verification to occur, the verify data stream must be presented to the device in the same sequence as that of the program phase data stream. Writing to a BBA not equal to WA terminates the EFP verify phase, and instructs the device to exit EFP .
3. Bits that did not fully program with the single WSM pulse of the EFP program phase receive additional program-pulse attempts during the EFP verify phase. The device will report any program failure by setting SR[4]=1; this check can be performed during the full status check after EFP has been exited for that block, and will indicate any error within the entire data stream.

6.0 Program and Erase Operations

6.1 Program/Erase Suspend and Resume

The Program Suspend and Erase Suspend commands halt an in-progress program or erase operation. The command can be issued at any device address. The partition corresponding to the command's address remains in its previous state. A suspend command allows data to be accessed from memory locations other than the one being programmed or the block being erased.

A program operation can be suspended only to perform a read operation. An erase operation can be suspended to perform either a program or a read operation within any block, except the block that is erase suspended. A program command nested within a suspended erase can subsequently be suspended to read yet another location. Once a program or erase process starts, the Suspend command requests that the WSM suspend the program or erase sequence at predetermined points in the algorithm. The partition that is actually suspended continues to output status register data after the Suspend command is written. An operation is suspended when status bits SR[7] and SR[6] and/or SR[2] are set.

To read data from blocks within the partition (other than an erase-suspended block), you can write a Read Array command. Block erase cannot resume until the program operations initiated during erase suspend are complete. Read Array, Read Status Register, Read Identifier (ID), Read Query, and Program Resume are valid commands during Program or Erase Suspend. Additionally, Clear Status Register, Program, Program Suspend, Erase Resume, Lock Block, Unlock Block, and Lock-Down Block are valid commands during erase suspend.

To read data from a block in a partition that is not programming or erasing, the operation does not need to be suspended. If the other partition is already in read array, ID, or Query mode, issuing a valid address returns corresponding data. If the other partition is not in a read mode, one of the read commands must be issued to the partition before data can be read.

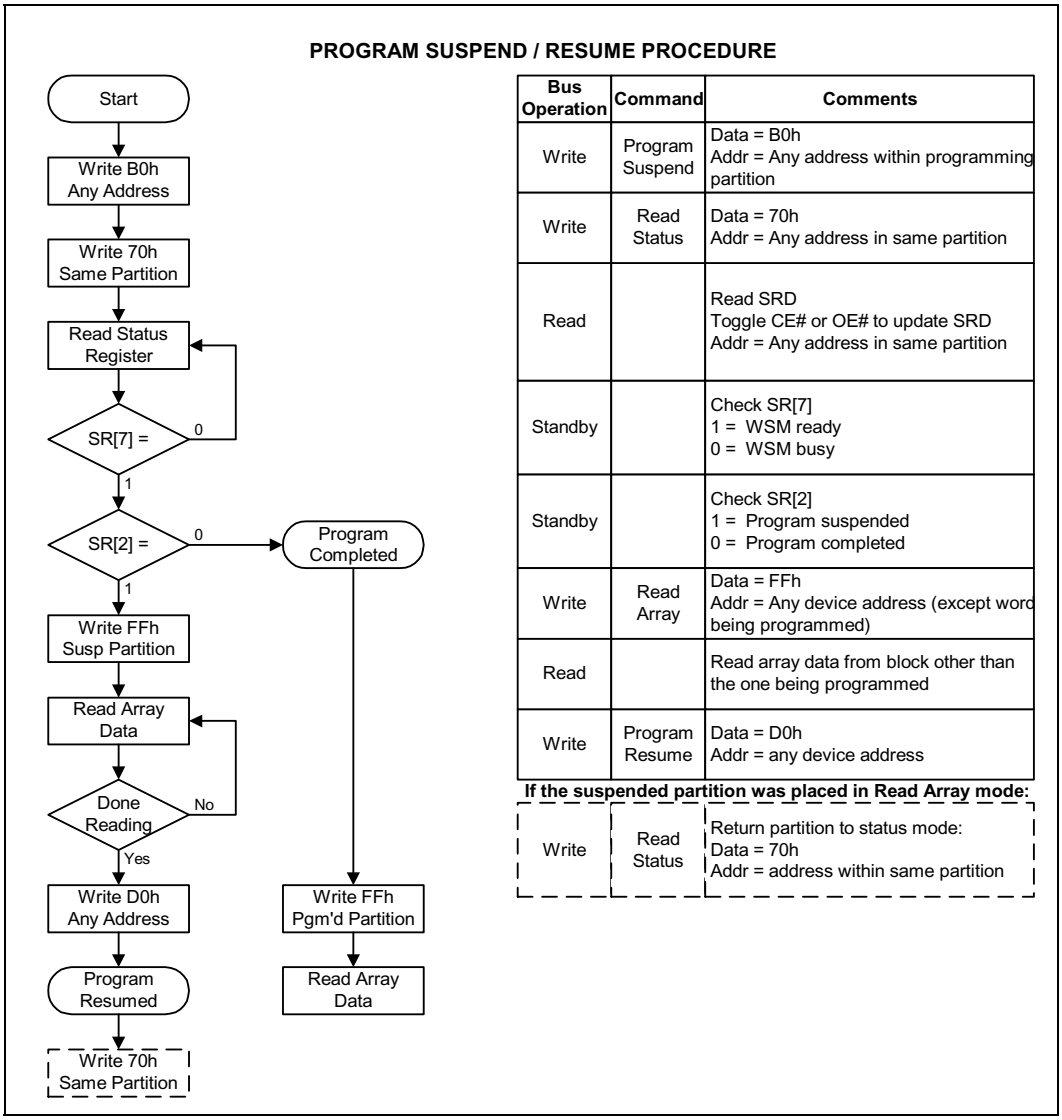
During a suspend, CE# = V_{IH} places the device in standby state, which reduces active current. V_{PP} must remain at its program level and WP# must remain unchanged while in suspend mode.

A resume command instructs the WSM to continue programming or erasing and clears status register bits SR[2] (or SR[6]) and SR[7]. The Resume command can be written to any partition. When read at the partition that is programming or erasing, the device outputs data corresponding to the partition's last mode. If status register error bits are set, the status register can be cleared before issuing the next instruction. RST# must remain at V_{IH}. See Figure 7, "Program Suspend / Resume Flowchart" on page 34, and Figure 8, "Erase Suspend / Resume Flowchart" on page 35.

If a suspended partition was placed in read array, read status register, read identifier (ID), or read query mode during the suspend, the device remains in that mode and outputs data corresponding to that mode after the program or erase operation is resumed. After resuming a suspended operation, issue the read command appropriate to the read operation. To read status after resuming a suspended operation, issue a Read Status Register command (70h) to return the suspended partition to status mode.

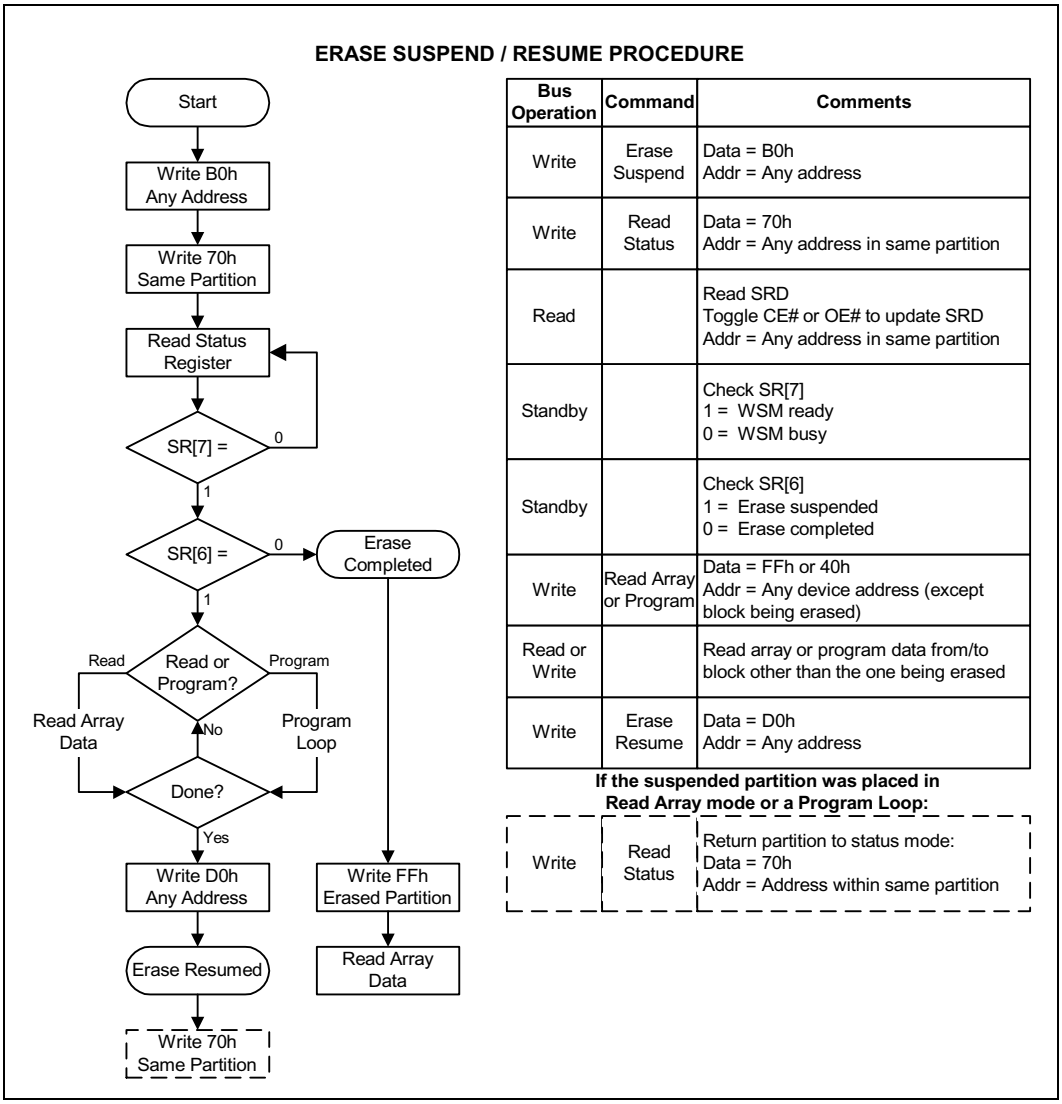
A minimum t_{WHWH} time should elapse between an Erase command and a subsequent Erase Suspend command to ensure that the device achieves sufficient cumulative erase time. Occasional Erase-to-Suspend interrupts do not cause problems, but Erase-to-Suspend commands issued too frequently may produce unexpected results.

Figure 7. Program Suspend / Resume Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0h Addr = Any address within programming partition
Write	Read Status	Data = 70h Addr = Any address in same partition
Read		Read SRD Toggle CE# or OE# to update SRD Addr = Any address in same partition
Standby		Check SR[7] 1 = WSM ready 0 = WSM busy
Standby		Check SR[2] 1 = Program suspended 0 = Program completed
Write	Read Array	Data = FFh Addr = Any device address (except word being programmed)
Read		Read array data from block other than the one being programmed
Write	Program Resume	Data = D0h Addr = any device address
If the suspended partition was placed in Read Array mode:		
Write	Read Status	Return partition to status mode: Data = 70h Addr = address within same partition

Figure 8. Erase Suspend / Resume Flowchart



6.2 Block Erase

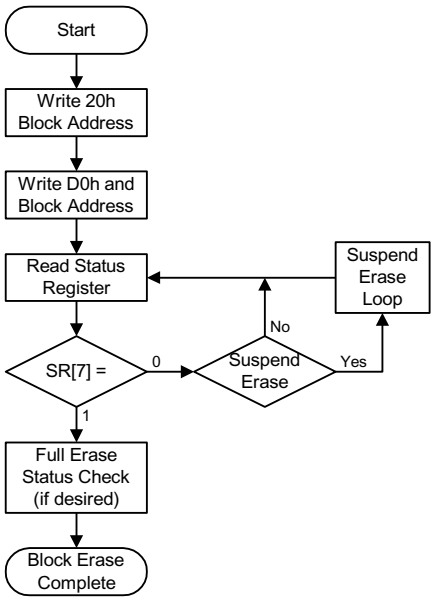
The 2-cycle block erase command sequence, consisting of Erase Setup (20h) and Erase Confirm (D0h), initiates one block erase at the addressed block. Only one partition can be in an erase mode at a time; other partitions must be in a read mode. The Erase Confirm command internally latches the address of the block to be erased. Erase forces all bits within the block to 1. SR[7] is cleared while the erase executes.

After writing the Erase Confirm command, the selected partition is placed in read status register mode and reads performed to that partition return the current status data. The address given during the Erase Confirm command does not need to be the same address used in the Erase Setup command. So, if the Erase Confirm command is given to partition B, then the selected block in partition B will be erased even if the Erase Setup command was to partition A.

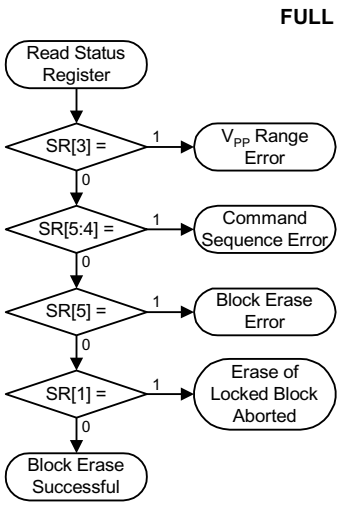
The 2-cycle erase sequence cannot be interrupted with a bus write operation. For example, an Erase Setup command must be immediately followed by the Erase Confirm command in order to execute properly. If a different command is issued between the setup and confirm commands, the partition is placed in read-status mode, the status register signals a command sequence error, and all subsequent erase commands to that partition are ignored until the status register is cleared.

The CPU can detect block erase completion by analyzing SR[7] of that partition. If an error bit (SR[5,3,1]) was flagged, the status register can be cleared by issuing the Clear Status Register command before attempting the next operation. The partition remains in read-status mode until another command is written to its CUI. Any CUI instruction can follow after erasing completes. The CUI can be set to read-array mode to prevent inadvertent status register reads.

Figure 9. Block Erase Flowchart



Bus Operation	Command	Comments
Write	Block Erase Setup	Data = 20h Addr = Block to be erased (BA)
Write	Erase Confirm	Data = D0h Addr = Block to be erased (BA)
Read		Read SRD Toggle CE# or OE# to update SRD
Standby		Check SR[7] 1 = WSM ready 0 = WSM busy
Repeat for subsequent block erasures. Full status register check can be done after each block erase or after a sequence of block erasures.		



Bus Operation	Command	Comments
Standby		Check SR[3] 1 = V_{PP} error
Standby		Check SR[5:4] Both 1 = Command sequence error
Standby		Check SR[5] 1 = Block erase error
Standby		Check SR[1] 1 = Attempted erase of locked block Erase aborted
SR[3,1] **must** be cleared before the WSM will allow further erase attempts. Only the Clear Status Register command clears SR[5:3,1]. If an error is detected, clear the Status register before attempting an erase retry or other error recovery.		

6.3 Read-While-Write and Read-While-Erase

The 1.8 Volt Intel® Wireless Flash memory supports flexible multi-partition dual-operation architecture. By dividing the flash memory into many separate partitions, the device can read from one partition while programing or erasing in another partition; hence the terms, RWW and RWE. Both of these features greatly enhance data storage performance.

The product does not support simultaneous program and erase operations. Attempting to perform operations such as these results in a command sequence error. Only one partition can be programming or erasing while another partition is reading. However, one partition may be in erase suspend mode while a second partition is performing a program operation, and yet another partition is executing a read command. Table 5, “Command Codes and Descriptions” on page 19 describes the command codes available for all functions.

7.0 Security Modes

The 1.8 Volt Intel Wireless Flash memory offers both hardware and software security features to protect the flash data. The software security feature is used by executing the Lock Block command. The hardware security feature is used by executing the Lock-Down Block command *and* by asserting the WP# signal.

Refer to Figure 10, “Block Locking State Diagram” on page 39 for a state diagram of the flash security features. Also see Figure 11, “Locking Operations Flowchart” on page 41.

7.1 Block Lock Operations

Individual instant block locking protects code and data by allowing any block to be locked or unlocked with no latency. This locking scheme offers two levels of protection. The first allows software-only control of block locking (useful for frequently changed data blocks), while the second requires hardware interaction before locking can be changed (protects infrequently changed code blocks).

The following sections discuss the locking system operation. The term “state [XYZ]” specifies locking states; for example, “state [001],” where X = WP# value, Y = block lock-down status bit D1, and Z = Block Lock status register bit D0. Figure 10, “Block Locking State Diagram” on page 39 defines possible locking states.

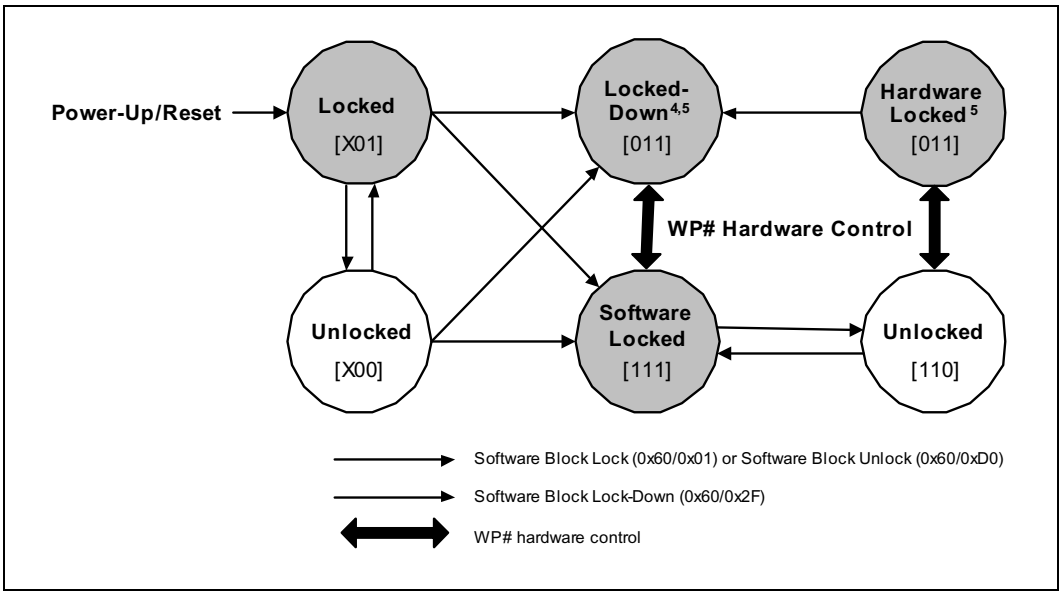
The following summarizes the locking functionality.

- All blocks power-up in a locked state.
- Unlock commands can unlock these blocks, and lock commands can lock them again.
- The Lock-Down command locks a block and prevents it from being unlocked when WP# is asserted.
  - Locked-down blocks can be unlocked or locked with commands as long as WP# is deasserted
  - When WP# is asserted, previously locked-down blocks return to lock-down.
  - The lock-down status bit is cleared only when the device is reset or powered-down.

Block lock registers are not affected by the V_{PP} level. They may be modified and read even if $V_{PP} \leq V_{PPLK}$.

Each block’s locking status can be set to locked, unlocked, and lock-down, as described in the following sections. See Figure 11, “Locking Operations Flowchart” on page 41.

Figure 10. Block Locking State Diagram



NOTE: The notation [X,Y,Z] denotes the locking state of a block, The current locking state of a block is defined by the state of WP# and the two bits of the block-lock status D[1:0].

7.1.1 Lock

All blocks default to locked (state [x01]) after initial power-up or reset. Locked blocks are fully protected from alteration. Attempted program or erase operations to a locked block will return an error in SR[1]. Unlocked blocks can be locked by using the Lock Block command sequence. Similarly, a locked block's status can be changed to unlocked or lock-down using the appropriate software commands.

7.1.2 Unlock

Unlocked blocks (states [x00] and [110]) can be programmed or erased. All unlocked blocks return to the locked state when the device is reset or powered-down. An unlocked block's status can be changed to the locked or locked-down state using the appropriate software commands. A locked block can be unlocked by writing the Unlock Block command sequence if the block is not locked-down.

7.1.3 Lock-Down

Locked-down blocks (state [011]) offer the user an additional level of write protection beyond that of a regular locked block. A block that is locked-down cannot have it's state changed by software if WP# is asserted. A locked or unlocked block can be locked-down by writing the Lock-Down Block command sequence. If a block was set to locked-down, then later changed to unlocked, a Lock-Down command should be issued prior asserting WP# will put that block back to the locked-down state. When WP# is deasserted, locked-down blocks are changed to the locked state and can then be unlocked by the Unlock Block command.

7.1.4 Block Lock Status

Every block's lock status can be read in read identifier mode. To enter this mode, issue the Read Identifier command to the device. Subsequent reads at Block Base Address + 02h will output that block's lock status. For example, to read the block lock status of block 10, the address sent to the device should be 50002h (for a top-parameter device). The lowest two data bits of the read data, D1 and D0, represent the lock status. D0 indicates the block lock status. It is set by the Lock Block command and cleared by the Block Unlock command. It is also set when entering the lock-down state. D1 indicates lock-down status and is set by the Lock-Down command. The lock-down status bit cannot be cleared by software–only by device reset or power-down. See Table 11.

Table 11. Write Protection Truth Table

VPP	WP#	RST#	Write Protection
X	X	V_{IL}	Device inaccessible
V_{IL}	X	V_{IH}	Word program and block erase prohibited
X	V_{IL}	V_{IH}	All lock-down blocks locked
X	V_{IH}	V_{IH}	All lock-down blocks can be unlocked

7.1.5 Lock During Erase Suspend

Block lock configurations can be performed during an erase suspend operation by using the standard locking command sequences to unlock, lock, or lock-down a block. This feature is useful when another block requires immediate updating.

To change block locking during an erase operation, first write the Erase Suspend command. After checking SR[6] to determine the erase operation has suspended, write the desired lock command sequence to a block; the lock status will be changed. After completing lock, unlock, read, or program operations, resume the erase operation with the Erase Resume command (D0h).

If a block is locked or locked-down during a suspended erase of the same block, the locking status bits change immediately. When the erase operation is resumed, it will complete normally.

Locking operations cannot occur during program suspend. Appendix A, "Write State Machine States" on page 80 shows valid commands during erase suspend.

7.1.6 Status Register Error Checking

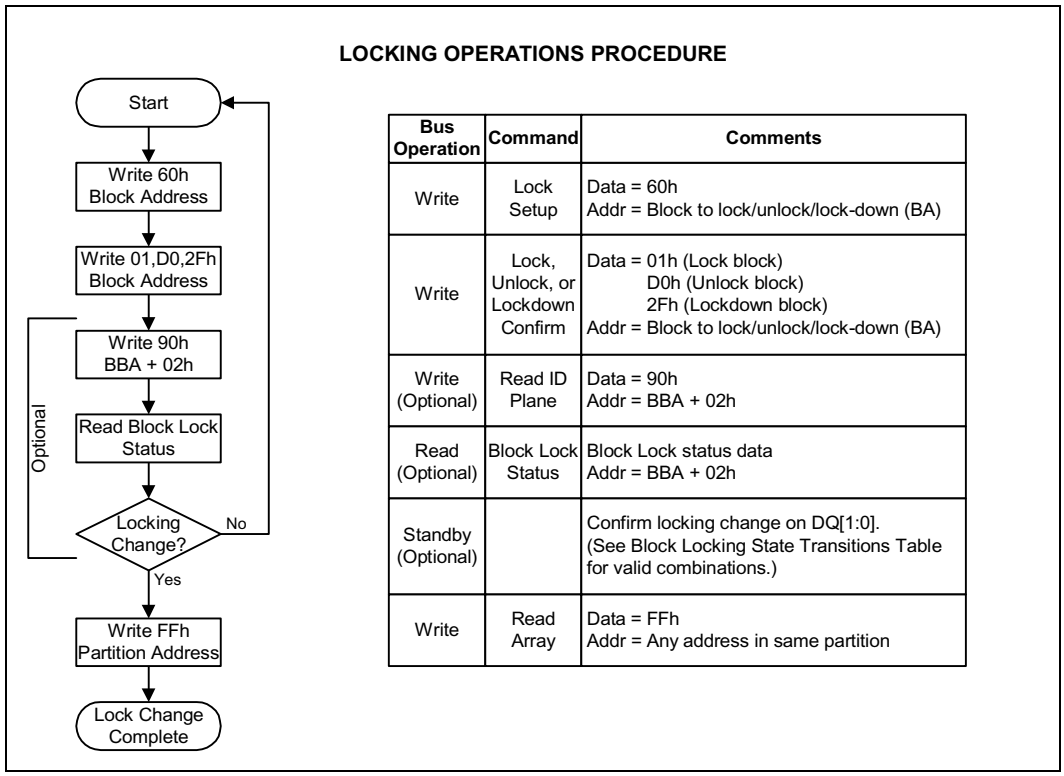
Using nested locking or program command sequences during erase suspend can introduce ambiguity into status register results.

Because locking changes require 2-cycle command sequences, for example, 60h followed by 01h to lock a block, following the Configuration Setup command (60h) with an invalid command produces a command sequence error (SR[5:4]=11b). If a Lock Block command error occurs during erase suspend, the device sets SR[4] and SR[5] to 1 even after the erase is resumed. When erase is complete, possible errors during the erase cannot be detected from the status register because of the previous locking command error. A similar situation occurs if a program operation error is nested within an erase suspend.

7.1.7 WP# Lock-Down Control

The Write Protect signal, WP#, adds an additional layer of block security. WP# only affects blocks that once had the Lock-Down command written to them. After the lock-down status bit is set for a block, asserting WP# forces that block into the lock-down state [011] and prevents it from being unlocked. After WP# is deasserted, the block's state reverts to locked [111] and software commands can then unlock the block (for erase or program operations) and subsequently re-lock it. Only device reset or power-down can clear the lock-down status bit and render WP# ineffective.

Figure 11. Locking Operations Flowchart



Bus Operation	Command	Comments
Write	Lock Setup	Data = 60h Addr = Block to lock/unlock/lock-down (BA)
Write	Lock, Unlock, or Lockdown Confirm	Data = 01h (Lock block) D0h (Unlock block) 2Fh (Lockdown block) Addr = Block to lock/unlock/lock-down (BA)
Write (Optional)	Read ID Plane	Data = 90h Addr = BBA + 02h
Read (Optional)	Block Lock Status	Block Lock status data Addr = BBA + 02h
Standby (Optional)		Confirm locking change on DQ[1:0]. (See Block Locking State Transitions Table for valid combinations.)
Write	Read Array	Data = FFh Addr = Any address in same partition

7.2 Protection Register

The 1.8 Volt Intel Wireless Flash memory includes a 128-bit protection register. This protection register is used to increase system security and for identification purposes. The protection register value can match the flash component to the system's CPU or ASIC to prevent device substitution.

The lower 64 bits within the protection register are programmed by Intel with a unique number in each flash device. The upper 64 OTP bits within the protection register are left for the customer to program. Once programmed, the customer segment can be locked to prevent further programming.

Note: The individual bits of the user segment of the protection register are OTP, not the register in total. The user may program each OTP bit individually, one at a time, if desired. After the protection

register is locked, however, the entire user segment is locked and no more user bits can be programmed.

The protection register shares some of the same internal flash resources as the parameter partition. Therefore, RWW is only allowed between the protection register and main partitions. Table 12 describes the operations allowed in the protection register, parameter partition, and main partition during RWW and RWE.

Table 12. Simultaneous Operations Allowed with the Protection Register

Protection Register	Parameter Partition Array Data	Main Partitions	Description
Read	See Description	Write/Erase	While programming or erasing in a main partition, the protection register can be read from any other partition. Reading the parameter partition data is not allowed if the protection register is being read from addresses within the parameter partition.
See Description	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers from parameter partition addresses is not allowed.
Read	Read	Write/Erase	While programming or erasing in a main partition, read operations are allowed in the parameter partition. Accessing the protection registers in a partition that is *different* from the one being programmed or erased, and also *different* from the parameter partition, is allowed.
Write	No Access Allowed	Read	While programming the protection register, reads are only allowed in the other main partitions. Access to the parameter partition is not allowed. This is because programming of the protection register can only occur in the parameter partition, so it will exist in status mode.
No Access Allowed	Write/Erase	Read	While programming or erasing the parameter partition, reads of the protection registers are not allowed in *any* partition. Reads in other main partitions are supported.

7.2.1 Reading the Protection Register

Writing the Read Identifier command allows the protection register data to be read 16 bits at a time from addresses shown in Table 7, “Device Identification Codes” on page 24. The protection register is read from the Read Identifier command and can be read in any partition.Writing the Read Array command returns the device to read-array mode.

7.2.2 Programing the Protection Register

The Protection Program command should be issued only at the bottom partition followed by the data to be programmed at the specified location. It programs the upper 64 bits of the protection register 16 bits at a time. Table 7, “Device Identification Codes” on page 24 shows allowable addresses. See also Figure 12, “Protection Register Programming Flowchart” on page 43. Issuing a Protection Program command outside the register’s address space results in a status register error (SR[4]=1).

7.2.3 Locking the Protection Register

PR-LK.0 is programmed to 0 by Intel to protect the unique device number. PR-LK.1 can be programmed by the user to lock the user portion (upper 64 bits) of the protection register (See Figure 13, "Protection Register Locking). This bit is set using the Protection Program command to program "FFFDh" into PR-LK.

After PR-LK register bits are programmed (locked), the protection register's stored values can't be changed. Protection Program commands written to a locked section result in a status register error (SR[4]=1, SR[5]=1).

Figure 12. Protection Register Programming Flowchart

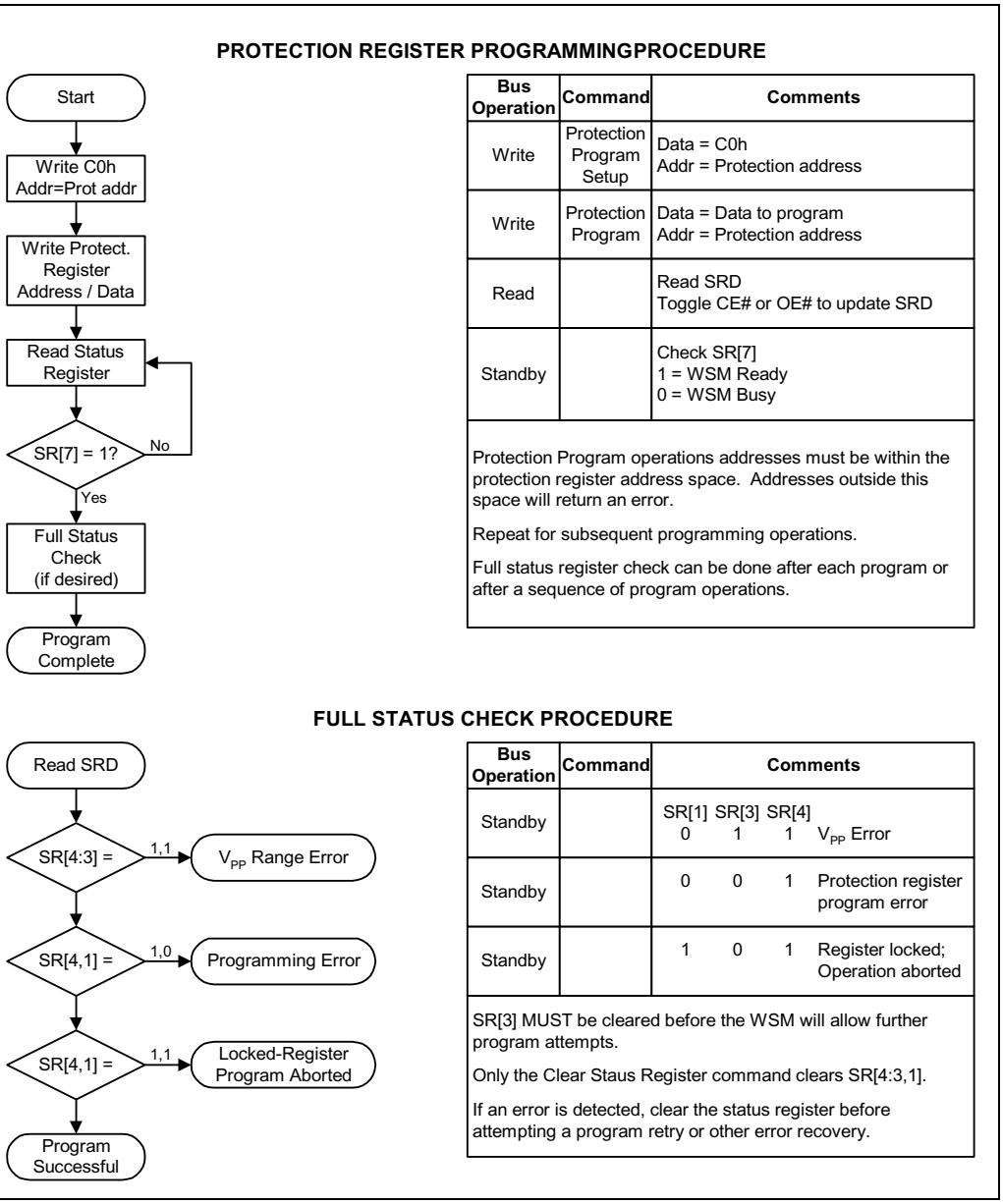
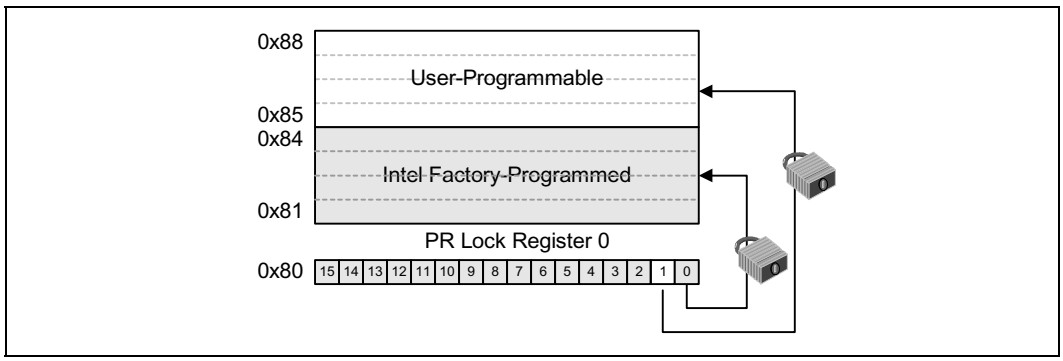


Figure 13. Protection Register Locking

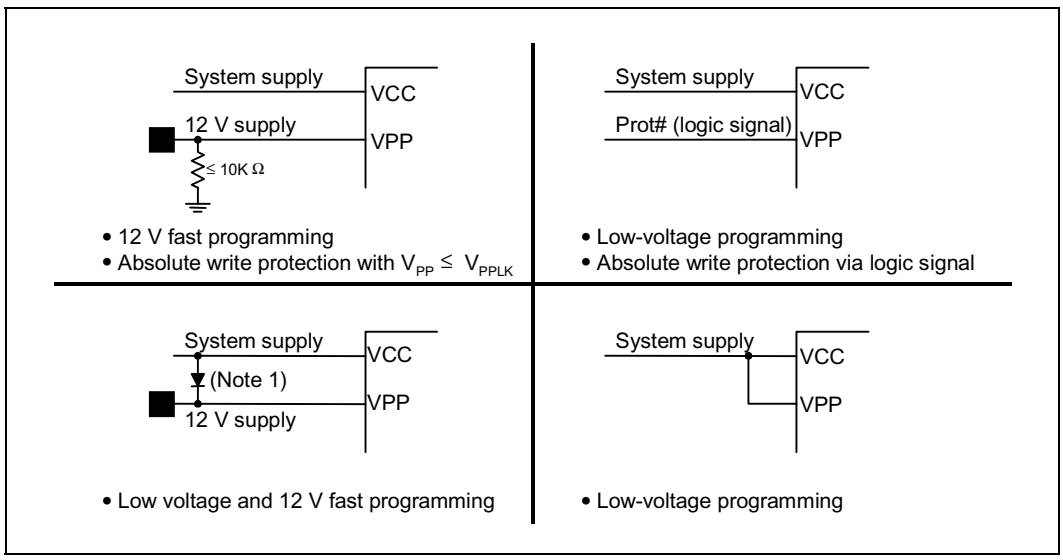


7.3 VPP Protection

The 1.8 Volt Intel® Wireless Flash memory provides in-system program and erase at V_{PP1}. For factory programming, it also includes a low-cost, backward-compatible 12 V programming feature.(See "Factory Programming" on page 28.) The EFP feature can also be used to greatly improve factory program performance as explained in Section 5.3, "Enhanced Factory Program (EFP)" on page 29.

In addition to the flexible block locking, holding the V_{PP} programming voltage low can provide absolute hardware write protection of all flash-device blocks. If V_{PP} is below V_{PPLK}, program or erase operations result in an error displayed in SR[3]. (See Figure 14.)

Figure 14. Examples of VPP Power Supply Configurations



NOTE: If the V_{CC} supply can sink adequate current, you can use an appropriately valued resistor.

8.0 Set Configuration Register

The Set Configuration Register command sets the burst order, frequency configuration, burst length, and other parameters.

A two-bus cycle command sequence initiates this operation. The configuration register data is placed on the lower 16 bits of the address bus (A[15:0]) during both bus cycles. The Set Configuration Register command is written along with the configuration data (on the address bus). This is followed by a second write that confirms the operation and again presents the configuration register data on the address bus. The configuration register data is latched on the rising edge of ADV#, CE#, or WE# (whichever occurs first). This command functions independently of the applied V_{PP} voltage. After executing this command, the device returns to read-array mode. The configuration register's contents can be examined by writing the Read Identifier command and then reading location 05h. (See Table 13 and Table 14.)

Table 13. Configuration Register Definitions

Read Mode	Res'd	First Access Latency Count			WAIT Polarity	Data Output Config	WAIT Config	Burst Seq	Clock Config	Res'd	Res'd	Burst Wrap	Burst Length		
RM	R	LC2	LC1	LC0	WT	DOC	WC	BS	CC	R	R	BW	BL2	BL1	BL0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 14. Configuration Register Descriptions

Bit	Name	Description	Notes[1]
15	**RM** Read Mode	0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)	2
14	**R**	Reserved	5
13-11	**LC2-0** First Access Latency Count	001 = Reserved 010 = Code 2 011 = Code 3 100 = Code 4 101 = Code 5 111 = Reserved (Default)	
10	**WT** WAIT Signal Polarity	0 = WAIT signal is asserted low 1 = WAIT signal is asserted high (Default)	3
9	**DOC** Data Output Configuration	0 = Hold Data for One Clock 1 = Hold Data for Two Clock (Default)	
8	**WC** WAIT Configuration	0 = WAIT Asserted During Delay 1 = WAIT Asserted One Data Cycle before Delay (Default)	
7	**BS** Burst Sequence	0 = Intel Burst Order 1 = Linear Burst Order (Default)	
6	**CC** Clock Configuration	0 = Burst Starts and Data Output on Falling Clock Edge 1 = Burst Starts and Data Output on Rising Clock Edge (Default)	
5	**R**	Reserved	5
4	**R**	Reserved	5
3	**BW** Burst Wrap	0 = Wrap bursts within burst length set by CR[2:0] 1 = Don't wrap accesses within burst length set by CR[2:0].(Default)	
2-0	**BL2-0** Burst Length	001 = 4-Word Burst 010 = 8-Word Burst 011 = 16-Word Burst 111 = Continuous Burst (Default)	4

NOTES:
1. Undocumented combinations of bits are reserved by Intel for future implementations.
2. Synchronous and page read mode configurations affect reads from main blocks and parameter blocks. Status register and configuration reads support single read cycles. CR[15]=1 disables configuration set by CR[14:0].
3. Data is not ready when WAIT is asserted.
4. Set the synchronous burst length. In asynchronous page mode, the burst length equals four words.
5. Set all reserved configuration register bits to zero.

8.1 Read Mode (CR[15])

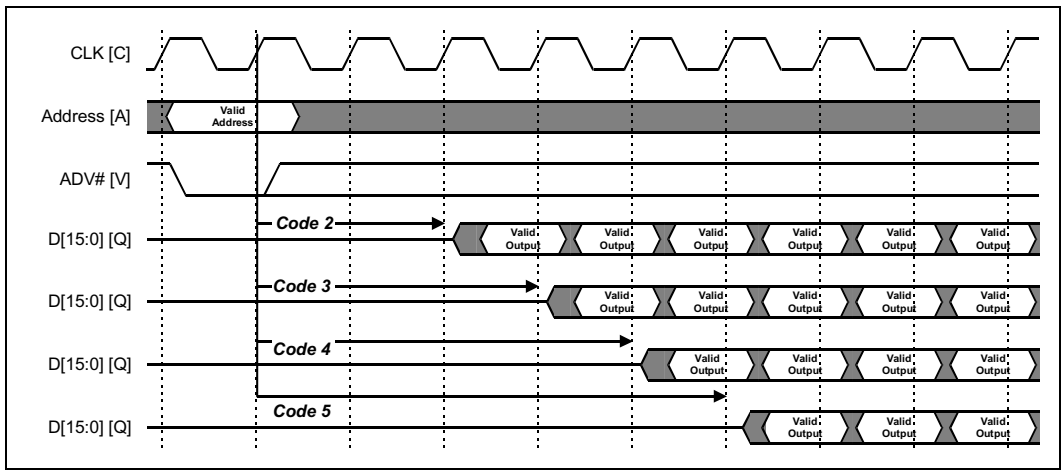
All partitions support two high-performance read configurations: synchronous burst mode and asynchronous page mode (default). CR[15] sets the read configuration to one of these modes.

Status register, query, and identifier modes support only asynchronous and single-synchronous read operations.

8.2 First Access Latency Count (CR[13:11])

The First Access Latency Count (CR[13:11]) configuration tells the device how many clocks must elapse from ADV# de-assertion (V_{IH}) before the first data word should be driven onto its data pins. The input clock frequency determines this value. See Table 13, "Configuration Register Definitions" on page 46 for latency values. Figure 15 shows data output latency from ADV# assertion for different latencies.

Figure 15. First Access Latency Configuration



NOTE: Other First Access Latency Configuration settings are reserved.

Use these equations to calculate First Access Latency Count:

(1) Clock Period (T) = 1 ÷ Frequency

(2) Choose the number of CLK cycles, *n*, such that:
$n \times T \geq t_{AVQV} + t_{ADD\text{-}DELAY} + t_{DATA}$

(3) First Access Latency Count (LC) = n – 2

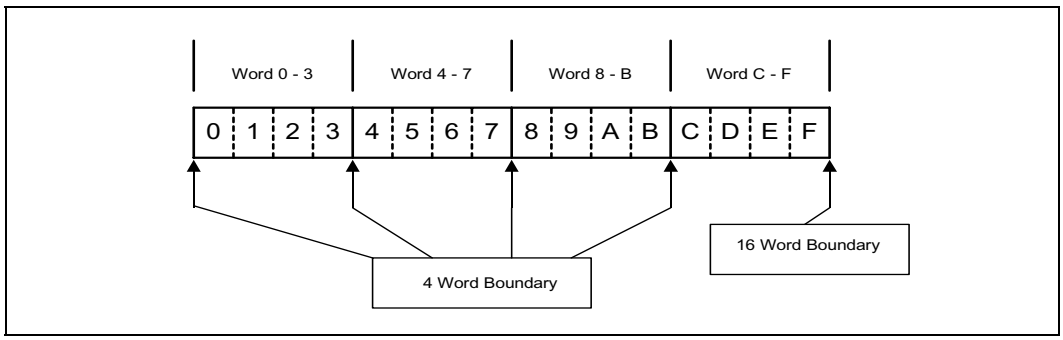
You must use LC = n - 1 when the starting address is **not** aligned to a 4-word boundary and CR[3]=1 (no-wrap).

Table 15. First Latency Count (LC)

LC Setting	Burst Length	Wrap	Aligned to 4-word Boundary?	WAIT Asserted on 16-Word Boundary Crossing?
n–1	4, 8, 16	Disabled	No	Yes, Occurs on Every 16 word boundary crossing
n–2	4, 8, 16	Disabled	Yes	No
n–2	4, 8, 16	Enabled	No	No
n–2	4, 8, 16	Enabled	Yes	No
n–1	Continuous	X	X	Yes, Occurs Once[1]

NOTE: 1. See Section 8.10, "Burst Length (CR[2:0])" on page 53 for details.

Figure 16. Word Boundary



NOTE: The 16-word boundary is the end of the device sense word-line.

Parameters defined by CPU:

$t_{ADD-DELAY}$ = Clock to CE#, ADV#, or Address Valid, whichever occurs last.
t_{DATA} = Data setup to Clock.

Parameters defined by flash:

t_{AVQV} = Address to Output Delay.

Example:

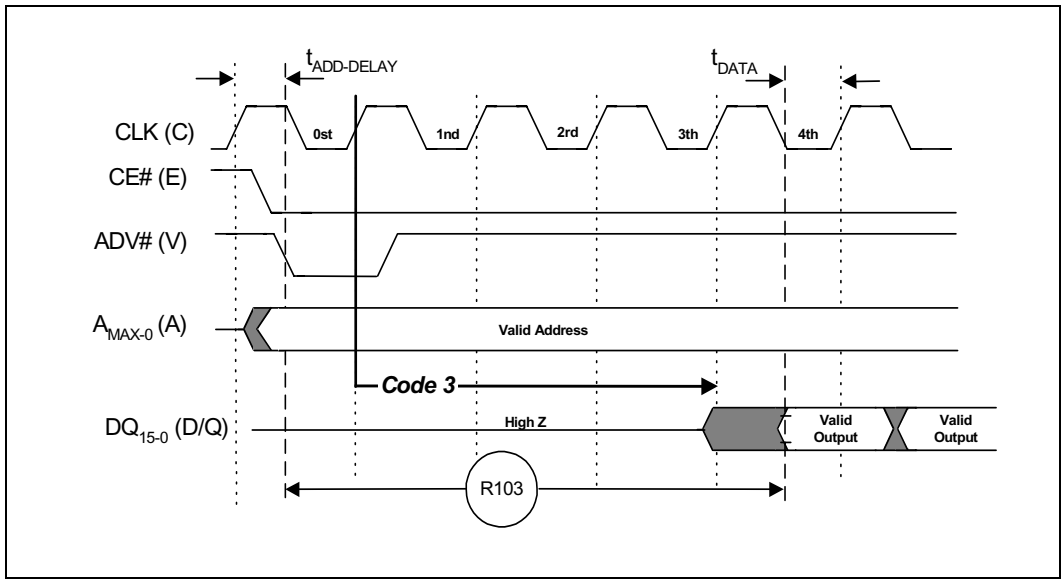
CPU Clock Speed = 66 MHz
$t_{ADD-DELAY}$ = 6 ns (typical speed from CPU) (max)
t_{DATA} = 4 ns (typical speed from CPU) (min)
t_{AVQV} = 60 ns (from AC Characteristic - Read Only Operations Table)
From Eq. (1): 1/66 (MHz) = 15 ns
From Eq. (2) $n(15\ ns) \geq 60\ ns + 6\ ns + 4\ ns$
$n(15\ ns) \geq 70\ ns$
$n \geq 70/15 = 4.67 = 5$ (Integer)
From Eq. (3) n - 2= 5 - 2 = 3 (assuming n-2 is applicable)
First Access Latency Count Setting to the CR is Code 3.

(Figure 17, “Data Output with LC Setting at Code 3” on page 49 displays sample data.)

The formula $t_{AVQV\ (ns)} + t_{ADD\text{-}DELAY}$ (ns) + t_{DATA} (ns) is also known as initial access time.

Figure 17 shows the data output available and valid after four clocks from the assertion of ADV# in the first clock period with the LC setting at 3.

Figure 17. Data Output with LC Setting at Code 3



8.3 WAIT Signal Polarity (CR[10])

If the WT bit is cleared (CR[10]=0), then WAIT is configured to be asserted low. This means that a 0 on the WAIT signal indicates that data is not ready and the data bus contains invalid data. Conversely, if CR[10] is set, then WAIT is asserted high. In either case, if WAIT is deasserted, then data is ready and valid. WAIT is asserted during asynchronous page mode reads.

8.4 WAIT Signal Function

The WAIT signal indicates data valid when the device is operating in synchronous mode (CR[15]=0), and when addressing a partition that is currently in read-array mode. The WAIT signal is only “deasserted” when data is valid on the bus.

When the device is operating in synchronous non-read-array mode, such as read status, read ID, or read query, WAIT is set to an “asserted” state as determined by CR[10]. See Figure 25, “WAIT Signal in Synchronous Non-Read Array Operation Waveform” on page 70.

When the device is operating in asynchronous page mode or asynchronous single word read mode, WAIT is set to an “asserted” state as determined by CR[10]. See Figure 21, “Page-Mode Read Operation Waveform” on page 66, and Figure 19, “Asynchronous Read Operation Waveform” on page 64.

From a system perspective, the WAIT signal is in the asserted state (based on CR[10]) when the device is operating in synchronous non-read-array mode (such as Read ID, Read Query, or Read Status), or if the device is operating in asynchronous mode (CR[15]=1). In these cases, the system software should ignore (mask) the WAIT signal, because it does not convey any useful information about the validity of what is appearing on the data bus.

CONDITION	WAIT
CE# = V_{IH} CE# = V_{IL}	Tri-State Active
OE#	No-Effect
Synchronous Array Read	Active
Synchronous Non-Array Read	Asserted
All Asynchronous Read and all Write	Asserted

8.5 Data Hold (CR[9])

The Data Output Configuration bit (CR[9]) determines whether a data word remains valid on the data bus for one or two clock cycles. The processor's minimum data set-up time and the flash memory's clock-to-data output delay determine whether one or two clocks are needed.

A Data Output Configuration set at 1-clock data hold corresponds to a 1-clock data cycle; a Data Output Configuration set at 2-clock data hold corresponds to a 2-clock data cycle. The setting of this configuration bit depends on the system and CPU characteristics. For clarification, see Figure 18, "Data Output Configuration with WAIT Signal Delay" on page 51.

A method for determining this configuration setting is shown below.

To set the device at 1-clock data hold for subsequent reads, the following condition must be satisfied:

$$t_{CHQV\ (ns)} + t_{DATA}\ (ns) \leq \text{One CLK Period (ns)}$$

As an example, use a clock frequency of 66 MHz and a clock period of 15 ns. Assume the data output hold time is one clock. Apply this data to the formula above for the subsequent reads:

$$11\ ns + 4\ ns \leq 15\ ns$$

This equation is satisfied, and data output will be available and valid at every clock period. If t_{DATA} is long, hold for two cycles.

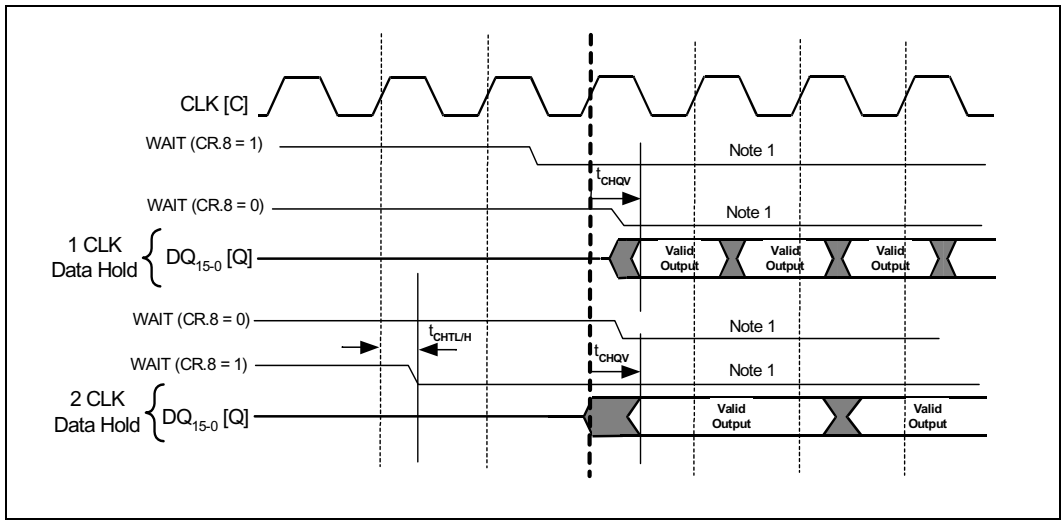
During page-mode reads, the initial access time can be determined by the formula:

$$t_{ADD\text{-}DELAY\ (ns)} + t_{DATA}\ (ns) + t_{AVQV}\ (ns)$$

Subsequent reads in page mode are defined by:

$$t_{APA\ (ns)} + t_{DATA}\ (ns) \qquad \text{(minimum time)}$$

Figure 18. Data Output Configuration with WAIT Signal Delay



NOTE: WAIT shown asserted high (CR[10]=1).

8.6 WAIT Delay (CR[8])

The WAIT configuration bit (CR[8]) controls WAIT signal delay behavior for all synchronous read-array modes. Its setting depends on the system and CPU characteristics. The WAIT can be asserted either during, or one data *cycle* before, a valid output.

In synchronous linear read array (no-wrap mode CR[3]=1) of 4-, 8-, 16-, or continuous-word burst mode, an output delay may occur when a burst sequence crosses its first device-row boundary (16-word boundary). If the burst start address is 4-word boundary aligned, the delay does not occur. If the start address is misaligned to a 4-word boundary, the delay occurs once per burst-mode read sequence. The WAIT signal informs the system of this delay.

8.7 Burst Sequence (CR[7])

The burst sequence specifies the synchronous-burst mode data order (see Table 16, “Sequence and Burst Length” on page 52). Set this bit for linear or Intel burst order. Continuous burst mode supports only linear burst order.

When operating in a linear burst mode, either 4-, 8-, or 16-word burst length with the burst wrap bit (CR[3]) set, or in continuous burst mode, the device may incur an output delay when the burst sequence crosses the first 16-word boundary. (See Figure 16, “Word Boundary” on page 48 for word boundary description.) This depends on the starting address. If the starting address is aligned to a 4-word boundary, there is no delay. If the starting address is the end of a 4-word boundary, the output delay is one clock cycle less than the First Access Latency Count; this is the worst-case delay. The delay takes place only once, and only if the burst sequence crosses a 16-word boundary. The WAIT pin informs the system of this delay. For timing diagrams of WAIT functionality, see these figures:

- Figure 22, “Single Synchronous Read-Array Operation Waveform” on page 67

- Figure 23, “Synchronous 4-Word Burst Read Operation Waveform” on page 68
- Figure 24, “WAIT Functionality for EOWL (End-of-Word Line) Condition Waveform” on page 69

Table 16. Sequence and Burst Length

	Start Addr. (Dec)	Burst Addressing Sequence (Decimal)						
		4-Word Burst CR[2:0]=001b		8-Word Burst CR[2:0]=010b		16-Word Burst CR[2:0]=011b		Continuous Burst CR[2:0]=111b
		Linear	Intel	Linear	Intel	Linear	Intel	Linear
Wrap (CR[3]=0)	0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2...14-15	0-1-2-3-4...14-15	0-1-2-3-4-5-6-...
	1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3...14-15-0	1-0-3-2-5...15-14	1-2-3-4-5-6-7-...
	2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4...15-0-1	2-3-0-1-6...12-13	2-3-4-5-6-7-8-...
	3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5...15-0-1-2	3-2-1-0-7...13-12	3-4-5-6-7-8-9-...
	4			4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3-	4-5-6...15-0-1-2-3	4-5-6-7-0...10-11	4-5-6-7-8-9-10...
	5			5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7...15-0-1...4	5-4-7-6-1...11-10	5-6-7-8-9-10-11...
	6			6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8...15-0-1...5	6-7-4-5-2...8-9	6-7-8-9-10-11-12-...
	7			7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9...15-0-1...6	7-6-5-4-3...9-8	7-8-9-10-11-12-13...
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	14					14-15-0-1...13	14-15-12-13-10...0-1	14-15-16-17-18-19-20-...
	15					15-0-1-2-3...14	15-14-13-12-11...1-0	15-16-17-18-19-...
No-Wrap (CR[3]=1)	0	0-1-2-3	NA	0-1-2-3-4-5-6-7	NA	0-1-2...14-15	NA	0-1-2-3-4-5-6-...
	1	1-2-3-4	NA	1-2-3-4-5-6-7-8	NA	1-2-3...15-16	NA	1-2-3-4-5-6-7-...
	2	2-3-4-5	NA	2-3-4-5-6-7-8-9	NA	2-3-4...16-17	NA	2-3-4-5-6-7-8-...
	3	3-4-5-6	NA	3-4-5-6-7-8-9-10	NA	3-4-5...17-18	NA	3-4-5-6-7-8-9-...
	4			4-5-6-7-8-9-10-11	NA	4-5-6...18-19	NA	4-5-6-7-8-9-10...
	5			5-6-7-8-9-10-11-12	NA	5-6-7...19-20	NA	5-6-7-8-9-10-11...
	6			6-7-8-9-10-11-12-13	NA	6-7-8...20-21	NA	6-7-8-9-10-11-12-...
	7			7-8-9-10-11-12-13-14	NA	7-8-9...21-22	NA	7-8-9-10-11-12-13...
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	14					14-15...28-29	NA	14-15-16-17-18-19-20-...
	15					15-16...29-30	NA	15-16-17-18-19-20-21-...

8.8 Clock Edge (CR[6])

Configuring the valid clock edge enables a flexible memory interface to a wide range of burst CPUs. Clock configuration sets the device to start a burst cycle, output data, and assert WAIT on the clock's rising or falling edge.

8.9 Burst Wrap (CR[3])

The burst wrap bit determines whether 4-, 8-, or 16-word burst accesses wrap within the burst-length boundary or whether they cross word-length boundaries to perform linear accesses. No-wrap mode (CR[3]=1) enables WAIT to hold off the system processor, as it does in the continuous burst mode, until valid data is available. In no-wrap mode (CR[3]=0), the device operates similarly to continuous linear burst mode but consumes less power during 4-, 8-, or 16-word bursts.

For example, if CR[3]=0 (wrap mode) and CR[2:0] = 1h (4-word burst), possible linear burst sequences are 0-1-2-3, 1-2-3-0, 2-3-0-1, 3-0-1-2.

If CR[3]=1 (no-wrap mode) and CR[2:0] = 1h (4-word burst length), then possible linear burst sequences are 0-1-2-3, 1-2-3-4, 2-3-4-5, and 3-4-5-6. CR[3]=1 not only enables limited non-aligned sequential bursts, but also reduces power by minimizing the number of internal read operations.

Setting CR[2:0] bits for continuous linear burst mode (7h) also achieves the above 4-word burst sequences. However, significantly more power may be consumed. The 1-2-3-4 sequence, for example, consumes power during the initial access, again during the internal pipeline lookup as the processor reads word 2, and possibly again, depending on system timing, near the end of the sequence as the device pipelines the next 4-word sequence. CR[3]=1 while in 4-word burst mode (no-wrap mode) reduces this excess power consumption.

8.10 Burst Length (CR[2:0])

The burst length is the number of words the device outputs in a synchronous read access. 4-, 8-, 16-, and continuous-word are supported. In 4-, 8-, or 16-word burst configuration, the burst wrap bit (CR[3]) determines if burst accesses wrap within word-length boundaries or whether they cross word-length boundaries to perform a linear access. Once an address is given, the device outputs data until it reaches the end of its burstable address space. Continuous burst accesses are linear only (burst wrap bit CR[3] is ignored during continuous burst) and do not wrap within word-length boundaries (see Table 16, "Sequence and Burst Length" on page 52).

9.0 Power Consumption

1.8 Volt Intel® Wireless Flash memory devices have a layered approach to power savings that can significantly reduce overall system power consumption. The APS feature reduces power consumption when the device is selected but idle. If CE# is deasserted, the memory enters its standby mode, where current consumption is even lower. Asserting RST# provides current savings similar to standby mode. The combination of these features can minimize memory power consumption, and therefore, overall system power consumption.

9.1 Active Power

With CE# at V_{IL} and RST# at V_{IH}, the device is in the active mode. Refer to Section 10.3, "DC Current Characteristics" on page 57, for I_{CC} values. When the device is in "active" state, it consumes the most power from the system. Minimizing device active current therefore reduces system power consumption, especially in battery-powered applications.

9.2 Automatic Power Savings (APS)

Automatic Power Saving (APS) provides low-power operation during a read's active state. During APS mode, I_{CCAPS} is the average current measured over any 5 ms time interval 5 µs after the following events happen:

- There is no internal sense activity;
- CE# is asserted;
- The address lines are quiescent, and at V_{SSQ} or V_{CCQ}.

OE# may be asserted during APS.

9.3 Standby Power

With CE# at V_{IH} and the device in read mode, the flash memory is in standby mode, which disables most device circuitry and substantially reduces power consumption. Outputs are placed in a high-impedance state independent of the OE# signal state. If CE# transitions to V_{IH} during erase or program operations, the device continues the operation and consumes corresponding active power until the operation is complete. ICCS is the average current measured over any 5 ms time interval 5 µs after a CE# de-assertion.

9.4 Power-Up/Down Characteristics

The device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required if V_{CC}, V_{CCQ}, and V_{PP} are connected together; so it doesn't matter whether V_{PP} or V_{CC} powers-up first. If V_{CCQ} and/or V_{PP} are not connected to the system supply, then V_{CC} should attain V_{CCMIN} before applying VCCQ and VPP. Device inputs should not be driven before supply voltage = V_{CCMIN}. Power supply transitions should only occur when RST# is low.

9.4.1 System Reset and RST#

The use of RST# during system reset is important with automated program/erase devices because the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. To allow proper CPU/flash initialization at system reset, connect RST# to the system CPU RESET# signal.

System designers must guard against spurious writes when VCC voltages are above V_{LKO}. Because both WE# and CE# must be low for a command write, driving either signal to V_{IH} inhibits writes to the device. The CUI architecture provides additional protection because alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until RST# is brought to V_{IH}, regardless of its control input states. By holding the device in reset (RST# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

9.4.2 VCC, VPP, and RST# Transitions

The CUI latches commands issued by system software and is not altered by VPP or CE# transitions or WSM actions. Read-array mode is its power-up default state after exit from reset mode or after VCC transitions above V_{LKO} (Lockout voltage).

After completing program or block erase operations (even after VPP transitions below V_{PPLK}), the Read Array command must reset the CUI to read-array mode if flash memory array access is desired.

9.5 Power Supply Decoupling

When the device is accessed, many internal conditions change. Circuits are enabled to charge pumps and switch voltages. This internal activity produces transient noise. To minimize the effect of this transient noise, device decoupling capacitors are required. Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection suppresses these transient voltage peaks. Each flash device should have a 0.1 µF ceramic capacitor connected between each power (VCC, VCCQ, VPP) and ground (VSS, VSSQ) signal. High-frequency, inherently low-inductance capacitors should be as close as possible to package signals.

10.0 Thermal and DC Characteristics

10.1 Absolute Maximum Ratings

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended, and extended exposure beyond the "Operating Conditions" may affect device reliability.

Notice: This datasheet contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Table 17. Absolute Maximum Ratings

Parameter	Note	Maximum Rating
Temperature under Bias		–40 °C to +85 °C
Storage Temperature		–65 °C to +125 °C
Voltage on Any Pin (except VCC, VCCQ, VPP)		–0.5 V to +2.45 V
VPP Voltage	1,2,3	–0.2 V to +14 V
VCC and VCCQ Voltage	1	–0.2 V to +2.45 V
Output Short Circuit Current	4	100 mA

NOTES:
1. All specified voltages are relative to VSS. Minimum DC voltage is –0.5 V on input/output pins and –0.2 V on VCC and VPP pins. During transitions, this level may undershoot to –2.0 V for periods < 20 ns which, during transitions, may overshoot to V_{CC} +2.0 V for periods < 20 ns.
2. Maximum DC voltage on VPP may overshoot to +14.0 V for periods < 20 ns.
3. V_{PP} program voltage is normally V_{PP1}. V_{PP} can be 12 V ± 0.6 V for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase.
4. Output shorted for no more than one second. No more than one output shorted at a time.

10.2 Operating Conditions

Table 18. Extended Temperature Operation

Symbol	Parameter[1]		Note	Min	Nom	Max	Unit
T_A	Operating Temperature			–40	25	85	°C
V_{CC}	V_{CC} Supply Voltage		3	1.7	1.8	1.95	V
V_{CCQ}	I/O Supply Voltage		3	1.7	1.8	2.24	
	I/O Supply Voltage (Extended)		4	1.35	1.5	1.8	
V_{PP1}	V_{PP} Voltage Supply (Logic Level)		2	0.90	1.80	1.95	
V_{PP2}	Factory Programming V_{PP}		2	11.4	12.0	12.6	
t_{PPH}	Maximum V_{PP} Hours	V_{PP} = 12 V	2			80	Hours
Block Erase Cycles	Main and Parameter Blocks	$V_{PP} \le V_{CC}$	2	100,000			Cycles
	Main Blocks	V_{PP} = 12 V	2			1000	
	Parameter Blocks	V_{PP} = 12 V	2			2500	

NOTES:
1. See Section 10.3, “DC Current Characteristics” on page 57 and Section 10.4, “DC Voltage Characteristics” on page 59 for specific voltage-range specifications.
2. VPP is normally V_{PP1}. VPP can be connected to 11.4 V–12.6 V for 1000 cycles on main blocks for extended temperatures and 2500 cycles on parameter blocks at extended temperature.
3. Contact your Intel field representative for V_{CC}/V_{CCQ} operations down to 1.65 V.
4. See the tables in Section 10.0, “Thermal and DC Characteristics” on page 55 and in Section 11.0, “AC Characteristics” on page 60 for operating characteristics within the Extended-V_{CCQ} voltage range.

10.3 DC Current Characteristics

Table 19. DC Current Characteristics (Sheet 1 of 2)

Sym	Parameter [1]		Note	V_{CCQ}=1.35 V – 1.8 V		V_{CCQ}= 1.8 V				Unit	Test Condition	
				32/64/128 Mbit		32/64 Mbit		128 Mbit				
				Typ	Max	Typ	Max	Typ	Max			
I_{LI}	Input Load		9		TBD		±1		±1	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max V_{IN} = V_{CCQ} or GND	
I_{LO}	Output Leakage	DQ[15:0]			TBD		±1		±1	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max V_{IN} = V_{CCQ} or GND	
I_{CCS}	V_{CC} Standby		10	TBD	TBD	5	18	5	25	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max CE# = V_{CC} RST# =V_{CC} or GND	
I_{CCAPS}	APS		11	TBD	TBD	5	18	5	25	µA	V_{CC} = V_{CC}Max V_{CCQ} = V_{CCQ}Max CE# = V_{SSQ} RST# =V_{CCQ} All other inputs =V_{CCQ} or V_{SSQ}	
I_{CCR}	Average V_{CC} Read	Asynchronous Page Mode f=13 MHz	2	TBD	TBD	3	6	4	7	mA	4 Word Read	V_{CC} = V_{CC}Max CE# = V_{IL} OE# = V_{IH} Inputs = V_{IH} or V_{IL}
		Synchronous CLK = 40 MHz	2	TBD	TBD	6	13	6	13	mA	Burst length = 4	
				TBD	TBD	8	14	8	14	mA	Burst length = 8	
				TBD	TBD	10	18	11	19	mA	Burst length =16	
				TBD	TBD	11	20	11	20	mA	Burst length = Continuous	
		Synchronous CLK = 54 MHz	2	TBD	TBD	7	16	7	16	mA	Burst length = 4	
				TBD	TBD	10	18	10	18	mA	Burst length = 8	
				TBD	TBD	12	22	12	22	mA	Burst length = 16	
				TBD	TBD	13	25	13	25	mA	Burst length = Continuous	

Table 19. DC Current Characteristics (Sheet 2 of 2)

Sym	Parameter [1]		Note	V_{CCQ}=1.35 V – 1.8 V		V_{CCQ}= 1.8 V				Unit	Test Condition	
				32/64/128 Mbit		32/64 Mbit		128 Mbit				
				Typ	Max	Typ	Max	Typ	Max			
I_{CCR}	Average V_{CC} Read	Synchronous CLK = 66 MHz	2, 3	TBD	TBD	8	17	N.A.	N.A.	mA	Burst length = 4	V_{CC} = V_{CC}Max CE# = V_{IL} OE# = V_{IH} Inputs = V_{IH} or V_{IL}
				TBD	TBD	11	20	N.A.	N.A.	mA	Burst length = 8	
				TBD	TBD	14	25	N.A.	N.A.	mA	Burst length = 16	
				TBD	TBD	16	30	N.A.	N.A.	mA	Burst length = Continuous	
I_{CCW}	V_{CC} Program		3,4,5	TBD	TBD	18	40	18	40	mA	V_{PP} = V_{PP1}, Program in Progress	
				TBD	TBD	8	15	8	15	mA	V_{PP} = V_{PP2}, Program in Progress	
I_{CCE}	V_{CC} Block Erase		3,4,5	TBD	TBD	18	40	18	40	mA	V_{PP} = V_{PP1}, Block Erase in Progress	
				TBD	TBD	8	15	8	15	mA	V_{PP} = V_{PP2}, Block Erase in Progress	
I_{CCWS}	V_{CC} Program Suspend		6	TBD	TBD	5	18	5	25	µA	CE# = V_{CC}, Program Suspended	
I_{CCES}	V_{CC} Erase Suspend		6	TBD	TBD	5	18	5	25	µA	CE# = V_{CC}, Erase Suspended	
I_{PPS} (I_{PPWS} I_{PPES})	V_{PP} Standby V_{PP} Program Suspend V_{PP} Erase Suspend		3	TBD	TBD	0.2	5	0.2	5	µA	$V_{PP} \leq V_{CC}$	
I_{PPR}	V_{PP} Read			TBD	TBD	2	15	2	15	µA	$V_{PP} \leq V_{CC}$	
I_{PPW}	V_{PP} Program		4	TBD	TBD	0.05	0.10	0.05	0.10	mA	V_{PP} = V_{PP1}, Program in Progress	
				TBD	TBD	8	22	16	37		V_{PP} = V_{PP2}, Program in Progress	
I_{PPE}	V_{PP} Erase		4	TBD	TBD	0.05	0.10	0.05	0.10	mA	V_{PP} = V_{PP1}, Erase in Progress	
				TBD	TBD	8	22	8	22		V_{PP} = V_{PP2}, Erase in Progress	

NOTES:
1. All currents are RMS unless noted. Typical values at typical V_{CC}, T_A = +25°C.
2. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation. See I_{CCRQ} specification for details.
3. Sampled, not 100% tested.
4. V_{CC} read + program current is the sum of V_{CC} read and V_{CC} program currents.
5. V_{CC} read + erase current is the sum of V_{CC} read and V_{CC} erase currents.
6. I_{CCES} is specified with device deselected. If device is read while in erase suspend, current is I_{CCES} plus I_{CCR}.
7. V_{PP} <= V_{PPLK} inhibits erase and program operations. Don't use V_{PPL} and V_{PPH} outside their valid ranges.
8. V_{IL} can undershoot to –0.4V and V_{IH} can overshoot to V_{CCQ}+0.4V for durations of 20 ns or less.
9. If V_{IN}>V_{CC} the input load current increases to 10 µA max.

10. ICCS is the average current measured over any 5ms time interval 5µs after a CE# de-assertion.
11. Refer to section Section 9.2, "Automatic Power Savings (APS)" on page 54 for I_{CCAPS} measurement details.
12. TBD values are to be determined pending silicon characterization.

10.4 DC Voltage Characteristics

Table 20. DC Voltage Characteristics

Sym	Parameter (1)	Note	V_{CCQ}=1.35 V – 1.8 V		V_{CCQ}= 1.8 V				Unit	Test Condition
			32/64/128 Mbit		32/64 Mbit		128 Mbit			
			Min	Max	Min	Max	Min	Max		
V_{IL}	Input Low	8	0	0.2	0	0.4	0	0.4	V	
V_{IH}	Input High		V_{CCQ} – 0.2	V_{CCQ}	V_{CCQ} – 0.4	V_{CCQ}	V_{CCQ} – 0.4	V_{CCQ}	V	
V_{OL}	Output Low			0.1		0.1		0.1	V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ}Min I_{OL} = 100 µA
V_{OH}	Output High		V_{CCQ} – 0.1		V_{CCQ} – 0.1		V_{CCQ} – 0.1		V	V_{CC} = V_{CC}Min V_{CCQ} = V_{CCQ}Min I_{OH} = –100 µA
V_{PPLK}	V_{PP} Lock-Out	7	0.4			0.4		0.4	V	
V_{LKO}	V_{CC} Lock		1.0		1.0		1.0		V	
V_{ILKOQ}	V_{CCQ} Lock		TBD		0.9		0.9		V	

NOTE: For all numbered note references in this table, refer to the notes in Table 19, "DC Current Characteristics" on page 57.

11.0 AC Characteristics

11.1 Read Operations – .13 µm Lithography

Table 21. Read Operations— .13 µm Lithography (Sheet 1 of 2)

#	Sym	Parameter [1,2]	Notes	V_{CCQ}= 1.35 V – 1.8 V				V_{CCQ}= 1.7 V – 2.24 V				Unit
				-65		-85		-60		-80		
				Min	Max	Min	Max	Min	Max	Min	Max	
Asynchronous Specifications												
R1	t_{AVAV}	Read Cycle Time	7,8	65		85		60		80		ns
R2	t_{AVQV}	Address to Output Valid	7,8		65		85		60		80	ns
R3	t_{ELQV}	CE# Low to Output Valid	7,8		65		85		60		80	ns
R4	t_{GLQV}	OE# Low to Output Valid	4		25		30		20		25	ns
R5	t_{PHQV}	RST# High to Output Valid			150		150		150		150	ns
R6	t_{ELQX}	CE# Low to Output Low-Z	5	0		0		0		0		ns
R7	t_{GLQX}	OE# Low to Output Low-Z	4,5	0		0		0		0		ns
R8	t_{EHQZ}	CE# High to Output High-Z	5		17		20		14		17	ns
R9	t_{GHQZ}	OE# High to Output High-Z	4,5		14		14		14		14	ns
R10	t_{OH}	CE# (OE#) High to Output Low-Z	4,5	0		0		0		0		ns
Latching Specifications												
R101	t_{AVVH}	Address Setup to ADV# High		7		7		7		7		ns
R102	t_{ELVH}	CE# Low to ADV# High		10		10		10		10		ns
R103	t_{VLQV}	ADV# Low to Output Valid	7,8		65		85		60		80	ns
R104	t_{VLVH}	ADV# Pulse Width Low		7		7		7		7		ns
R105	t_{VHVL}	ADV# Pulse Width High		7		7		7		7		ns
R106	t_{VHAX}	Address Hold from ADV# High	3	7		7		7		7		ns
R108	t_{APA}	Page Address Access Time			25		30		20		25	ns
Clock Specifications												
R200	f_{CLK}	CLK Frequency			54		40		66		54	MHz
R201	t_{CLK}	CLK Period		18.5		25		15		18.5		ns
R202	$t_{CH/L}$	CLK High or Low Time		4.5		9.5		3.5		4.5		ns
R203	t_{CHCL}	CLK Fall or Rise Time			3		3		3		3	ns

Table 21. Read Operations— .13 µm Lithography (Sheet 2 of 2)

#	Sym	Parameter [1,2]	Notes	V_{CCQ}= 1.35 V – 1.8 V				V_{CCQ}= 1.7 V – 2.24 V				Unit
				-65		-85		-60		-80		
				Min	Max	Min	Max	Min	Max	Min	Max	
Synchronous Specifications												
R301	t_{AVCH}	Address Valid Setup to CLK		7		7		7		7		ns
R302	t_{VLCH}	ADV# Low Setup to CLK		7		7		7		7		ns
R303	t_{ELCH}	CE# Low Setup to CLK		7		7		7		7		ns
R304	t_{CHQV}	CLK to Output Valid	8		14		20		11		14	ns
R305	t_{CHQX}	Output Hold from CLK		3		3		3		3		ns
R306	t_{CHAX}	Address Hold from CLK	3	7		7		7		7		ns
R307	t_{CHTV}	CLK to WAIT Valid	8		14		20		11		14	ns
R308	t_{ELTV}	CE# Low to WAIT Valid	6		14		20		11		14	ns
R309	t_{EHTZ}	CE# High to WAIT High-Z	5,6		14		20		11		14	ns
R310	t_{EHEL}	CE# Pulse Width High	6	14		14		14		14		ns

11.2 Read Operations – .18 µm Lithography

Table 22. Read Operations — .18 µm Lithography (Sheet 1 of 2)

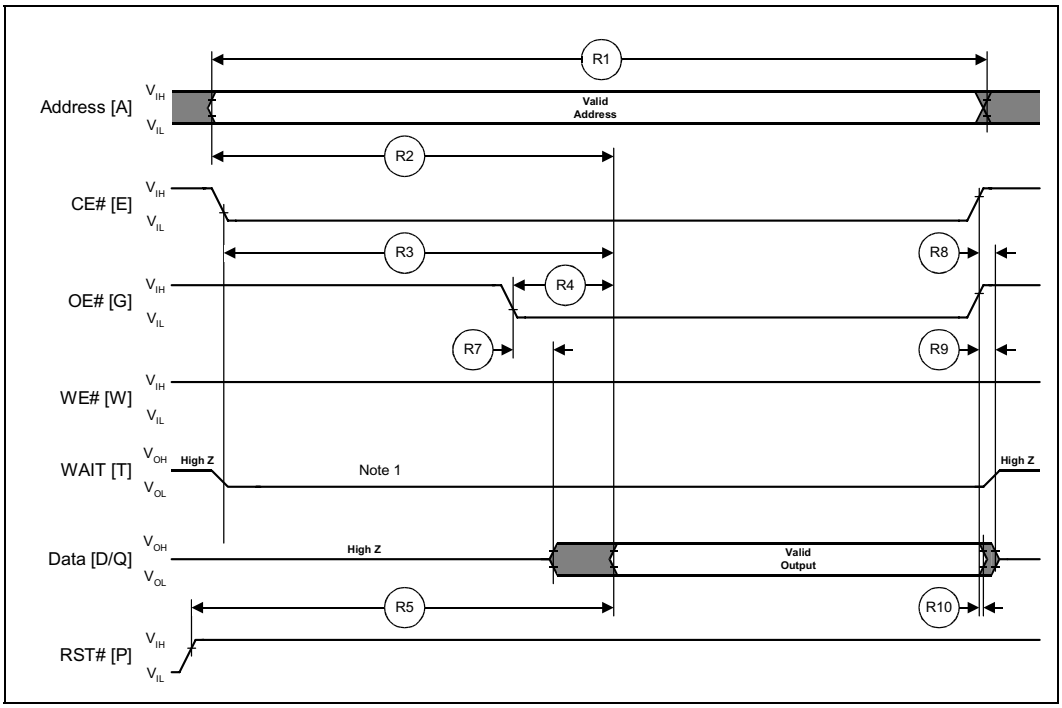
#	Sym	Parameter [1,2]	Notes	32/64 Mbit				128 Mbit		Unit
				–70		–85		-85		
				Min	Max	Min	Max	Min	Max	
Asynchronous Specifications										
R1	t_{AVAV}	Read Cycle Time		70		85		85		ns
R2	t_{AVQV}	Address to Output Delay			70		85		85	ns
R3	t_{ELQV}	CE# Low to Output Delay			70		85		85	ns
R4	t_{GLQV}	OE# Low to Output Delay	4		30		30		30	ns
R5	t_{PHQV}	RST# High to Output Delay			150		150		150	ns
R6	t_{ELQX}	CE# Low to Output in Low-Z	5	0		0		0		ns
R7	t_{GLQX}	OE# Low to Output in Low-Z	4,5	0		0		0		ns
R8	t_{EHQZ}	CE# High to Output in High-Z	5		20		20		20	ns
R9	t_{GHQZ}	OE# High to Output in High-Z	4,5		14		14		14	ns
R10	t_{OH}	CE# (OE#) High to Output in Low-Z	4,5	0		0		0		ns
Latching Specifications										
R101	t_{AVVH}	Address Setup to ADV# High		10		10		10		ns
R102	t_{ELVH}	CE# Low to ADV# High		10		10		10		ns
R103	t_{VLQV}	ADV# Low to Output Delay			70		85		85	ns
R104	t_{VLVH}	ADV# Pulse Width Low		10		10		10		ns
R105	t_{VHVL}	ADV# Pulse Width High		10		10		10		ns
R106	t_{VHAX}	Address Hold from ADV# High	3	9		9		9		ns
R108	t_{APA}	Page Address Access Time			20		25		25	ns
Clock Specifications										
R200	f_{CLK}	CLK Frequency			52		40		40	MHz
R201	t_{CLK}	CLK Period		19		25		25		ns
R202	$t_{CH/L}$	CLK High or Low Time		5		5		5		ns
R203	t_{CHCL}	CLK Fall or Rise Time			3		3		3	ns

Table 22. Read Operations — .18 µm Lithography (Sheet 2 of 2)

#	Sym	Parameter (1,2)	Notes	32/64 Mbit				128 Mbit		Unit
				–70		–85		-85		
				Min	Max	Min	Max	Min	Max	
Synchronous Specifications										
R301	t_{AVCH}	Address Valid Setup to CLK		9		9		9		ns
R302	t_{VLCH}	ADV# Low Setup to CLK		10		10		10		ns
R303	t_{ELCH}	CE# Low Setup to CLK		9		9		9		ns
R304	t_{CHQV}	CLK to Output Valid			14		18		18	ns
R305	t_{CHQX}	Output Hold from CLK		3.5		3.5		3.5		ns
R306	t_{CHAX}	Address Hold from CLK	3	10		10		10		ns
R307	t_{CHTV}	CLK to WAIT Valid			14		18		18	ns
R308	t_{ELTV}	CE# Low to WAIT Valid	6		14		18		18	ns
R309	t_{EHTZ}	CE# High to WAIT High-Z	5,6		20		25		25	ns
R310	t_{EHEL}	CE# Pulse Width High	6	15		20		20		ns

NOTES:
1. See Figure 33, “AC Input/Output Reference Waveform” on page 78 for timing measurements and maximum allowable input slew rate.
2. AC specifications assume the data bus voltage is less than or equal to V_{CCQ} when a read operation is initiated.
3. Address hold in synchronous-burst mode is defined as t_{CHAX} or t_{VHAX}, whichever timing specification is satisfied first.
4. OE# may be delayed by up to t_{ELQV}– t_{GLQV} after the falling edge of CE# without impact to t_{ELQV}.
5. Sampled, not 100% tested.
6. Applies only to subsequent synchronous reads.
7. During the initial access of a synchronous burst read, data from the first word may begin to be driven onto the data bus as early as the first clock edge after t_{AVQV}.
8. All specs above apply to all densities.

Figure 19. Asynchronous Read Operation Waveform



NOTES:.
1. WAIT shown asserted (CR.10=0)
2. ADV# assumed to be driven to VIL in this waveform

Figure 20. Latched Asynchronous Read Operation Waveform

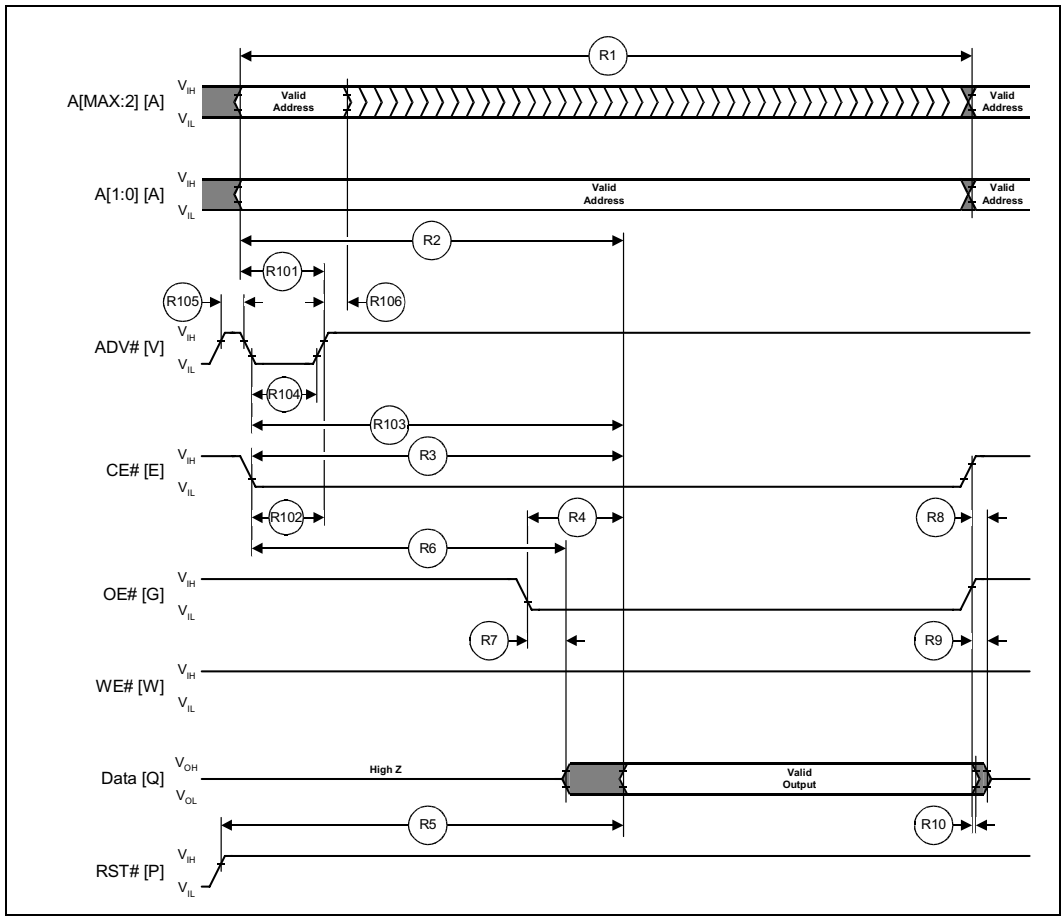
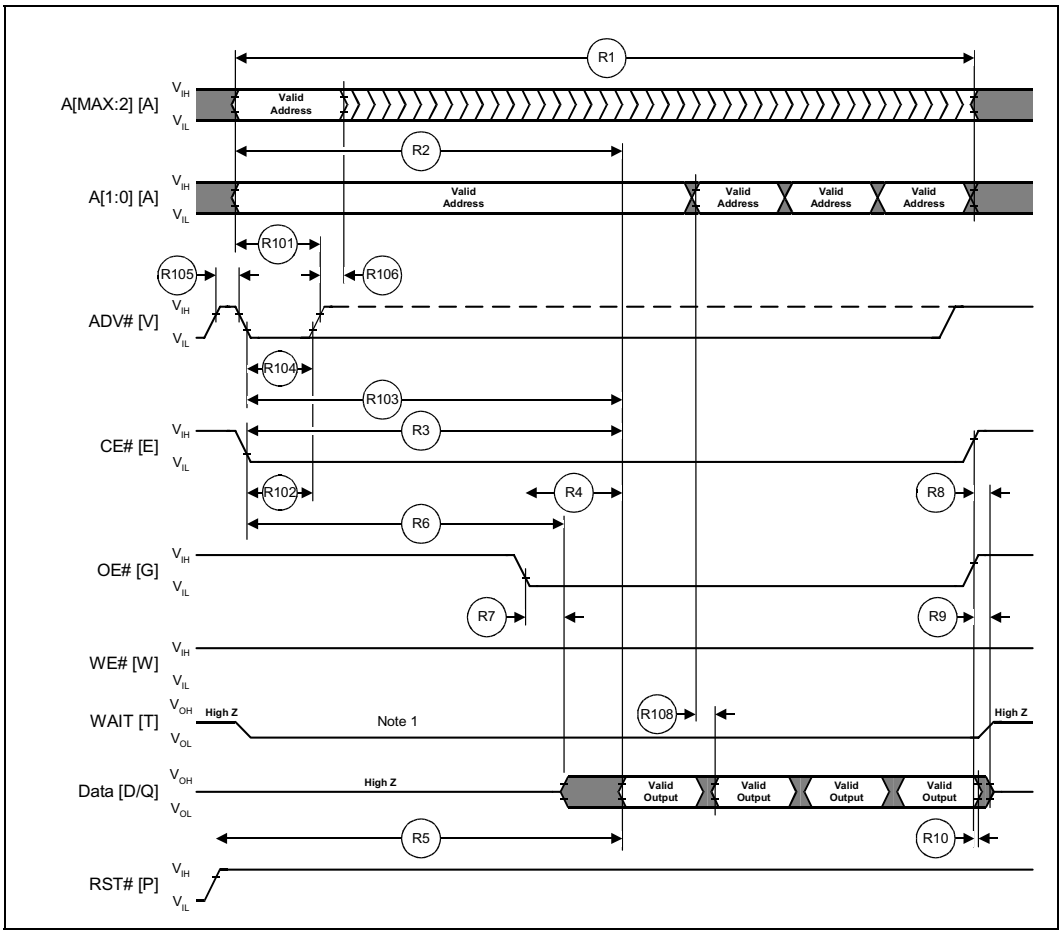
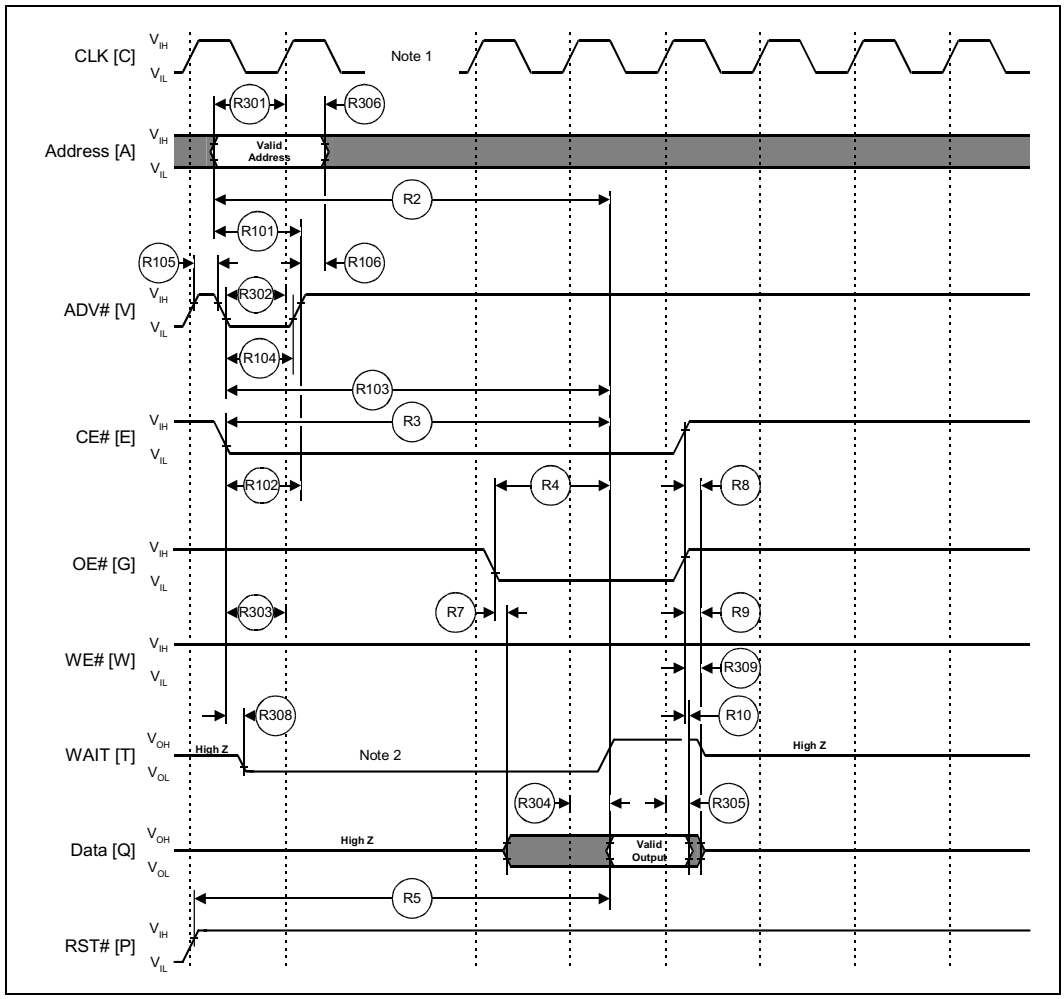


Figure 21. Page-Mode Read Operation Waveform



NOTE: WAIT shown asserted (CR.10 = 0).

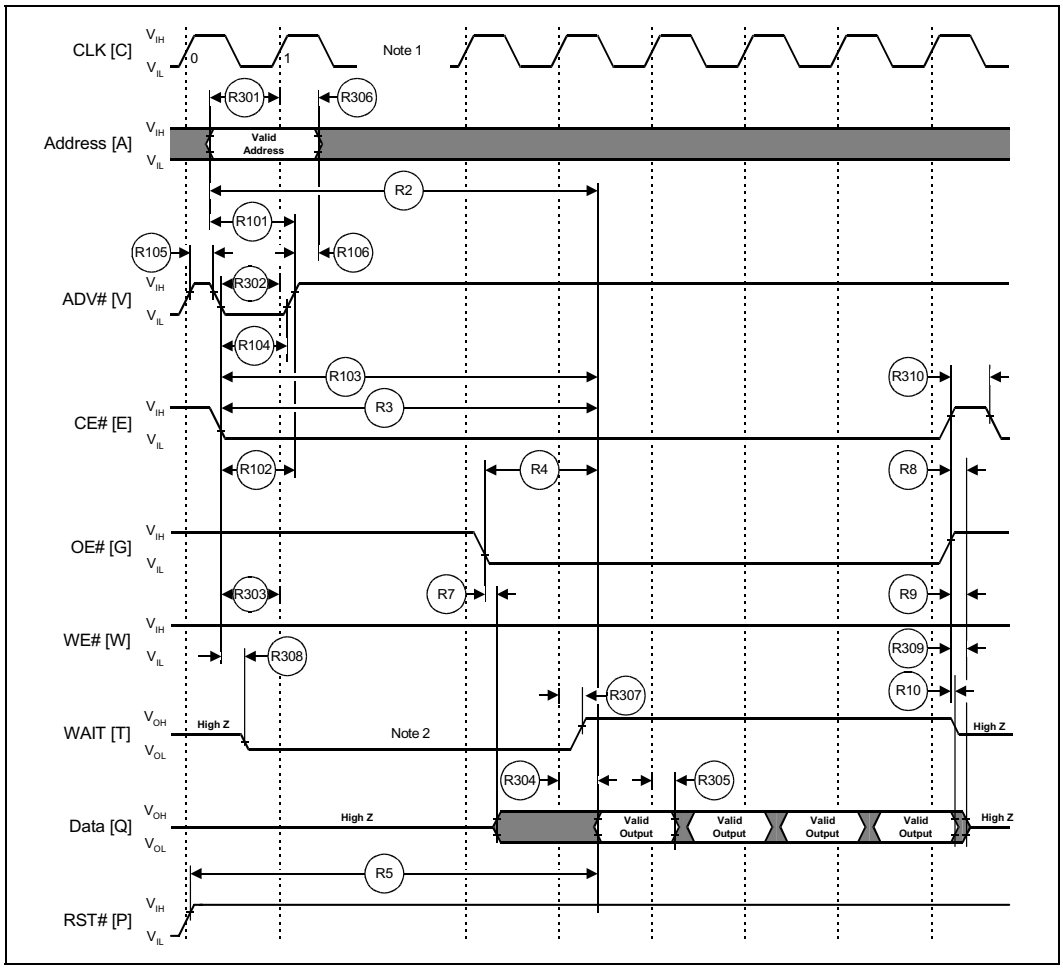
Figure 22. Single Synchronous Read-Array Operation Waveform



NOTES:

1. Section 8.2, "First Access Latency Count (CR[13:11])" on page 47 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; CR.10=0) can be configured to assert either during, or one data cycle before, valid data.
3. This waveform illustrates the case in which an x-word burst is initiated to the main array and it is terminated by a CE# de-assertion after the first word in the burst. If this access had been done to Status, ID, or Query reads, the asserted (low) WAIT signal would have remained asserted (low) as long as CE# is asserted (low).

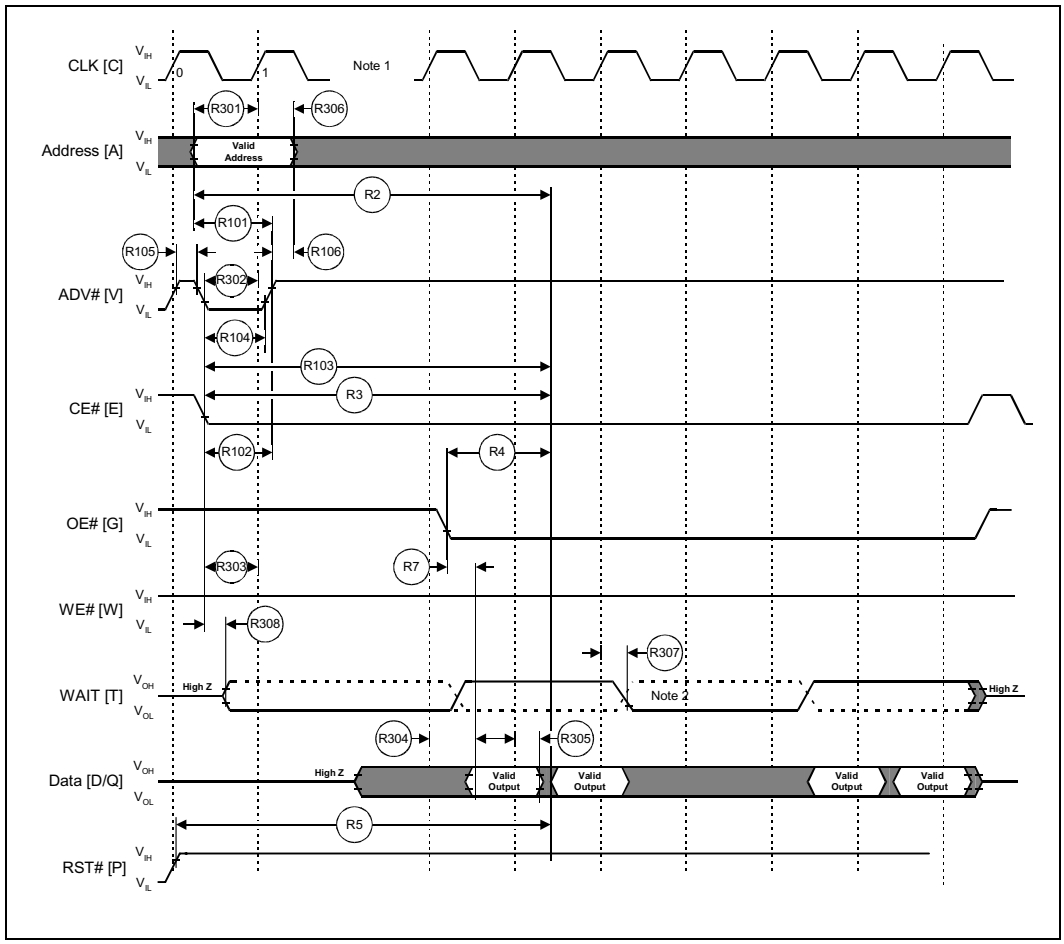
Figure 23. Synchronous 4-Word Burst Read Operation Waveform



NOTES:

1. Section 8.2, "First Access Latency Count (CR[13:11])" on page 47 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; CR.10 = 0) can be configured to assert either during, or one data cycle before, valid data.

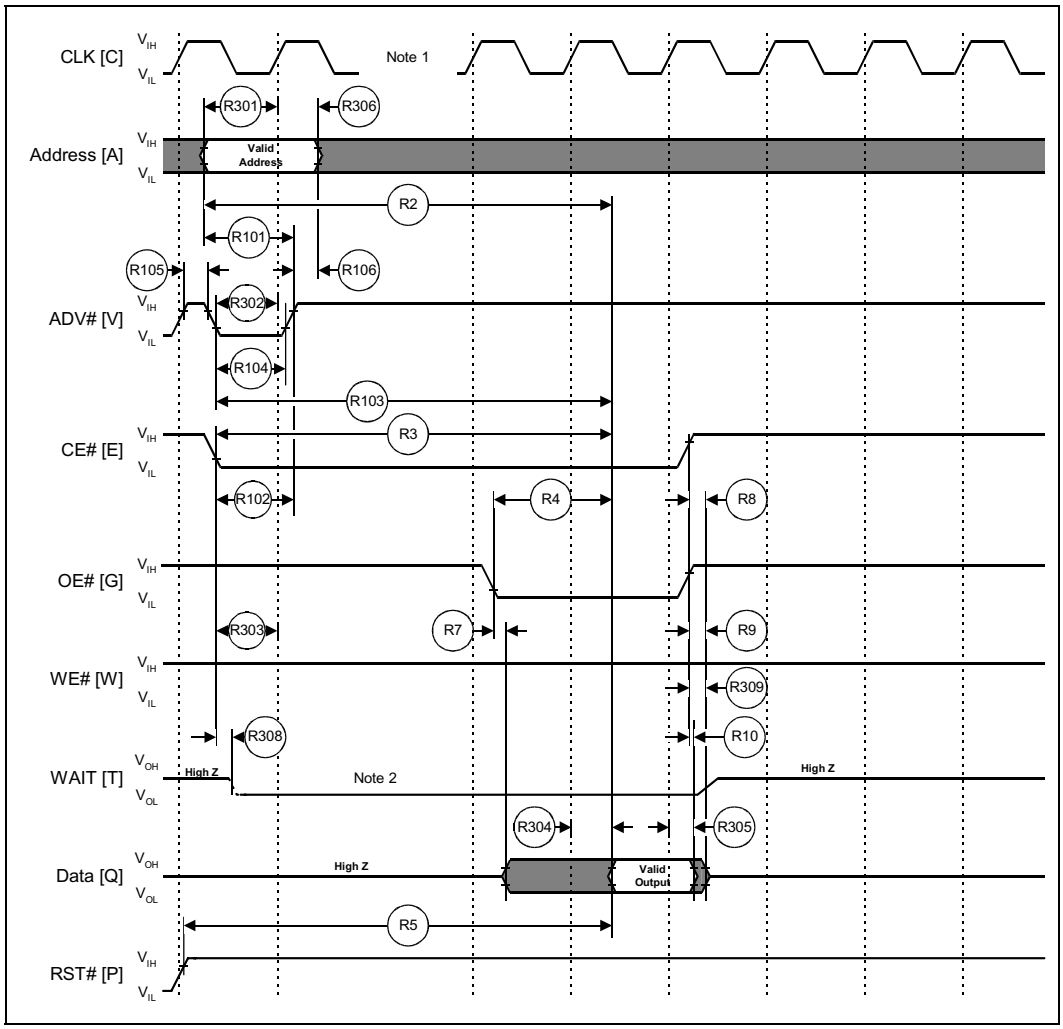
Figure 24. WAIT Functionality for EOWL (End-of-Word Line) Condition Waveform



NOTES:

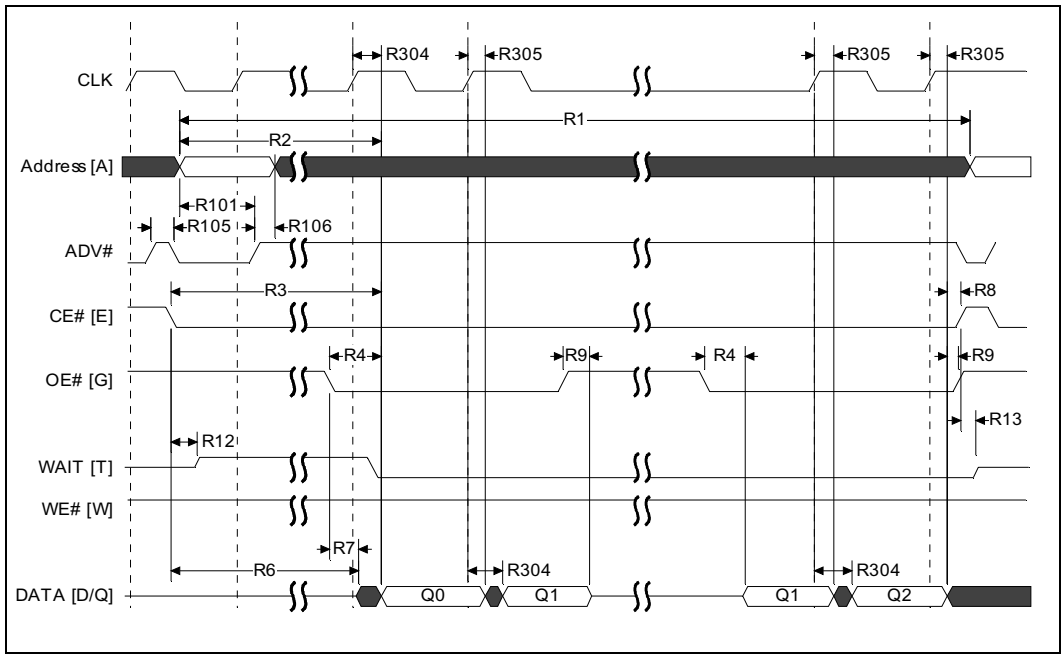
1. Section 8.2, “First Access Latency Count (CR[13:11])” on page 47 describes how to insert clock cycles during the initial access.
2. WAIT (shown asserted; CR.10=0) can be configured to assert either during, or one data cycle before, valid data. (assumed wait delay of two clocks for example)

Figure 25. WAIT Signal in Synchronous Non-Read Array Operation Waveform



NOTES:
1. Section 8.2, "First Access Latency Count (CR[13:11])" on page 47 describes how to insert clock cycles during the initial access.
2. WAIT shown asserted (CR.10=0).

Figure 26. Burst Suspend



NOTE:
1. During Burst Suspend Clock signal can be held high or low

11.3 AC Write Characteristics

Table 23. AC Write Characteristics

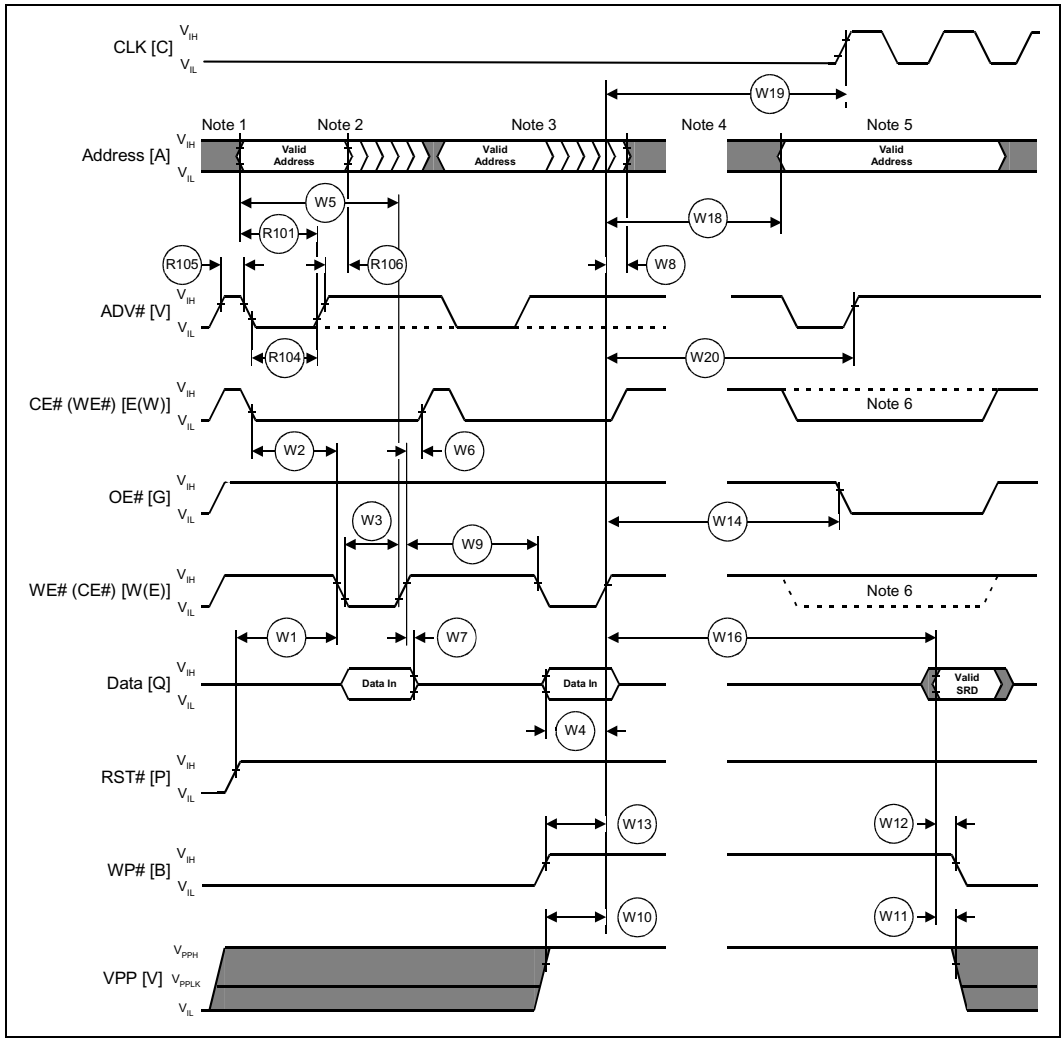
#	Sym	Parameter [1,2]	Notes	V_{CCQ}= 1.35 V – 1.8 V				V_{CCQ}= 1.7 V – 2.24 V				Unit
				-65		-85		-60		-80		
				Min	Max	Min	Max	Min	Max	Min	Max	
W1	t_{PHWL} (t_{PHEL})	RST# High Recovery to WE# (CE#) Low	3	150		150		150		150		ns
W2	t_{ELWL} (t_{WLEL})	CE# (WE#) Setup to WE# (CE#) Low		0		0		0		0		ns
W3	t_{WLWH} (t_{ELEH})	WE# (CE#) Write Pulse Width Low	4	50		60		40		60		ns
W4	t_{DVWH} (t_{DVEH})	Data Setup to WE# (CE#) High		50		60		40		60		ns
W5	t_{AVWH} (t_{AVEH})	Address Setup to WE# (CE#) High		50		60		40		60		ns
W6	t_{WHEH} (t_{EHWH})	CE# (WE#) Hold from WE# (CE#) High		0		0		0		0		ns
W7	t_{WHDX} (t_{EHDX})	Data Hold from WE# (CE#) High		0		0		0		0		ns
W8	t_{WHAX} (t_{EHAX})	Address Hold from WE# (CE#) High		0		0		0		0		ns
W9	t_{WHWL} (t_{EHEL})	WE# (CE#) Pulse Width High	5,6,7	20		25		20		25		ns
W10	t_{VPWH} (t_{VPEH})	VPP Setup to WE# (CE#) High	3	200		200		200		200		ns
W11	t_{QVVL}	VPP Hold from Valid SRD	3,8	0		0		0		0		ns
W12	t_{QVBL}	WP# Hold from Valid SRD	3,8	0		0		0		0		ns
W13	t_{BHWH} (t_{BHEH})	WP# Setup to WE# (CE#) High	3	200		200		200		200		ns
W14	t_{WHGL} (t_{EHGL})	Write Recovery before Read		0		0		0		0		ns
W16	t_{WHQV}	WE# High to Valid Data	3,6,10	t_{AVQV} + 25		t_{AVQV} + 55		t_{AVQV} +20		t_{AVQV} +50		ns
W18	t_{WHAV}	WE# High to Address Valid	3,9,10	0		0		0		0		ns
W19	t_{WHCV}	WE# High to CLK Valid	3,10	16		20		12		20		ns
W20	t_{WHVH}	WE# High to ADV# High	3,10	16		20		12		20		ns

NOTES:
1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. A write operation can be terminated with either CE# or WE#.
3. Sampled, not 100% tested.
4. Write pulse width low (t_{WLWH} or t_{ELEH}) is defined from CE# or WE# low (whichever occurs last) to CE# or WE# high (whichever occurs first). Hence, $t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$.
5. Write pulse width high (t_{WHWL} or t_{EHEL}) is defined from CE# or WE# high (whichever is first) to CE# or WE# low (whichever is last). Hence, $t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.

6. System designers should take this into account and may insert a software No-Op instruction to delay the first read after issuing a command.
7. For commands other than resume commands.
8. V_{PP} should be held at V_{PP1} or V_{PP2} until block erase or program success is determined.
9. Applicable during asynchronous reads following a write.
10. $t_{WHCH/L}$ OR t_{WHVH} must be met when transitioning from a write cycle to a synchronous burst read. $t_{WHCH/L}$ and t_{WHVH} both refer to the address latching event (either the rising/falling clock edge or the rising ADV# edge, whichever occurs first).

NOTES:

Figure 27. Write Operations Waveform



NOTES:

1. V_{CC} power-up and standby.
2. Write Program or Erase Setup command.
3. Write valid address and data (for program) or Erase Confirm command.
4. Automated program/erase delay.
5. Read status register data (SRD) to determine program/erase operation completion.
6. OE# and CE# must be asserted and WE# must be deasserted for read operations.
7. CLK is ignored. (but may be kept active/toggling)

Figure 28. Asynchronous Read to Write Operation Waveform

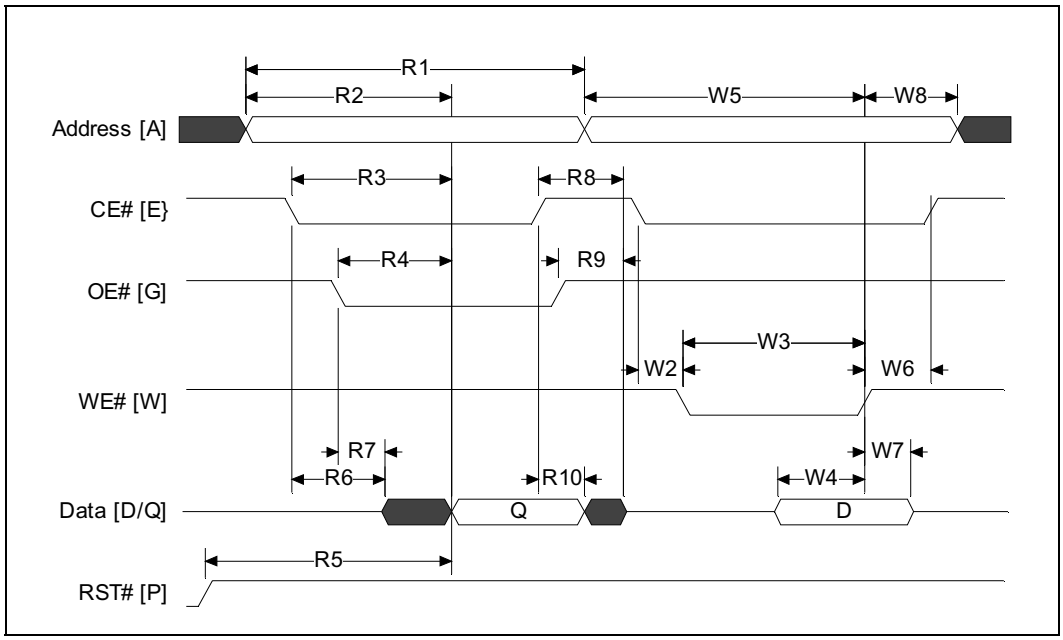


Figure 29. Asynchronous Write to Read Operation

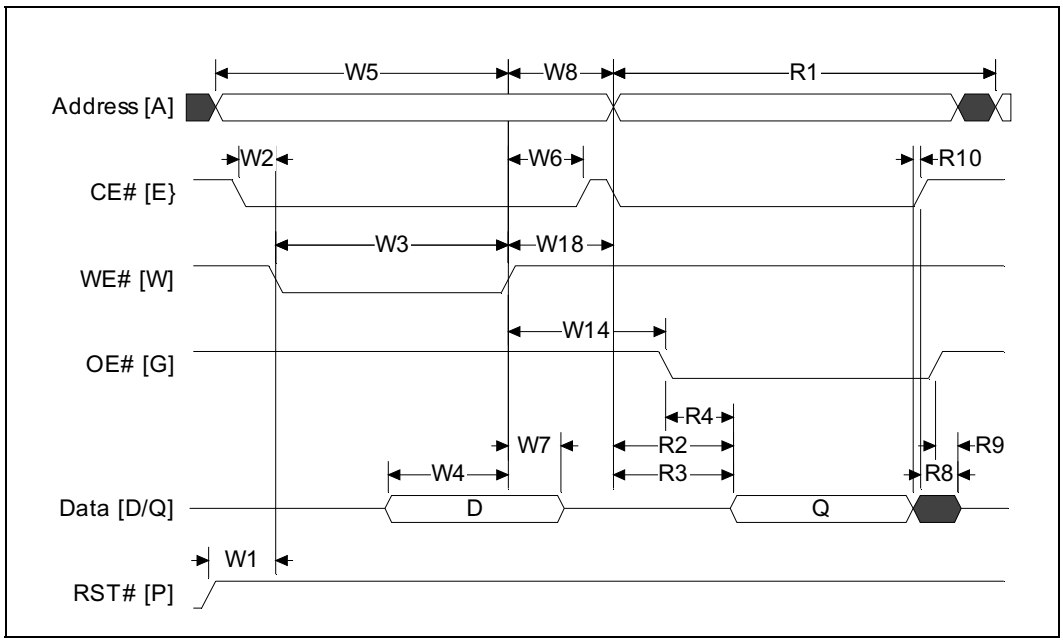


Figure 30. Synchronous Read to Write Operation

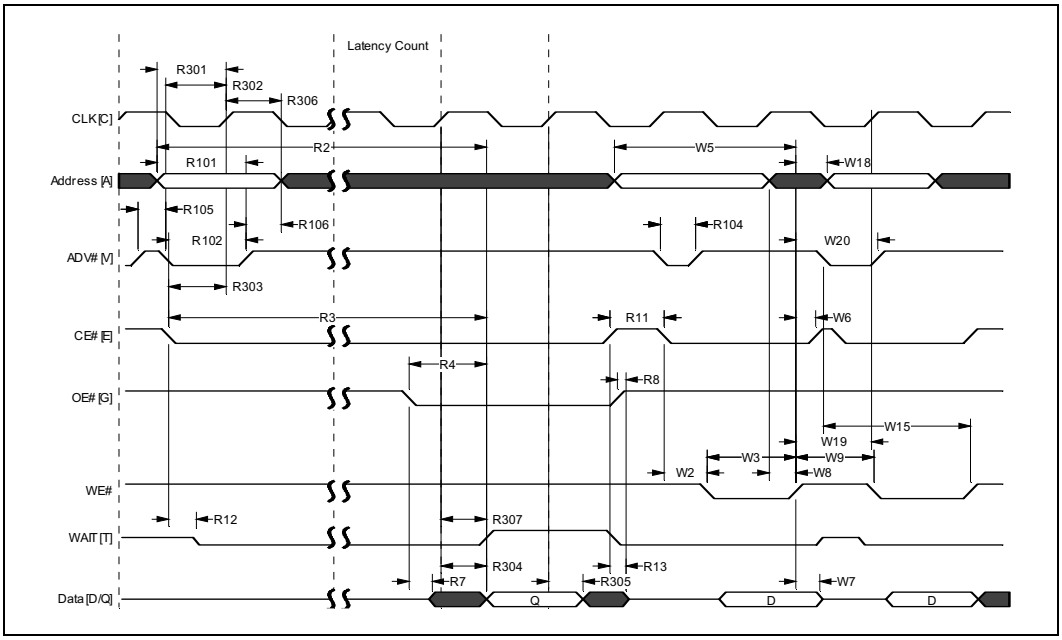
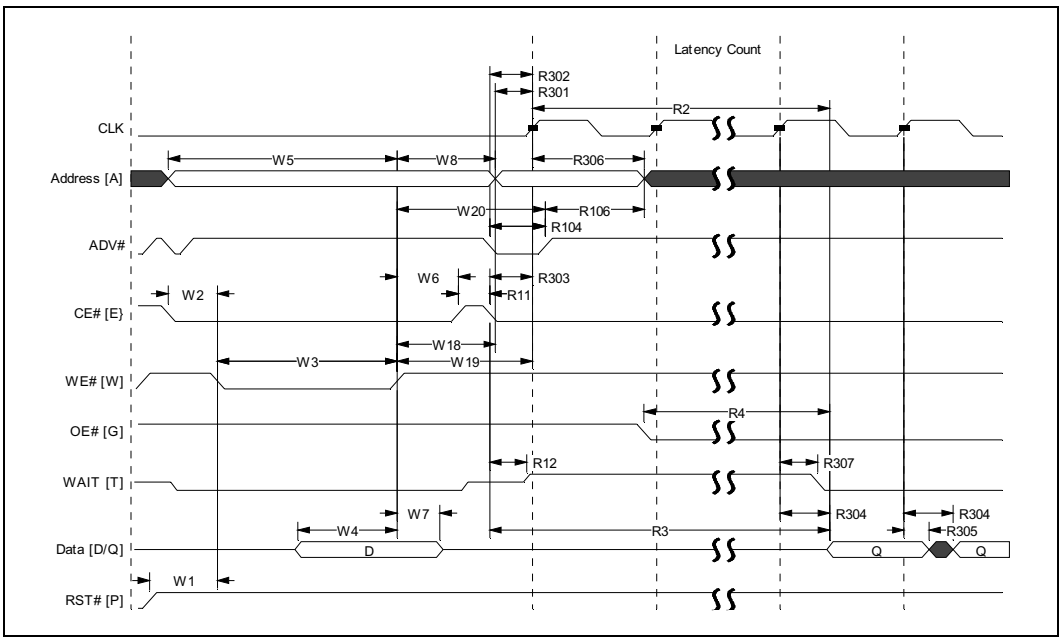


Figure 31. Synchronous Write To Read Operation



11.4 Erase and Program Times

Table 24. Erase and Program Times

Operation	Symbol	Parameter	Description[1]	Notes	V_{PP1}		V_{PP2}		Unit
					Typ	Max	Typ	Max	
Erasing and Suspending									
Erase Time	W500	tERS/PB	4-Kword Parameter Block	2,3	0.3	2.5	0.25	2.5	s
	W501	$t_{ERS/MB}$	32-Kword Main Block	2,3	0.7	4	0.4	4	s
Suspend Latency	W600	$t_{SUSP/P}$	Program Suspend	2	5	10	5	10	µs
	W601	$t_{SUSP/E}$	Erase Suspend	2	5	20	5	20	µs
Programming									
Program Time	W200	tPROG/W	Single Word	2	12	150	8	130	µs
	W201	tPROG/PB	4-Kword Parameter Block	2,3	0.05	.23	0.03	0.07	s
	W202	tPROG/MB	32-Kword Main Block	2,3	0.4	1.8	0.24	0.6	s
Enhanced Factory Programming[5]									
Program	W400	tEFP/W	Single Word	4	N/A	N/A	3.1	16	µs
	W401	tEFP/PB	4-Kword Parameter Block	2,3	N/A		15		ms
	W402	tEFP/MB	32-Kword Main Block	2,3	N/A		120		ms
Operation Latency	W403	$t_{EFP/SETUP}$	EFP Setup			N/A		5	µs
	W404	$t_{EFP/TRAN}$	Program to Verify Transition		N/A	N/A	2.7	5.6	µs
	W405	$t_{EFP/VERIFY}$	Verify		N/A	N/A	1.7	130	µs

NOTES:
1. Unless noted otherwise, all parameters are measured at T_A = +25 °C and nominal voltages, and they are sampled, not 100% tested.
2. Excludes external system-level overhead.
3. Exact results may vary based on system overhead.
4. W400-Typ is the calculated delay for a single programming pulse. W400-Max includes the delay when programming within a new word-line.
5. Some EFP performance degradation may occur if block cycling exceeds 10.

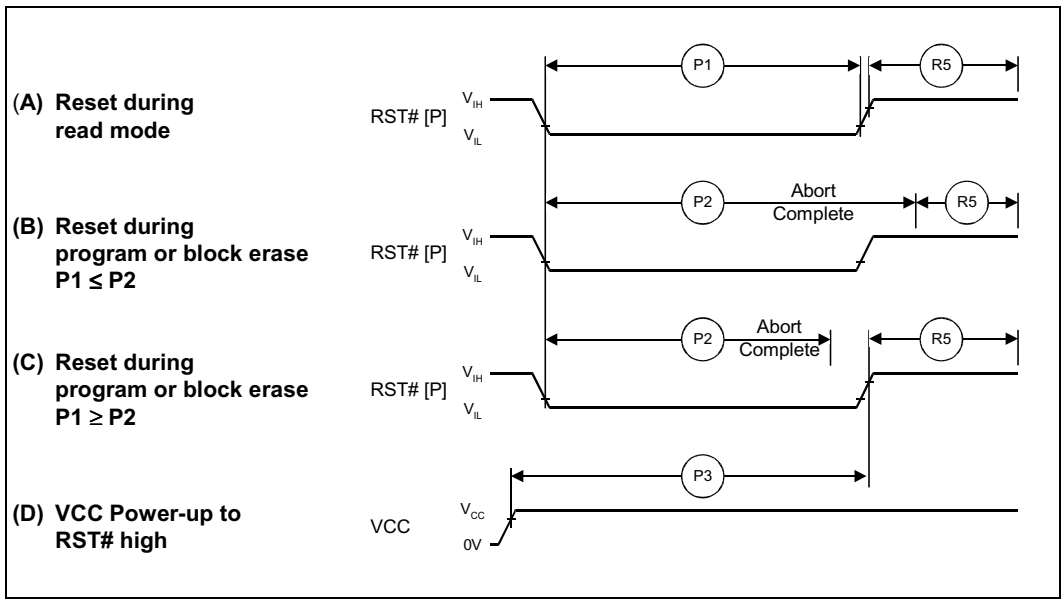
11.5 Reset Specifications

Table 25. Reset Specifications

#	Symbol	Parameter[1]	Notes	Min	Max	Unit
P1	t_{PLPH}	RST# Low to Reset during Read	1, 2, 3, 4	100		ns
P2	t_{PLRH}	RST# Low to Reset during Block Erase	1, 3, 4, 5		20	µs
		RST# Low to Reset during Program	1, 3, 4, 5		10	µs
P3	t_{VCCPH}	VCC Power Valid to Reset	1,3,4,5,6	60		µs

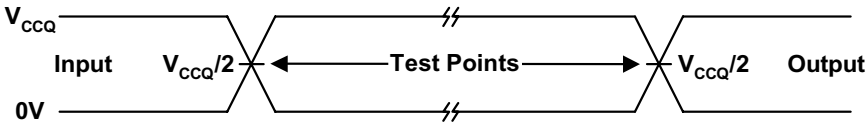
NOTES:
1. These specifications are valid for all product versions (packages and speeds).
2. The device may reset if $t_{PLPH} < t_{PLPH}$Min, but this is not guaranteed.
3. Not applicable if RST# is tied to VCC.
4. Sampled, but not 100% tested.
5. If RST# is tied to VCC, the device is not ready until t_{VCCPH} occurs after when $V_{CC} \geq V_{CC}$Min.
6. If RST# is tied to any supply/signal with V_{CCQ} voltage levels, the RST# input voltage must not exceed V_{CC} until $V_{CC} \geq V_{CC}$Min.

Figure 32. Reset Operations Waveforms



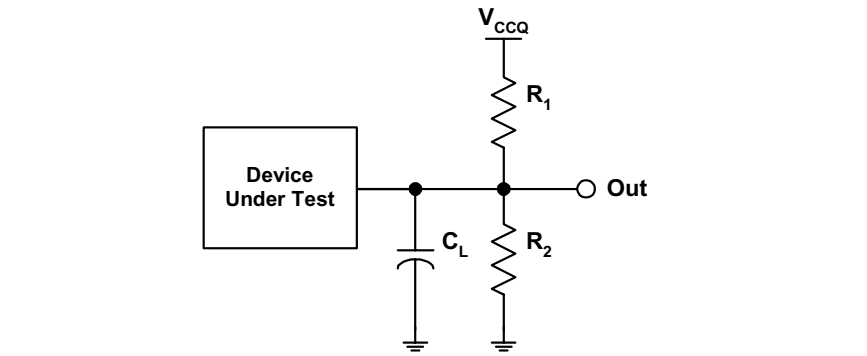
11.6 AC I/O Test Conditions

Figure 33. AC Input/Output Reference Waveform



NOTE: Input timing begins, and output timing ends, at $V_{CCQ}/2$. Input rise and fall times (10% to 90%) < 5 ns. Worst case speed conditions are when $V_{CC} = V_{CC}$Min.

Figure 34. Transient Equivalent Testing Load Circuit



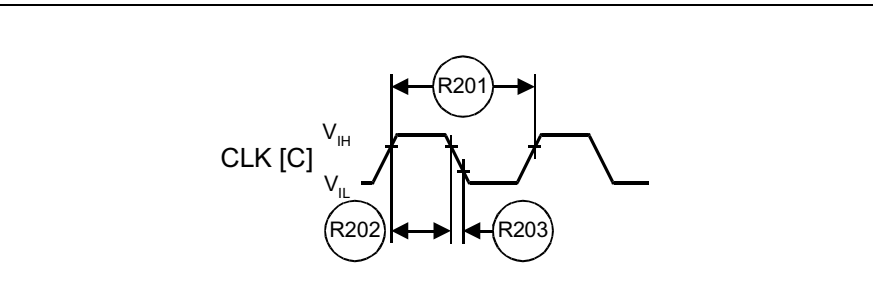
NOTE: See Table 17 for component values.

Table 26. Test Configuration Component Values for Worst Case Speed Conditions

Test Configuration	C_L (pF)	R_1 (kΩ)	R_2 (kΩ)
V_{CCQ}Min-Extended (1.35 V) Standard Test	30	13.5	13.5
V_{CCQ}Min (1.7 V) Standard Test	30	16.7	16.7

NOTE: C_L includes jig capacitance.

Figure 35. Clock Input AC Waveform



11.7 Device Capacitance

T_A = +25 °C, f = 1 MHz

Symbol	Parameter[§]	Typ	Max	Unit	Condition
C_{IN}	Input Capacitance	6	8	pF	V_{IN} = 0.0 V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0.0 V
C_{CE}	CE# Input Capacitance	10	12	pF	V_{IN} = 0.0 V

[§]Sampled, not 100% tested.

Appendix A Write State Machine States

This table shows the command state transitions based on incoming commands. Only one partition can be actively programming or erasing at a time.

Figure 36. Write State Machine — Next State Table (Sheet 1 of 2)

Write State Machine (WSM) Next State Table

***Chip* Next State after Command Input**

Current Chip State[8]		Read Array[3] (FFH)	Program Setup[4,5] (10H/40H)	Erase Setup[4,5] (20H)	Enhanced Factory Pgm Setup[4] (30H)	BE Confirm, P/E Resume, ULB Confirm[9] (D0H)	Program/ Erase Suspend (B0H)	Read Status (70H)	Clear Status Register[6] (50H)	Read ID/Query (90H, 98H)
Ready		Ready	Program Setup	Erase Setup	EFP Setup	Ready				
Lock/CR Setup		Ready (Lock Error)				Ready	Ready (Lock Error)			
OTP	Setup	OTP Busy								
	Busy									
Program	Setup	Program Busy								
	Busy	Program Busy					Pgm Susp	Program Busy		
	Suspend	Program Suspend				Pgm Busy	Program Suspend			
Erase	Setup	Ready (Error)				Erase Busy	Ready (Error)			
	Busy	Erase Busy					Erase Susp	Erase Busy		
	Suspend	Erase Suspend	Pgm in Erase Susp Setup	Erase Suspend		Erase Busy	Erase Suspend			
Program in Erase Suspend	Setup	Program in Erase Suspend Busy								
	Busy	Program in Erase Suspend Busy					Pgm Susp in Erase Susp	Program in Erase Suspend Busy		
	Suspend	Program Suspend in Erase Suspend				Pgm in Erase Susp Busy	Program Suspend in Erase Suspend			
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)				Erase Susp	Erase Suspend (Lock Error)			
Enhanced Factory Program	Setup	Ready (Error)				EFP Busy	Ready (Error)			
	EFP Busy	EFP Busy[7]								
	EFP Verify	Verify Busy[7]								

***Output* Next State after Command Input**

Output Next State Table[1]

Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status						
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status						
OTP Busy	Array[3]	Status	Output does not change	Status	Output does not change	Status	
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp						ID/Query	

Figure 36. Write State Machine — Next State Table (Sheet 2 of 2)

Write State Machine (WSM) Next State Table

***Chip* Next State after Command Input**

Current Chip State[8]		Lock, Unlock, Lock-down, CR setup[5] (60H)	OTP Setup[5] (C0H)	Lock Block Confirm[9] (01H)	Lock-Down Block Confirm[9] (2FH)	Write CR Confirm[9] (03H)	Enhanced Fact Pgm Exit (blk add <> WA0) (XXXXH)	Illegal commands or EFP data[2] (other codes)	WSM Operation Completes
Ready		Lock/CR Setup	OTP Setup	Ready					N/A
Lock/CR Setup		Ready (Lock Error)		Ready	Ready	Ready	Ready (Lock Error)		N/A
OTP	Setup	OTP Busy							N/A
	Busy								Ready
Program	Setup	Program Busy							N/A
	Busy	Program Busy							Ready
	Suspend	Program Suspend							N/A
Erase	Setup	Ready (Error)							N/A
	Busy	Erase Busy						Erase Busy	Ready
	Suspend	Lock/CR Setup in Erase Susp	Erase Suspend						N/A
Program in Erase Suspend	Setup	Program in Erase Suspend Busy							N/A
	Busy	Program in Erase Suspend Busy							Erase Suspend
	Suspend	Program Suspend in Erase Suspend							N/A
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)		Erase Susp	Erase Susp	Erase Susp	Erase Suspend (Lock Error)		N/A
Enhanced Factory Program	Setup	Ready (Error)							N/A
	EFP Busy	EFP Busy[7]					EFP Verify	EFP Busy[7]	N/A
	EFP Verify	Verify Busy[7]					Ready	EFP Verify[7]	Ready

***Output* Next State after Command Input**

Output Next State Table[1]

Pgm Setup, Erase Setup, OTP Setup, Pgm in Erase Susp Setup, EFP Setup, EFP Busy, Verify Busy	Status						Output does not change
Lock/CR Setup, Lock/CR Setup in Erase Susp	Status			Array	Status		
OTP Busy	Status	Output does not change			Array	Output does not change	
Ready, Pgm Busy, Pgm Suspend, Erase Busy, Erase Suspend, Pgm In Erase Susp Busy, Pgm Susp In Erase Susp							

NOTES:

1. The output state shows the type of data that appears at the outputs if the partition address is the same as the command address.
   A partition can be placed in Read Array, Read Status or Read ID/CFI, depending on the command issued. Each partition stays in its last output state (Array, ID/CFI or Status) until a new command changes it. The next WSM state does not depend on the partition's output state.
   For example, if partition #1's output state is Read Array and partition #4's output state is Read Status, every read from partition #4 (without issuing a new command) outputs the Status register.

2. Illegal commands are those not defined in the command set.
3. All partitions default to Read Array mode at power-up. A Read Array command issued to a busy partition results in undermined data when a partition address is read.
4. Both cycles of 2 cycles commands should be issued to the same partition address. If they are issued to different partitions, the second write determines the active partition. Both partitions will output status information when read.
5. If the WSM is active, both cycles of a 2 cycle command are ignored. This differs from previous Intel devices.
6. The Clear Status command clears status register error bits except when the WSM is running (Pgm Busy, Erase Busy, Pgm Busy In Erase Suspend, OTP Busy, EFP modes) or suspended (Erase Suspend, Pgm Suspend, Pgm Suspend In Erase Suspend).
7. EFP writes are allowed only when status register bit SR.0 = 0. EFP is busy if Block Address = address at EFP Confirm command. Any other commands are treated as data.
8. The "current state" is that of the WSM, not the partition.
9. Confirm commands (Lock Block, Unlock Block, Lock-down Block, Configuration Register) perform the operation and then move to the Ready State.
10. In Erase suspend, the only valid two cycle commands are "Program Word", "Lock/Unlock/Lockdown Block", and "CR Write". Both cycles of other two cycle commands ("OEM CAM program & confirm", "Program OTP & confirm", "EFP Setup & confirm", "Erase setup & confirm") will be ignored. In Program suspend or Program suspend in Erase suspend, both cycles of all two cycle commands will be ignored.

Appendix B Common Flash Interface

This appendix defines the data structure or "database" returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

B.1 Query Structure Output

The Query database allows system software to obtain information for controlling the flash device. This section describes the device's CFI-compliant interface that allows access to Query data.

Query data are presented on the lowest-order data outputs (DQ0-7) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two Query-structure bytes, ASCII "Q" and "R," appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00h data on upper bytes. The device outputs ASCII "Q" in the low byte (DQ_{0-7}) and 00h in the high byte (DQ_{8-15}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the "h" suffix has been dropped. In addition, since the upper byte of word-wide devices is always "00h," the leading "00" has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table 27. Summary of Query Structure Output as a Function of Device and Mode

Device	Hex Offset	Hex Code	ASCII Value
Device Addresses	00010:	51	"Q"
	00011:	52	"R"
	00012:	59	"Y"

Table 28. Example of Query Structure Output of x16- and x8 Devices

Word Addressing:			Byte Addressing:		
Offset	Hex Code	Value	Offset	Hex Code	Value
A_X–A_0	D_{15}–D_0		A_X–A_0	D_7–D_0	
00010h	0051	"Q"	00010h	51	"Q"
00011h	0052	"R"	00011h	52	"R"
00012h	0059	"Y"	00012h	59	"Y"
00013h	P_ID_{LO}	PrVendor	00013h	P_ID_{LO}	PrVendor
00014h	P_ID_{HI}	ID #	00014h	P_ID_{LO}	ID #
00015h	P_{LO}	PrVendor	00015h	P_ID_{HI}	ID #
00016h	P_{HI}	TblAdr	00016h	...	...
00017h	A_ID_{LO}	AltVendor	00017h		
00018h	A_ID_{HI}	ID #	00018h		
...	...	...	...		

B.2 Query Structure Overview

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The structure sub-sections and address locations are summarized below.

Table 29. Query Structure

Offset	Sub-Section Name	Description(1)
00000h		Manufacturer Code
00001h		Device Code
(BA+2)h(2)	Block Status register	Block-specific information
00004-Fh	Reserved	Reserved for vendor-specific information
00010h	CFI query identification string	Command set ID and vendor data offset
0001Bh	System interface information	Device timing & voltage information
00027h	Device geometry definition	Flash device layout
P(3)	Primary Intel-specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

NOTES:
1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = Block Address beginning location (i.e., 08000h is block 1's beginning location when the block size is 32K-word).
3. Offset 15 defines "P" which points to the Primary Intel-specific Extended Query Table.

B.3 Block Status Register

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. BSR.1 can be used just after power-up to verify that the VCC supply was not accidentally removed during an erase operation.

Table 30. Block Status Register

Offset	Length	Description	Add.	Value
(BA+2)h(1)	1	Block Lock Status Register	BA+2	--00 or --01
		BSR.0 Block lock status 0 = Unlocked 1 = Locked	BA+2	(bit 0): 0 or 1
		BSR.1 Block lock-down status 0 = Not locked down 1 = Locked down	BA+2	(bit 1): 0 or 1
		BSR 2–7: Reserved for future use	BA+2	(bit 2–7): 0

NOTES:
1. BA = Block Address beginning location (i.e., 08000h is block 1's beginning location when the block size is 32K-word).

B.4 CFI Query Identification String

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table 31. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string “QRY“	10: 11: 12:	--51 --52 --59	"Q" "R" "Y"
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--03 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--39 --00	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

Table 32. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--17	1.7V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--19	1.9V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--B4	11.4V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--C6	12.6V
1Fh	1	“n” such that typical single word program time-out = 2^n µ-sec	1F:	--04	16µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µ-sec	20:	--00	NA
21h	1	“n” such that typical block erase time-out = 2^n m-sec	21:	--0A	1s
22h	1	“n” such that typical full chip erase time-out = 2^n m-sec	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--04	256µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--00	NA
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--03	8s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

B.5 Device Geometry Definition

Table 33. Device Geometry Definition

Offset	Length	Description	Code		
27h	1	"n" such that device size = 2^n in number of bytes	27:	See table below	
28h	2	Flash device interface code assignment: "n" such that n+1 specifies the bit field that represents the flash device width capabilities as described in the table: 7 6 5 4 3 2 1 0 — — — — x64 x32 x16 x8 15 14 13 12 11 10 9 8 — — — — — — — —	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--00 --00	0
2Ch	1	Number of erase block regions (x) within device: 1. x = 0 means no erase blocking; the device erases in bulk 2. x specifies the number of device regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region	2C:	See table below	
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:	See table below	
31h	4	Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	31: 32: 33: 34:	See table below	
35h	4	Reserved for future erase block region information	35: 36: 37: 38:	See table below	

Address	32 Mbit		64 Mbit		128 Mbit	
	–B	–T	–B	–T	–B	–T
27:	--16	--16	--17	--17	--18	--18
28:	--01	--01	--01	--01	--01	--01
29:	--00	--00	--00	--00	--00	--00
2A:	--00	--00	--00	--00	--00	--00
2B:	--00	--00	--00	--00	--00	--00
2C:	--02	--02	--02	--02	--02	--02
2D:	--07	--3E	--07	--7E	--07	--FE
2E:	--00	--00	--00	--00	--00	--00
2F:	--20	--00	--20	--00	--20	--00
30:	--00	--01	--00	--01	--00	--01
31:	--3E	--07	--7E	--07	--FE	--07
32:	--00	--00	--00	--00	--00	--00
33:	--00	--20	--00	--20	--00	--20
34:	--01	--00	--01	--00	--01	--00
35:	--00	--00	--00	--00	--00	--00
36:	--00	--00	--00	--00	--00	--00
37:	--00	--00	--00	--00	--00	--00
38:	--00	--00	--00	--00	--00	--00

B.6 Intel-Specific Extended Query Table

Table 34. Primary Vendor-Specific Extended Query

Offset[1] P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	39:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	3A:	--52	"R"
(P+2)h			3B:	--49	"I"
(P+3)h	1	Major version number, ASCII	3C:	--31	"1"
(P+4)h	1	Minor version number, ASCII	3D:	--33	"3"
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	3E:	--E6	
(P+6)h		*bits 10–31 are reserved; undefined bits are "0." If bit 31 is*	3F:	--03	
(P+7)h		*"1" then another 31 bit field of Optional features follows at*	40:	--00	
(P+8)h		*the end of the bit–30 field.*	41:	--00	
		bit 0 Chip erase supported	bit 0	= 0	No
		bit 1 Suspend erase supported	bit 1	= 1	Yes
		bit 2 Suspend program supported	bit 2	= 1	Yes
		bit 3 Legacy lock/unlock supported	bit 3	= 0	No
		bit 4 Queued erase supported	bit 4	= 0	No
		bit 5 Instant individual block locking supported	bit 5	= 1	Yes
		bit 6 Protection bits supported	bit 6	= 1	Yes
		bit 7 Pagemode read supported	bit 7	= 1	Yes
		bit 8 Synchronous read supported	bit 8	= 1	Yes
		bit 9 Simultaneous operations supported	bit 9	= 1	Yes
(P+9)h	1	Supported functions after suspend: read Array, Status, Query	42:	--01	
		Other supported operations are:			
		bits 1–7 reserved; undefined bits are "0"			
		bit 0 Program supported after erase suspend	bit 0	= 1	Yes
(P+A)h	2	Block status register mask	43:	--03	
(P+B)h		*bits 2–15 are Reserved; undefined bits are "0"*	44:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0	= 1	Yes
		bit 1 Block Lock-Down Bit Status active	bit 1	= 1	Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage	45:	--18	1.8V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 BCD value in volts			
(P+D)h	1	V_{PP} optimum program/erase supply voltage	46:	--C0	12.0V
		bits 0–3 BCD value in 100 mV			
		bits 4–7 HEX value in volts			

Table 35. Protection Register Information

Offset(1) P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection fields are available	47:	--01	1
(P+F)h (P+10)h (P+11)h (P+12)h	4	Protection Field 1: Protection Description This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section's first byte. The following bytes are factory pre-programmed and user-programmable. bits 0–7 = Lock/bytes Jedec-plane physical low address bits 8–15 = Lock/bytes Jedec-plane physical high address bits 16–23 = "n" such that 2n = factory pre-programmed bytes bits 24–31 = "n" such that 2n = user programmable bytes	48: 49: 4A: 4B:	--80 --00 --03 --03	80h 00h 8 byte 8 byte

Table 36. Burst Read Information for Non-muxed Device

Offset(1) P = 39h	Length	Description (Optional flash features and commands)	Add.	Hex Code	Value
(P+13)h	1	Page Mode Read capability bits 0–7 = "n" such that 2^n HEX value represents the number of read-page bytes. See offset 28h for device word width to determine page-mode data output width. 00h indicates no read page buffer.	4C:	--03	8 byte
(P+14)h	1	Number of synchronous mode read configuration fields that follow. 00h indicates no burst capability.	4D:	--04	4
(P+15)h	1	Synchronous mode read capability configuration 1 Bits 3–7 = Reserved bits 0–2 "n" such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the Read Configuration Register bits 0–2 if the device is configured for its maximum word width. See offset 28h for word width to determine the burst data output width.	4E:	--01	4
(P+16)h	1	Synchronous mode read capability configuration 2	4F:	--02	8
(P+17)h	1	Synchronous mode read capability configuration 3	50:	--03	16
(P+18)h	1	Synchronous mode read capability configuration 4	51:	--07	Cont

Table 37. Partition and Erase-block Region Information

Offset(1) P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+19)h	(P+19)h	Number of device hardware-partition regions within the device. x = 0: a single hardware partition device (no fields follow). x specifies the number of device partition regions containing one or more contiguous erase block regions.	1	52:	52:

Partition Region 1 Information

Offset[1] P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+1A)h (P+1B)h	(P+1A)h (P+1B)h	Number of identical partitions within the partition region	2	53: 54:	53: 54:
(P+1C)h	(P+1C)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	55:	55:
(P+1D)h	(P+1D)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	56:	56:
(P+1E)h	(P+1E)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	57:	57:
(P+1F)h	(P+1F)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +…+ (Type n blocks)x(Type n block sizes)	1	58:	58:
(P+20)h (P+21)h (P+22)h (P+23)h	(P+20)h (P+21)h (P+22)h (P+23)h	Partition Region 1 Erase Block Type 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	59: 5A: 5B: 5C:	59: 5A: 5B: 5C:
(P+24)h (P+25)h	(P+24)h (P+25)h	Partition 1 (Erase Block Type 1) Minimum block erase cycles x 1000	2	5D: 5E:	5D: 5E:
(P+26)h	(P+26)h	Partition 1 (erase block Type 1) bits per cell; internal ECC bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	5F:	5F:
(P+27)h	(P+27)h	Partition 1 (erase block Type 1) page mode and synchronous mode capabilities defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	60:	60:
(P+28)h (P+29)h (P+2A)h (P+2B)h		Partition Region 1 Erase Block Type 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes (bottom parameter device only)	4	61: 62: 63: 64:	
(P+2C)h (P+2D)h		Partition 1 (Erase block Type 2) Minimum block erase cycles x 1000	2	65: 66:	
(P+2E)h		Partition 1 (Erase block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	67:	
(P+2F)h		Partition 1 (Erase block Type 2) pagemode and synchronous mode capabilities defined in Table 10 bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	68:	

Partition Region 2 Information

Offset(1) P = 39h		Description	See table below		
				Address	
Bottom	Top	(Optional flash features and commands)	Len	Bot	Top
(P+30)h (P+31)h	(P+28)h (P+29)h	Number of identical partitions within the partition region	2	69: 6A:	61: 62:
(P+32)h	(P+2A)h	Number of program or erase operations allowed in a partition bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6B:	63:
(P+33)h	(P+2B)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Program mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6C:	64:
(P+34)h	(P+2C)h	Simultaneous program or erase operations allowed in other partitions while a partition in this region is in Erase mode bits 0–3 = number of simultaneous Program operations bits 4–7 = number of simultaneous Erase operations	1	6D:	65:
(P+35)h	(P+2D)h	Types of erase block regions in this Partition Region. x = 0 = no erase blocking; the Partition Region erases in bulk x = number of erase block regions w/ contiguous same-size erase blocks. Symmetrically blocked partitions have one blocking region. Partition size = (Type 1 blocks)x(Type 1 block sizes) + (Type 2 blocks)x(Type 2 block sizes) +…+ (Type n blocks)x(Type n block sizes)	1	6E:	66:
(P+36)h (P+37)h (P+38)h (P+39)h	(P+2E)h (P+2F)h (P+30)h (P+31)h	Partition Region 2 Erase Block Type 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4	6F: 70: 71: 72:	67: 68: 69: 6A:
(P+3A)h (P+3B)h	(P+32)h (P+33)h	Partition 2 (Erase block Type 1) Minimum block erase cycles x 1000	2	73: 74:	6B: 6C:
(P+3C)h	(P+34)h	Partition 2 (Erase block Type 1) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserve for future use	1	75:	6D:
(P+3D)h	(P+35)h	Partition 2 (erase block Type 1) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1	76:	6E:
	(P+36)h (P+37)h (P+38)h (P+39)h	Partition Region 2 Erase Block Type 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	4		6F: 70: 71: 72:
	(P+3A)h (P+3B)h	Partition 2 (Erase Block Type 2) Minimum block erase cycles x 1000	2		73: 74:
	(P+3C)h	Partition 2 (Erase Block Type 2) bits per cell bits 0–3 = bits per cell in erase region bit 4 = reserved for “internal ECC used” (1=yes, 0=no) bits 5–7 = reserved for future use	1		75:
	(P+3D)h	Partition 2 (Erase block Type 2) pagemode and synchronous mode capabilities as defined in Table 10. bit 0 = page-mode host reads permitted (1=yes, 0=no) bit 1 = synchronous host reads permitted (1=yes, 0=no) bit 2 = synchronous host writes permitted (1=yes, 0=no) bits 3–7 = reserved for future use	1		76:
(P+3E)h	(P+3E)h	Features Space definitions (Reserved for future use)	TBD	77:	77:
(P+3F)h	(P+3F)h	Reserved for future use	Resv'd	78:	78:

Partition and Erase-block Region Information

Address	32 Mbit		64Mbit		128Mbit	
	–B	–T	–B	–T	–B	–T
52:	--02	--02	--02	--02	--02	--02
53:	--01	--07	--01	--0F	--01	--1F
54:	--00	--00	--00	--00	--00	--00
55:	--11	--11	--11	--11	--11	--11
56:	--00	--00	--00	--00	--00	--00
57:	--00	--00	--00	--00	--00	--00
58:	--02	--01	--02	--01	--02	--01
59:	--07	--07	--07	--07	--07	--07
5A:	--00	--00	--00	--00	--00	--00
5B:	--20	--00	--20	--00	--20	--00
5C:	--00	--01	--00	--01	--00	--01
5D:	--64	--64	--64	--64	--64	--64
5E:	--00	--00	--00	--00	--00	--00
5F:	--01	--01	--01	--01	--01	--01
60:	--03	--03	--03	--03	--03	--03
61:	--06	--01	--06	--01	--06	--01
62:	--00	--00	--00	--00	--00	--00
63:	--00	--11	--00	--11	--00	--11
64:	--01	--00	--01	--00	--01	--00
65:	--64	--00	--64	--00	--64	--00
66:	--00	--02	--00	--02	--00	--02
67:	--01	--06	--01	--06	--01	--06
68:	--03	--00	--03	--00	--03	--00
69:	--07	--00	--0F	--00	--1F	--00
6A:	--00	--01	--00	--01	--00	--01
6B:	--11	--64	--11	--64	--11	--64
6C:	--00	--00	--00	--00	--00	--00
6D:	--00	--01	--00	--01	--00	--01
6E:	--01	--03	--01	--03	--01	--03
6F:	--07	--07	--07	--07	--07	--07
70:	--00	--00	--00	--00	--00	--00
71:	--00	--20	--00	--20	--00	--20
72:	--01	--00	--01	--00	--01	--00
73:	--64	--64	--64	--64	--64	--64
74:	--00	--00	--00	--00	--00	--00
75:	--01	--01	--01	--01	--01	--01
76:	--03	--03	--03	--03	--03	--03

NOTES:
1. The variable P is a pointer which is defined at CFI offset 15h.
2. TPD - Top parameter device; BPD - Bottom parameter device.
3. Partition: Each partition is 4Mb in size. It can contain main blocks OR a combination of both main and parameter blocks.
4. Partition Region: Symmetrical partitions form a partition region. (there are two partition regions, A. contains all the partitions that are made up of main blocks only. B. contains the partition that is made up of the parameter and the main blocks.

Appendix C Mechanical Specifications

Figure 37. 32-Mbit and 64-Mbit VF BGA, 0.75 mm Ball Pitch, 7×8 Ball Matrix Package Drawing

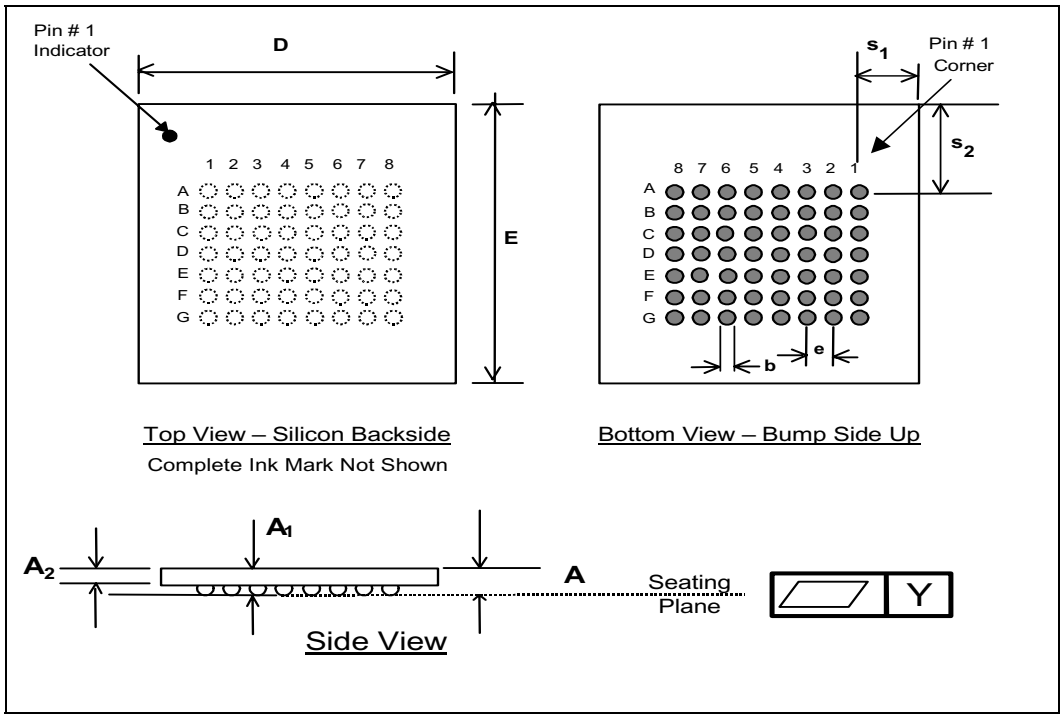


Figure 38. 128-Mbit VF BGA, 0.75 mm Ball Pitch, 7×8 Ball Matrix Package Drawing

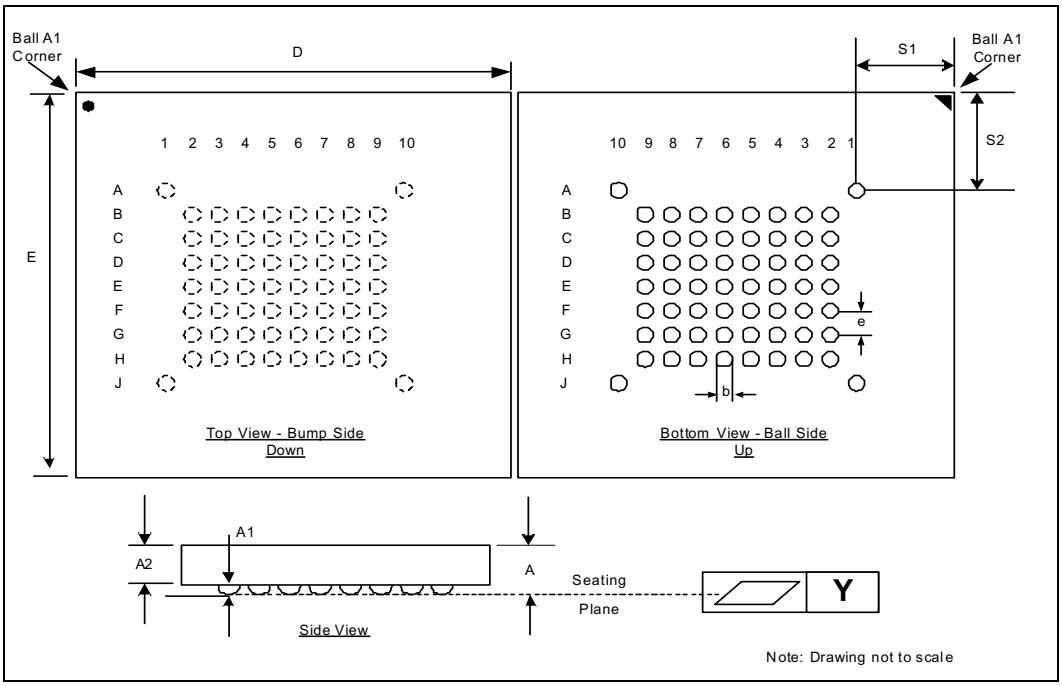


Table 38. 32-Mbit and 64-Mbit Package Dimensions

Dimension	Symbol	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	0.850		1.000	0.0335		0.0394
Ball Height	A_1	0.150			0.0059		
Package Body Thickness	A_2	0.615	0.665	0.715	0.0242	0.0262	0.0281
Ball (Lead) Width	b	0.325	0.375	0.425	0.0128	0.0148	0.0167
Package Body Width (32Mb/64Mb)	D	7.600	7.700	7.800	0.2992	0.3031	0.3071
Package Body Width (128Mb)	D	12.400	12.500	12.600	0.4882	0.4921	0.4961
Package Body Length (32Mb/64Mb)	E	8.900	9.000	9.100	0.3503	0.3543	0.3583
Package Body Length (128Mb)	E	11.900	12.000	12.100	0.4685	0.4724	0.4764
Pitch	[e]		0.750			0.0295	
Ball (Lead) Count (32Mb/64Mb)	N		56			56	
Ball (Lead) Count (128Mb)	N		60			60	
Seating Plane Coplanarity	Y			0.100			0.0039
Corner to Ball A1 Distance Along D (32Mb/64Mb)	S_1	1.125	1.225	1.325	0.0443	0.0482	0.0522
Corner to Ball A1 Distance Along D (128Mb)	S_1	2.775	2.875	2.975	0.1093	0.1132	0.1171
Corner to Ball A1 Distance Along E (32Mb/64Mb)	S_2	2.150	2.250	2.350	0.0846	0.0886	0.0925
Corner to Ball A1 Distance Along E (128Mb)	S_2	2.900	3.000	3.100	0.1142	0.1181	0.1220

Appendix D Ordering Information

Figure 39. Component Ordering Information