GS1560
Deserializer with loop-through cable driver for HD-SDI, SD-SDI and DVB-ASI

PRODUCT BRIEF

FEATURES

- compliant with SMPTE 292M and SMPTE 259M-C
- DVB-ASI auto-configuration
- DVB-ASI sync word detection and 8b/10b decoding
- dual serial digital input buffers with 2 x 1 mux
- integrated serial digital signal termination
- built in reclocker
- reclocked serial digital output buffer / cable driver
- automatic or manual rate selection / indication (HD / SD)
- SMPTE 292M and SMPTE 259M compliant de-scrambling and NRZI - > NRZ decoding (with bypass)
- descrambler bypass option
- user selectable additional processing features including:
  - CRC, TRS, ANC data checksum, line number and EDH CRC error detection and correction
  - programmable ANC data detection
  - illegal code re-mapping
- internal flywheel for noise immune H, V, F extraction
- FIFO load Pulse
- 20-Bit / 10-Bit CMOS parallel output data bus
- 148.5MHz / 74.25MHz / 27MHz / 13.5MHz parallel digital output
- automatic standards detection and indication
- 1.8V core power supply and 3.3V charge pump power supply
- 3.3V digital I/O supply
- JTAG test interface
- small footprint compatible with GS1561, GS1532, GS9060 and GS9062
- low power operation (typically < 475mW)

APPLICATIONS

- SMPTE 292M Serial Digital Interfaces
- SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

DESCRIPTION

The GS1560 is a dual-rate reclocking deserializer, compliant with SMPTE 292M and SMPTE 259M-C.

When used in conjunction with a GS1524 automatic cable equalizer and a GO1525 voltage controlled oscillator, a dual rate (1.485 / 1.483Gb/s and 270Mb/s), receive solution can be realized for HD-SDI, SD-SDI and DVB-ASI.

In addition to providing robust serial to parallel conversion with word alignment, the GS1560 includes a range of additional data processing functions such as error detection and correction, automatic standards detection, DVB-ASI and EDH support.

After reclocking and serial-to-parallel conversion, the device performs NRZI to NRZ decoding, descrambling as per SMPTE 292M / 259M and word alignment of the incoming data stream. The SMPTE descrambler and word alignment features can optionally be bypassed to support the reception of signals with other coding schemes.

Two serial digital input buffers are provided with a 2x1 multiplexor. This allows the device to select from one of two serial digital input signals.

The integrated reclocker features a very wide Input Jitter Tolerance (IJT) of ±0.3 UI, a rapid (typically less than 265µs) asynchronous lock time, and full compliance with DVB-ASI data streams.

A SMPTE 259M-C and SMPTE 292M compliant cable driver output is also provided for serial input loop through applications. The serial digital output can be selected as either before or after the integrated reclocker. The cable driver also features an output mute on loss of signal, high impedance mode, adjustable signal swing and automatic dual slew-rate selection depending on HD / SD operational requirements.

The GS1560 also features a number of signal integrity checks and measurement capabilities. Line-based CRC errors, Line number errors, TRS errors, EDH CRC errors and ancillary data check sum errors can all be detected. A single 'error' pin is provided which is a logical 'or'ing of all the detected errors. Individual error status can be read from the host interface port.

In addition to detecting signal errors, the device also includes the ability to correct all of the above detected errors. Each error correction function may be individually enabled / disabled via host interface control.

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In addition to the above, additional processing capabilities such as DVB-ASI decoding, EDH and various other signal detection and error correction capabilities are provided.

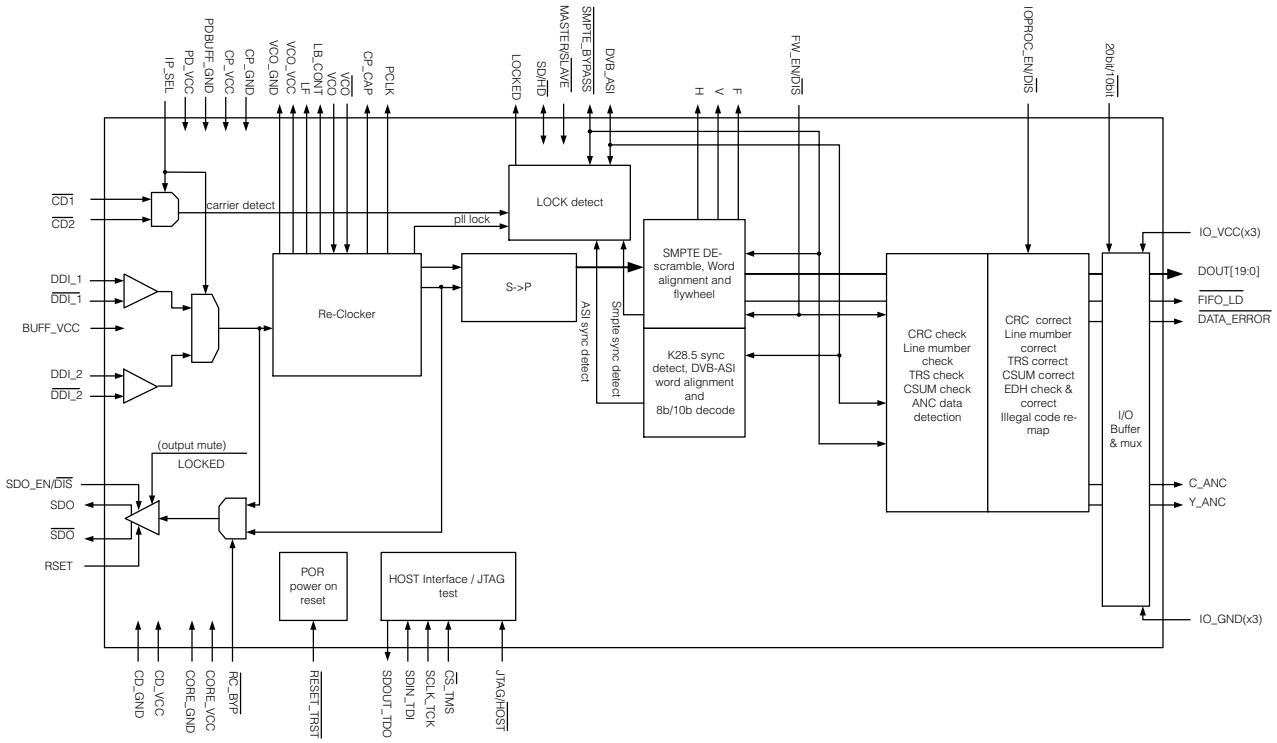
The device will detect the presence of DVB-ASI sync words and will automatically switch into bypass mode. The DVB-ASI data will be word aligned to K28.5 sync characters and 8b/10b decoding is applied to the received data stream.

EDH FF and AP CRC calculation and comparison is performed. Error flags are generated based on these CRC comparisons. Re-calculated CRC's may be inserted into the output data stream.

In addition to the error detection schemes previously mentioned, the GS1560 may optionally correct and replace detected errors. TRS error correction; CRC error correction; checksum error correction; line number error correction and illegal code re-mapping can all be carried out by the device.

Each error correction function may be individually enabled / disabled via host interface control. Line number generation is also performed by the device, and for HDTV interfaces, the line number may be inserted into the output data stream

As well as detecting and extracting SMPTE 352M payload identifier packets, the GS1560 also automatically identifies the received video standard. The detected video standard may be read via the host interface port.



GS1560 BLOCK DIAGRAM

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
PRODUCT BRIEF

REVISION NOTES:
Update PB with page 1-2 of new AIN.

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