ZARLINK
SEMICONDUCTOR

GSC200 Series
## 0.35μ CMOS Standard Cell ASICs
Advance Information

INTRODUCTION

The GSC200 standard cell ASIC family from Mitel Semiconductor is a standard cell product combining low power, mixed voltage capability with a very high density architecture on a 0.35μm process. The broad cell library includes a range of complex embedded functions and high-density ROMs and RAMs, as well as PLL and oscillators. These cells are optimised for easy synthesis, and are supported by high quality design kits for a range of industry standard CAE tools providing a low risk solution and faster time-to-market.

FEATURES

- Three or four layer metal on a 0.35μm (drawn) process
- Operation from 1.8V to 3.6V
- High density of up to 18,900 gates/mm^2
- Up to 5M gates
- 97ps gate delay for 2-input NAND with two loads (3.3V)
- Low power, 0.06μW/MHz/gate at 2V supply (NAND driving 2 inputs)
- 2V and 3.3V I/O capability on the same device
- 5V tolerant inputs and outputs
- Full set of I/O cells for direct pad synthesis
- Accurate delay modelling for gates and tracks with *sign off quality* CAE design libraries for QuickSim II, Verilog XL and VITAL
- CAE libraries optimized for synthesis
- Methodologies for ensuring low clock skew
- High density memories including single and dual port RAM
- Expanding range of Mitel Semiconductor SystemBuilder soft and hard cells for complex functions including 85C30, 8051, 8251 devices and OakDSPCore™ and ARM7TDMI™ programmable cores
- Wide range of packaging options including ball grid arrays
- Variable output speeds for low noise
- Supports IDDQ testing for high reliability
- Operating range -55°C to +125°C
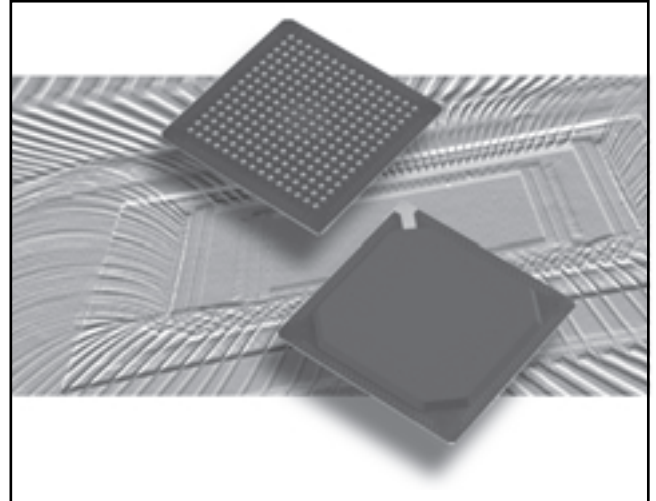
BENEFITS

- Fast customer time to market
  - Direct sign-off on industry standard CAE tools
  - Comprehensive industry standard CAE tools
  - SystemBuilder™ megacell libraries
  - World-wide design centre support
  - Reliable prototype and production delivery
  - Dual silicon sources

- Cost -effective Solutions
  - Optimised architecture for high density silicon utilisation
  - ISO9001 Factory with Statistical process control for optimum yield

ADVANTAGES OF STANDARD CELL ARCHITECTURE

Using GSC200 can represent a significant saving in chip area on many designs, with D-types 33% smaller than their gate array counterparts. GSC200 also offers a wide range of speed and power options - three different sizes of 2-input NAND gate, for example - making synthesis and retargetting of existing technology easier and quicker. Linear and staggered pads are available giving a low and high density pad option suited to the application.

By building a design from these cells, standard cell technology allows the designer to achieve a similar chip size to a fully-handcrafted custom IC, but in a fraction of the time. The small chip size means that GSC200 chips are low cost to manufacture, while the ability of GSC200 designs to include areas of gate array logic allows the designer to retain flexibility for last-minute design changes, or rapid introduction of derivative products.

CELL LIBRARIES

The cell library is optimized for synthesis and includes an expanding range of soft and hard macros. Cells include basic logic, such as inverters, NAND and NOR gates, adders, multiplexers, latches and flip flops, in a choice of drive strengths, allowing designers to make trade-offs between speed, power and silicon area. Memories and macros are also available from the extensive SystemBuilder library including microprocessors, UARTs, and a DSP core. The wide range of cells leads to shorter design cycle times.
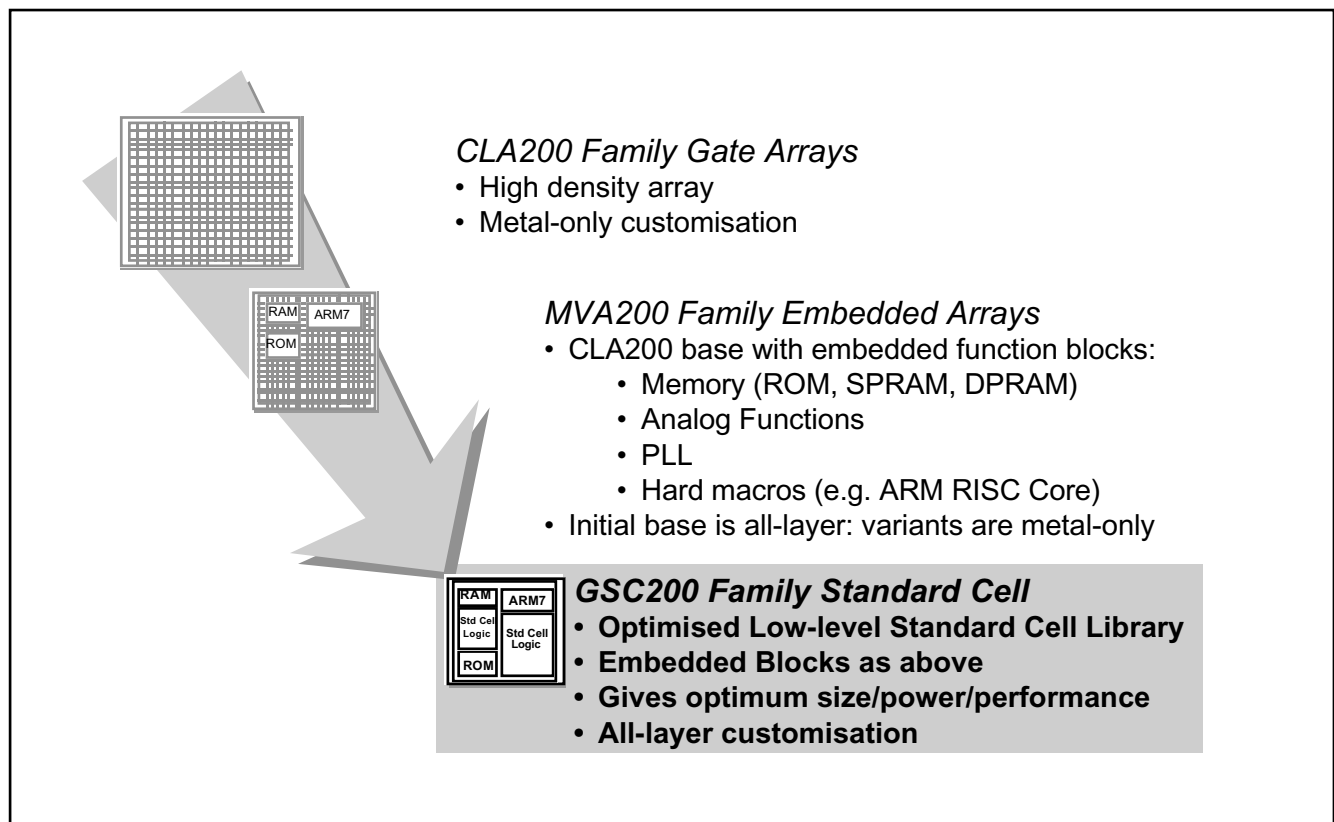

CLA200 Family Gate Arrays
• High density array
• Metal-only customisation

MVA200 Family Embedded Arrays
• CLA200 base with embedded function blocks:
  • Memory (ROM, SPRAM, DPRAM)
  • Analog Functions
  • PLL
  • Hard macros (e.g. ARM RISC Core)
• Initial base is all-layer: variants are metal-only

GSC200 Family Standard Cell
• **Optimised Low-level Standard Cell Library**
• **Embedded Blocks as above**
• **Gives optimum size/power/performance**
• **All-layer customisation**

Fig.1 The Mitel Semiconductor 0.35μm ASIC Families

I/O Cells
The GSC200 standard cell series libraries contain a wide choice of input, output and bi-directional cells.

GSC200 series I/Os have the following features:

•   Cell library contains distinct and complete inputs, outputs and bidirectionals to allow direct pad synthesis
•   Selectable I/O output speeds allow the designer to maintain low noise and reduce the number of power supply pins if output speed is not critical
•   All inputs have optional pullup, pulldown resistors and can have a hold option to hold the input in tristate applications
•   Device I/O can interface to 5V logic with no static power consumption while still benefiting from a low voltage, low power core
•   All input and output cells are noninverting
•   I/O cells are optimized for 3.3V $\pm$ 10% and are fully functional down to 1.8V with derated current and speed
•   Device I/O can operate at a different voltage from the device core
•   Output currents up to 12mA supported from a single I/O cell
•   24mA current drive available

GSC200 has four separate VDD supply rails and three GND rails, one VDD rail for the core, one for input buffers, and two for output areas of the chip. The intermediate buffer supply rail can be completely isolated for very low noise. This offers the benefit of good noise immunity with multiple supply voltage capability to suit the application. The mixed 2 and 3.3V I/O capability can be used for power saving or interfacing with 2V and 3.3V systems. 5V tolerant input and output cells are also available to offer the advantages of a very low power core whilst interfacing to 5V systems.

Electrostatic discharge (ESD) protection is built into the input and output cells, and is specified to withstand at least 2kV (human body model). The structure and process is also highly resistant to latch-up and able to withstand forward bias currents in excess of 200mA.

SYSTEMBUILDER
The SystemBuilder library contains a broad range of macrofunctions designed to improve designers efficiency. Most of the SystemBuilder macrofunctions are supplied as synthesizable RTL models for both VHDL and Verilog. In addition these macrofunctions are fully supported with synthesis scripts, test-benches and full documentation. More information is provided on SystemBuilder on page 11.

The SystemBuilder library includes the following functions:

•   ARM7TDMI ARM RISC microprocessor core
•   The OakDSPCore™ - DSP Core processor
•   Standard Microprocessor Cores including 8048, 8051 & 8086
•   Standard Microprocessor peripherals including DMA controllers, programmable interval timers, real time clock & programmable interrupt controllers.

•   Floppy disc/tape functions including controllers and data separators
•   Standard Serial Communications controllers including 85C30, 16C450, 16C550, 8251 & 8250
•   Bus interface cores including PCMCIA, Ethernet, IEEE1284, USB and PCI

In addition the SystemBuilder library also contains a range of clearly defined functions that are frequently required for Systems Level Integration (SLI) ASICs. Please see page 11.

Further functions are continually being added. An up to date list may be obtained from any Mitel Semiconductor Sales and Design Centre.

ARM Core

The ARM7 core offers the following features:
•   32 bit RISC core
•   Operation up to 40MHz with 3.3V supply
•   Hardware debug capabilities on TDMI version
•   Support for 'Thumb' instruction set
•   30% improvement in code density over native ARM code
•   Efficient 16 bit bus operation
•   Software Development Toolkit with C compiler, and board development products available

Notes
i)   The 'Thumb' operating mode uses a subset of the standard ARM instruction set that has been re-coded into 16 bit wide op-codes. A small amount of additional logic decompresses these 16 bit instructions back to their 32-bit ARM equivalent in real time for execution.
ii) Mitel Semiconductor will supply datasheets and behavioural VHDL models of the ARM7TDMI core to SystemBuilder customers, and will incorporate the core itself as a hard macro at the layout stage of an embedded array or cell-based device.

OakDSPCore™

OakDSPCore™ offers the following features:
•   16-bit fixed point DSP core, with modified Harvard architecture
•   Power-saving modes for portable applications
•   Single cycle 16 x 16 + 36 -> 36-bit
•   Multiply-accumulate instruction
•   User-configurable on-chip registers and program/data memory
•   Special RAM and ROM support
•   Operation up to 60MHz with 3.3V supply
•   Expandable data RAM or ROM
•   Expandable program RAM or ROM

Please contact your Mitel Semiconductor Customer Service Centre
for more details of programmable cores.

MEMORY BLOCKS

A memory compiler (PMG) is available which allows designers to specify the number of bits and words required. The PMG can automatically create design views for all of the supported CAE tools.

Available memories, RAMs and ROMs include :
- Single port and true dual port RAMs and ROM

Single Port RAM
- Flexible
    - RAMs up to 128Kbits
    - Word size from 4 to 128 bits in steps of 1
    - Address 24 to 8k words
    - Range of mux options
        - >> (4, 8, 16 and 32)
  Wide operating range
    - 1.8 to 3.6V
    - - 55 to 150°C
- Interface
    - Simple clocked interface
    - Input and output buses
    - Zero DC power (intrinsic leakage)

RAM Size	512	4K	64K	128K	Bits
Cycle time	3.0	3.3	5.3	6.2	ns
Access time	3.0	3.2	4.7	5.3	ns
Read power	0.5	0.6	0.7	0.8	mW/MHz
Write power	0.2	0.4	0.7	0.8	mW/MHz
Area	0.08	0.26	2.4	4.6	sq. mm

Table. 1

Dual Port RAM

- Same generator options and operating range as single port RAM
- Full read and write access from both ports
- Separate input and output data buses
- Wide range of instance sizes
    - RAMs from 96 to 128KBits
    - Word size from 4 to 64 bits in steps of 1
    - Address 24 to 8k words
- Zero static DC power consumption (Intrinsic leakage)
- Wide operating range
    - 1.8 to 3.6V
    - - 55 to 150°C

ROM
- Flexible
    - ROMs up to 256kbits
    - Word up to 64bits
    - Address 512 to 8k words
    - Range of mux options
        - >> (16, 32 and 64)
- Contact mask programming
- Interface
    - Simple clocked interface
    - Zero DC power
- Zero static DC power consumption (Intrinsic leakage)
- 150,000 Bits/mm^2
  Wide operating range
    - 1.8 to 3.6V
    - - 55 to 150°C

ANALOG BLOCKS

Phase Locked Loop

The increasingly high clock rates used on smaller technology devices give rise to increased problems with clock delay and clock skew. The phase-locked loop (PLL) provides the means to synchronize internal clock edges. The connection of high speed clocks from external sources is becoming a significant problem at high frequencies. A PLL can can solve this problem by multiplying a (relatively) low speed off-chip clock to provide a high speed on-chip clock.

The GSC200 PLL has been designed to use an internal loop stabilization filter. It can be configured to be used in either clock multiplication or clock synchronization modes, and has the following main features:

- Clock multiplication & clock synchronization to either external or internal clocks
- Output clock frequencies from 10MHz to 250MHz
- Phase alignment offset: ±0.3ns
- Phase alignment jitter: ±0.5ns
- Low power consumption: 7mW at 20MHz input, 80MHz output frequency
- Cell area 0.2mm^2
- Low package pin count requirement
- Internal programmable divider for clock multiplication between 1 and 25
- Integrated loop filter
- Operation from 2.7 to 3.6V supplies

Oscillator Cells
The following crystal oscillators are supported:

- 32kHz oscillator
- 1 to 10MHz oscillator
- 10 to 16MHz oscillator
- 16 to 25MHZ oscillator
- 25 to 30MHZ and overtone oscillator

Features
• IDDQ test compatible
• Dual enable pins
  ENB supports power down for Iddq testing
  ENBO power down and input clamp
• Operating range
  Supply voltage: 2.7 to 3.6V
• Overtone operation up to 60MHz supported

CLOCK AND POWER DISTRIBUTION
It is known that large, complex designs working at high speed are vulnerable to problems associated with poor clock and power distribution. Mitel Semiconductor has published design notes that describe approaches to clock and power distribution.

Clock Distribution
The GSC200 series supports a number of clock distribution methodologies which may be implemented depending on the particular design and the CAD tools being used by the designer. For small designs with a light clock load, a single large buffer may be sufficient. For large designs, with large clock loads, a clock grid or clock tree is recommended to avoid clock skew and metal electromigration in the clock network. Clock trees can either be synthesized or manually specified as a clock hierarchy by the designer.

The GSC200 Series clock grid methodology uses up to three stages of buffers, where each stage drives a grid which feeds the next stage cells (Fig. 2).
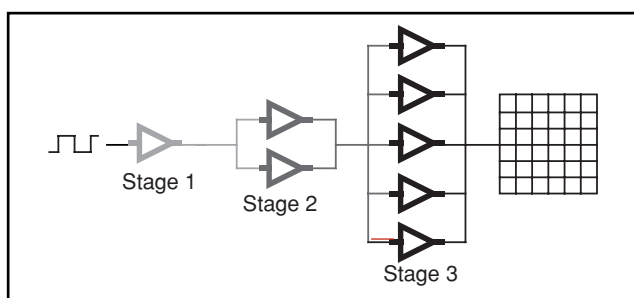

Fig. 2

The final stage grid is a starting point for routing to the actual clocked inputs. Fig. 3 illustrates each buffer stage, which is generated at layout.

Power Distribution
GSC200 can be used from 1.8 to 3.3V, giving great flexibility of supply voltage. Core supply can be chosen from a nominal 2V or 3.3V, with mixed voltage I/O available if the core supply is 2V. I/O cells are available as either CMOS or TTL compatible for all supply configurations.
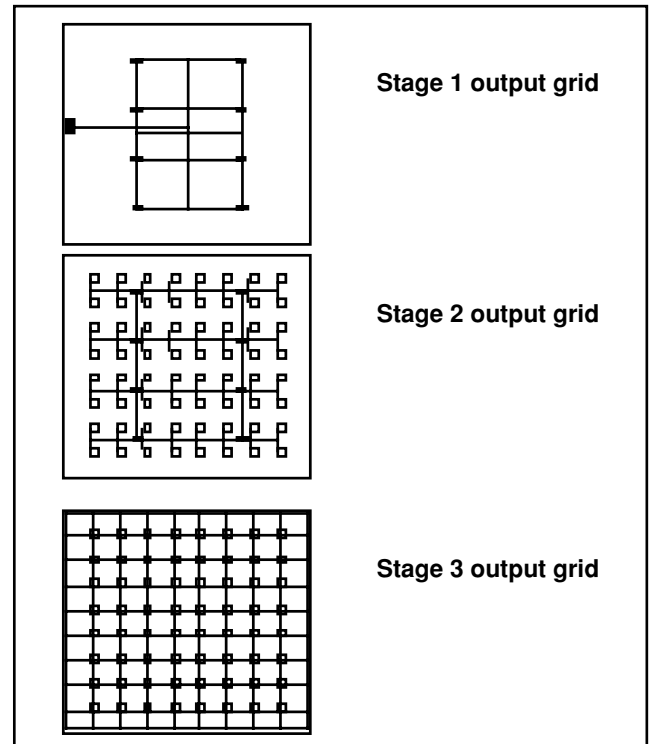

Stage 1 output grid

Stage 2 output grid

Stage 3 output grid

Fig. 3

The GSC200 series utilises a grid methodology for power distribution. This grid, which is automatically constructed during layout, uses metal layers one and three for horizontal power rails and metal layer two for vertical connections. Metal layer four is also available for vertical connections, which may be useful on some larger devices. Methods of implementation are available for use with flat layout, manual methods, or hierarchical layout.

Advanced Delay Modelling
Delay calculation includes the following features:

• Edge speed modelling
• Pin to pin timings
• Non-linear delay modelling
• Accurate delay derating
• Conditional delay modelling

Pin to Pin Delays
Delay models use times between individual input and output pins for both rising and falling delays, as illustrated in Fig. 4 below.
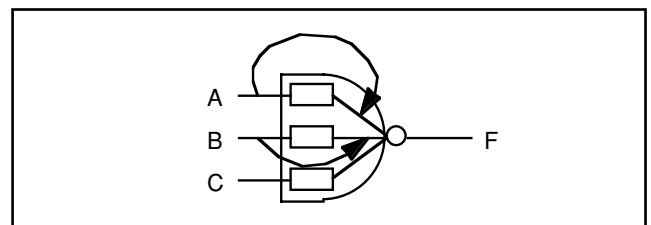

Fig. 4

Calculation uses individual pin to pin delays, e.g. A to F and B to F, which improves simulation accuracy by modelling the considerable variation in delay between different input pins. For complex gates (e.g. AND-NOR gates or adders) the variation is up to 40%. For simple NAND and NOR logic gates the typical variation is 20%.

Non-linear delay modelling

For fast input edges (0.5ns) delay time increases linearly with the output load, whereas for high output loads delay increases linearly with edge speed. Delays for slow input edges and light input loads do not follow the linear model, so a simple linear model cannot represent delays accurately. A more complex equation, which includes interaction between edge and load factors, is used to model delays.

Thermal Management

The increase in speed and density available through advanced CMOS processes results in a corresponding increase in power dissipation. Designs can now have more than half a million used gates and chip power consumption is an important issue.

The GSC200 series offers the following:
• Lower power CMOS for improved thermal management
• Software constructed power grids for efficient power distribution
• Copper lead frame QFPs for lower thermal resistance
• High pinout power packages

DESIGN SUPPORT

Mitel Semiconductor offers flexible design support allowing customers a wide choice of design interfaces. Whichever design interface is chosen each customer design is supported fully by an applications engineer with software support from the Mitel Semiconductor group that produces the design kits. Four main design interfaces are supported. These are described in Table 2 below.

The design process incorporates an audit procedure to verify compliance and to ensure manufacturability. The procedure includes three design reviews held at key stages of the design process to ensure device performance and timescales.

Design Review 1: Held at the beginning of the design cycle to check and agree on performance, packaging, specification and design time scales

Design Review 2: Held after logic simulation but prior to layout to ensure satisfactory functionality, timing performance and adequate fault coverage

Design Review 3: Held after layout and post layout simulation verification. This checks correct performance with actual track loads. This is the final check of all device specifications prior to prototype manufacture

CAE SUPPORT

The GSC200 series is supported by comprehensive design kits for industry standard design tools, including Mentor Graphics, Cadence Design Systems, and Synopsys. A VITAL-compliant library is also available.

Features of design kits include:

• Sign-off simulation with Mentor or Cadence
• VITAL sign-off with Synopsys VSS
• Full top-down design flow support
• Synthesis with Synopsys, Mentor or Cadence
• Electrical Rule Checks (ERC)
• Paracell Model Generator (PMG)
• VIEWLOGIC VCS simulator supported
• Sunrise ATPG supported
• Advanced Pin-to-Pin Delay modelling
• Direct routes to layout and test

Use of the Mitel Semiconductor design kits for sign-off enables customers to sign-off their design without the need to re-simulate on a golden simulator. This has the benefit of customers not having to learn new tools. There is also no overhead in engineering effort or time taken rechecking simulation results.

Interface	Description
1	Netlist interface. Customer completes logical design and simulation using a Mitel Semiconductor design kit. Mitel Semiconductor performs layout only.
2	Technology mapping. Mitel Semiconductor converts a customer-supplied netlist created using a non-Mitel Semiconductor library (e.g., FPGA or other vendor's library) and simulates using customer-supplied test patterns. The production test program is based on these test patterns. Mitel Semiconductor performs layout.
3	Layout interface. Customer completes logical design and simulation. Customer performs layout.
4	Turnkey. Mitel Semiconductor completes schematic capture or logic synthesis or both based on a paper schematic or specification or VHDL or Verilog description. Mitel Semiconductor performs layout.

Table. 2 Design interfaces

CORE CELL LIBRARY

Most core cells have a number of drive variants. The large number of functions and variety of drive strengths for each logic function helps synthesis produce an optimum gate-level implementation of a design. The following table is a list of basic functions:

Inverter
Noninverting buffer
Tristate inverting buffer
Tristate noninverting buffer
2-input NAND
2-input NAND with one inverting input
3-input NAND
3-input NAND with one inverting input
4-input NAND
4-input NAND with one inverting input
4-input NAND with two inverting inputs
2-input NOR
2-input NOR with one inverting input
3-input NOR
3-input NOR with one inverting input
4-input NOR
4-input NOR with one inverting input
4-input NOR with two inverting inputs
2-input AND
3-input AND
4-input AND
2-input OR
3-input OR
4-input OR
2-input AND into 2-input NOR
2-input AND with inverting inputs into 2-input NOR
Two 2-input ANDs into 2-input NOR
Two 2-input ANDs (one with inverting inputs) into 2-input NOR
3-input AND into 2-input NOR
3-input AND and 2-input AND into 2-input NOR
Two 3-input ANDs into 2-input NOR
2-input AND into 3-input NOR
Two 2-input ANDs into 3-input NOR
Three 2-input ANDs into 3-input NOR
2-input OR into 2-input NAND
2-input OR with inverting inputs into 2-input NAND
Two 2-input ORs into 2-input NAND
Two 2-input ORs (one with inverting inputs) into 2-input NAND
3-input OR into 2-input NAND
One 3-input OR and one 2-input OR into 2-input NAND
Two 3-input ORs into 2-input NAND
2-input OR into 3-input NAND
Two 2-input ORs into 3-input NAND
Three 2-input ORs into 3-input NAND
2-input exclusive NOR
2-input exclusive OR
2-bit half adder
2-bit full adder
2-input multiplexer with inverting output
2-input multiplexer
4-input multiplexer with inverting output
4-input multiplexer
Active high D-type transparent latch
Active high D-type transparent latch with active low asynchronous reset
Active high D-type transparent latch with active low asynchronous set
Active high D-type transparent latch with active low asynchronous set and reset
Active low D-type transparent latch
Active low D-type transparent latch with active low asynchronous reset

Active low D-type transparent latch with active low asynchronous set
Active low D-type transparent latch with active low asynchronous set and reset
High-speed, positive-edge triggered, static D-type flip-flop
High-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low reset
High-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set
High-speed, positive-edge triggered, static D-type flip-flop with asynchronous active-low set and reset
Positive-edge triggered, static D-type flip-flop
Positive-edge triggered, static D-type flip-flop with asynchronous active-low reset
Positive-edge triggered, static D-type flip-flop with asynchronous active-low set
Positive-edge triggered, static D-type flip-flop with asynchronous active-low set and reset
Negative-edge triggered static D-type flip-flop
Negative-edge triggered static D-type flip-flop with asynchronous active-low reset
Negative-edge triggered static D-type flip-flop with asynchronous active-low set
Negative-edge triggered static D-type flip-flop with asynchronous active-low set and reset
High-speed positive-edge gritted static D-type flip-flop with scan input and active-high scan enable
High-speed positive-edge triggered static D-type flip-flop with scan input (SI) and active-high scan enable with asynchronous active-low reset
High-speed positive-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low set
High-speed positive-edge triggered static D-type flip-flop with scan input and active-high scan enable
Positive-edge triggered static D-type flip-flop with scan input and active-high scan enable
Positive-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low reset
Positive-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low set
Positive-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low set and reset
Negative-edge triggered static D-type flip-flop with scan input and active-high scan enable
Negative-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low reset
Negative-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low set
Negative-edge triggered static D-type flip-flop with scan input and active-high scan enable with asynchronous active-low set and reset
Positive-edge triggered JK flip-flop
Positive-edge triggered JK flip-flop with asynchronous active-low reset

Positive-edge triggered JK flip-flop with asynchronous active-low set
Positive-edge triggered JK flip-flop with asynchronous active-low set and reset
RS latch with active-high set and reset
RS latch with active-low set and reset
Delay
Long delay
Cell to hold data on a tristate bus
Fast rise noninverting buffer
Fast rise 2-input AND gate

DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage (VDD)	-0.5	5.0	V
Bias for 5V tolerant cells (VBIAS)	-0.5	7.0	V
Input Voltage	-0.5	VDD + 0.5	V
Output Voltage	-0.5	VDD + 0.5	V
Static Discharge (HBM)		2	kV
Storage Temperature Plastic	-55	125	°C

Table. 3

Exceeding the absolute maximum ratings may cause permanent damage to the device. Extended exposure at the maximum ratings will affect device reliability. HBM stands for Human Body Model.

NORMAL OPERATING CONDITIONS

Parameter	Min	Max	Units
Supply Voltage (VDD)	1.8	3.6	V
Bias for 5V tolerant cells (VBIAS)	4.5	5.5	V
Input Voltage	0.0	VDD	V
Input Voltage on 5V Tolerant inputs with VDD 3 @ $\geq$2.7V	0.0	VBIAS	V
Output Voltage	0.0	VDD	V
Input Voltage on tristated 5V tolerant I/O cells with VDD 3 @ $\geq$2.7V	0.0	VBIAS	V
DC Current per Bond Pad		30	mA
Ambient Temperature- Commercial	0	70	°C
Industrial	-40	85	°C
Military	-55	125	°C

Table. 4

DC ELECTRICAL SPECIFICATION

Typical characteristics are at 3.3V, 25°C and typical processing. Min and Max values are defined over all process conditions, from -40 to +85°C and between 3.0 and 3.6V unless otherwise stated.

Parameter	Value			Units	
	Min.	Typ.	Max.		
Input Loads					
Input Leakage			±1	µA	No Pull Up/Down, VDD = 3.6V
Output (Tristate) Leakage	-	-	1	µA	No Pull Up/Down, VDD = 3.6V
Input Capacitance		5		pF	Not including package
Output Capacitance 01, 03, 06	-	5	-	pF	Not including package
Output Capacitance x12	-	10	-	pF	Not including package
Weak Pull-Up Current		-30		µA	Input at 0V
Weak Pull-Down Current		30		µA	Input at VDD
Input Hold Cell - HD					
Hold-Up Current		-24		µA	@ 55% of VDD
Hold Threshold		1.48		V	@ 3.3V
Hold-Down Current		19		µA	@ 30% of VDD
CMOS & TTL Input Levels					
All Cells Types					
CMOS - Vil	-	-	0.3 VDD	V	1.8V < VDD < 3.6V
CMOS - Vih	0.7 VDD	-	-	V	1.8V < VDD < 3.6V
TTL - Vil	-	-	0.8	V	3.0V < VDD < 3.6V
TTL - Vih	2.0	-	-	V	3.0V < VDD < 3.6V
Vt- negative Schmitt threshold	-	1.2	-	V	@ 3.3V
Vt+ positive Schmitt threshold	-	1.6	-	V	@ 3.3V

Table. 5

CMOS and TTL Output Levels

	Parameter	Min	Typ	Max	Units	Conditions
CMOS	Vol Voh	 0.8 VDD		0.2 VDD 	V	1.8V < VDD < 3.6V
TTL	Vol Voh	 2.4V		0.4 	V	3.0V < VDD < 3.6V

Table. 6

Note: These figures apply to all speeds and output current conditions are given in the Table. 9 below.

Output Currents

	Drive Strength							
	x01		x03		x06		x12	
Device Voltage	I_{ol}	I_{oh}	I_{ol}	I_{oh}	I_{ol}	I_{oh}	I_{ol}	I_{oh}
1.8V < VDD < 2.2V	1mA	1mA	3mA	1.5mA	6mA	3mA	12mA	6mA
2.2V < VDD < 2.7V	1mA	1mA	4mA	3mA	8mA	6mA	16mA	12mA
2.7V < VDD < 3.3V	2mA	*2mA	5mA	5mA	10mA	10mA	20mA	20mA
3.0V < VDD < 3.6V	2mA	2mA	6mA	6mA	12mA	12mA	24mA	24mA

Table. 7

*1.5mA for 5V tolerant push-pull cells.

Note: These figures apply to all available speeds.

MANUFACTURING

The GSC200 Series product is manufactured in Mitel Semiconductor advanced wafer fabrication facility near Plymouth, England. This facility is a purpose-built, vibration-free facility equipped with the latest automated technology for 8 inch wafer processing. This equipment utilises mini-environments together with the use of SMIF boxes to achieve ultra clean processing conditions. Computer aided manufacture ensures production efficiency. In addition to the world class wafer fabrication facility, the probe and final test areas are equipped with the latest analog and digital testers. Mitel Semiconductor is committed to continuous investment to provide state-of-the-art CMOS ASICs.

A qualified second source for this silicon process is also available.

QUALITY AND RELIABILITY

At Mitel Semiconductor, quality and reliability are built into the product by statistical control of all processing operations and by minimising random uncontrolled effects in all manufacturing operations. Process management involves full documentation of procedures with recording of batch by batch data using computerised WIP tracking systems.
A common information management system is used to monitor the manufacturing of Mitel Semiconductor CMOS processes and operations. All products benefit from the use of this integrated monitoring system resulting in the highest quality standards for all technologies.

Further information and reliability results are contained in the Quality MOS brochure, available from Mitel Semiconductor Customer Service Centres.

PACKAGING

The GSC200 Series is available in a wide range of metric quad flat packages (MQFP) and plastic ball grid array packages (BGA). The tables below show the preferred packaging range at the time of preparing this datasheet. Detailed package specifications are available from Mitel Semiconductor Design Centres on request. Additional packages are being regularly added to this list, so if a particular package is not listed, please enquire through your Mitel Semiconductor sales representative. Stock is held of preferred packages to ensure a fast prototype assembly turn around.

PLASTIC QUAD FLAT PACKS - SURFACE MOUNT

Code	Lead Count	Body Size*	Lead Pitch	Description
GP	44	10 x 10 x 2.0	0.80	GP - gull wing metric quad flat pack
	64	10 x 10 x 1.4	0.50	
	64	14 x 14 x 2.0	0.80	
	80	14 x 14 x 1.4	0.65	
	80	14 x 20 x 2.8	0.80	
	100	14 x 14 x 1.4	0.50	
	100	14 x 20 x 2.8	0.65	
	120	28 x 28 x 3.4	0.80	
	128	28 x 28 x 3.4	0.80	
	144	20 x 20 x 1.4	0.50	
	144	28 x 28 x 3.4	0.65	
	160	24 x 24 x 1.4	0.50	
	160	28 x 28 x 3.4	0.65	
	176	24 x 24 x 1.4	0.50	
	208	28 x 28 x 3.4	0.50	

Table. 8

PLASTIC BALL GRID ARRAYS (OMPAC STYLE) - SURFACE MOUNT

Code	Lead Count	Body Size*	Lead Pitch	Description
BP	169	23 x 23 x 1.73	1.50	
	225	27 x 27 x 1.73	1.50	
	256	27 x 27 x 1.73	1.27	
	313	35 x 35 x 1.73	1.27S	
	352	35 x 35 x 1.73	1.27	

Table. 9

All dimensions are in millimetres

SYSTEMBUILDER HARD MACROFUNCTIONS

Complex Programmable Cores

- **ARM7TDMI** (Thumb) 16/32 bit RISC Core
- **OakDSPCore** (16-bit)
  (Release to SystemBuilder: Q4 1998)

Memory

- ROMs (size can be specified in software)
- SPRAMs (size can be specified in software)
- DPRAMs (size can be specified in software)

Analog Functions

- Current Reference
- Bandgap References
- Voltage Multiplier
- Power-on-Reset
- 9-bit Video DAC
- 8 bit Control DAC
- 8-bit ADC 10MS/s
- 8-bit Control ADC

LICENCES FOR HARD MACROFUNCTIONS

SystemBuilder hard macrofunction blocks are supplied to customers only as behavioural models. The actual Intellectual Property (IP) is encapsulated in the mask data, which Mitel Semiconductor adds at the layout stage.

Mitel Semiconductor has all the necessary licences to be able to offer the hard macrofunction blocks to customers without signing any additional agreements.

SYSTEMBUILDER SYNTHESISABLE MACROFUNCTIONS

Standard Microprocessor Cores

- **8042**
- **8048**
- **8051**
- **8052**
- **8086**
- **Z80**

Standard Microprocessor Peripheral Cores

- **82C206**   Integrated Peripherals Controller
- **8237A**   4 Channel DMA Controller
- **8253**   3 Channel Prog. Interval Timer
- **8254**   3 Channel Prog. Interval Timer
- **6845**   CRT Controller
- **146818**   Real Time Clock
- **8259A**   8 Ch. Prog. Interrupt Controller
- **8255**   Prog. Peripheral Interface

Bus-based Microcontroller Macrofunctions

- Test/Diagnostic Module
- Bus arbiter cell
- ARM7TDMI Core-to-bus interface
- 2 channel multi-mode DMA Controller
- Interrupt Controller
- Memory/Peripheral Controller
  (for 8-, 16-, or 32 bit external buses)
- UART

- Power Control Module
- Versatile Programmable Peripheral I/F (parallel port)
- System Address Decoder
- Dual Timer Counter
- Watchdog Timer

Floppy Disk/Tape Functions

- **FDC**   Floppy Disk Controller (82077SL)
- **765A**   Floppy Disk Controller
- **91C36**   Floppy Disk Data Separator (1.25Mbit/s)
- **91C360**   High Margin Floppy Disk /Tape DataSeparator (1.25Mbit/s)
- **DDS24**   Enhanced Floppy Disk/ Tape Data Separator (2Mbit/s)

Standard Serial Communications Cores

- **85C30**   2 Channel SCC
- **82530**   2 Channel SCC
- **16C450**   UART
- **16C550A**   UART with FIFOs
- **8251A**   USART
- **8250B**   UART
- **8868A**   UART
- **6402**   UART

Bus Interface Cores

- **PCMCIA**   Both Master (82365SL) and Slave interfaces
- **Ethernet**   (79C90)
- **IEEE1284**   Host Parallel Port
- **USB**   Host, hub and peripherals cores
- **PCI**   Both 32- and 64-bit

Because the range of functions available to SystemBuilder customers is subject to regular additions, the lists in this brochure are not complete.

For an up-to-date list, consult your Mitel Semiconductor representative, or visit our Website: http://www.gpsemi.com

The SystemBuilder Licences

Each SystemBuilder soft macrofunction represents a significant amount of design effort, and the resulting IP must be protected.

Mitel Semiconductor has a brief and straightforward agreement for customers to sign which protects the IP.

ZARLINK™
SEMICONDUCTOR

**For more information about all Zarlink products
visit our Web Site at**

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE