Intel® i960® RM/RN I/O Processor

Design Guide

April 2002

Order Number: 273139-004

Contents

Figures

Tables

Revision History

Rev	Date	Description of Changes
004	04/2002	• Changed “Thermal Recommendations” section.
003	08/2000	• Added schematics.
002	06/2000	• Updated Trademarks and Branding. • Updated vendor tables. • Minor text rewrites. • Updated Pinout tables.
1.0	06/1998	• Added reference schematics. • Added debug connector recommendations section. • Added more detailed heat-sink drawings. • Updated heat-sink vendor table.
0.9	12/10/97	Original Document

1.0 Introduction

This design guide addresses design considerations for designing with either the Intel® i960® RN I/O processor or the Intel® i960® RM I/O processor. Where necessary and applicable, differences in design constraints between the two processors is clarified.

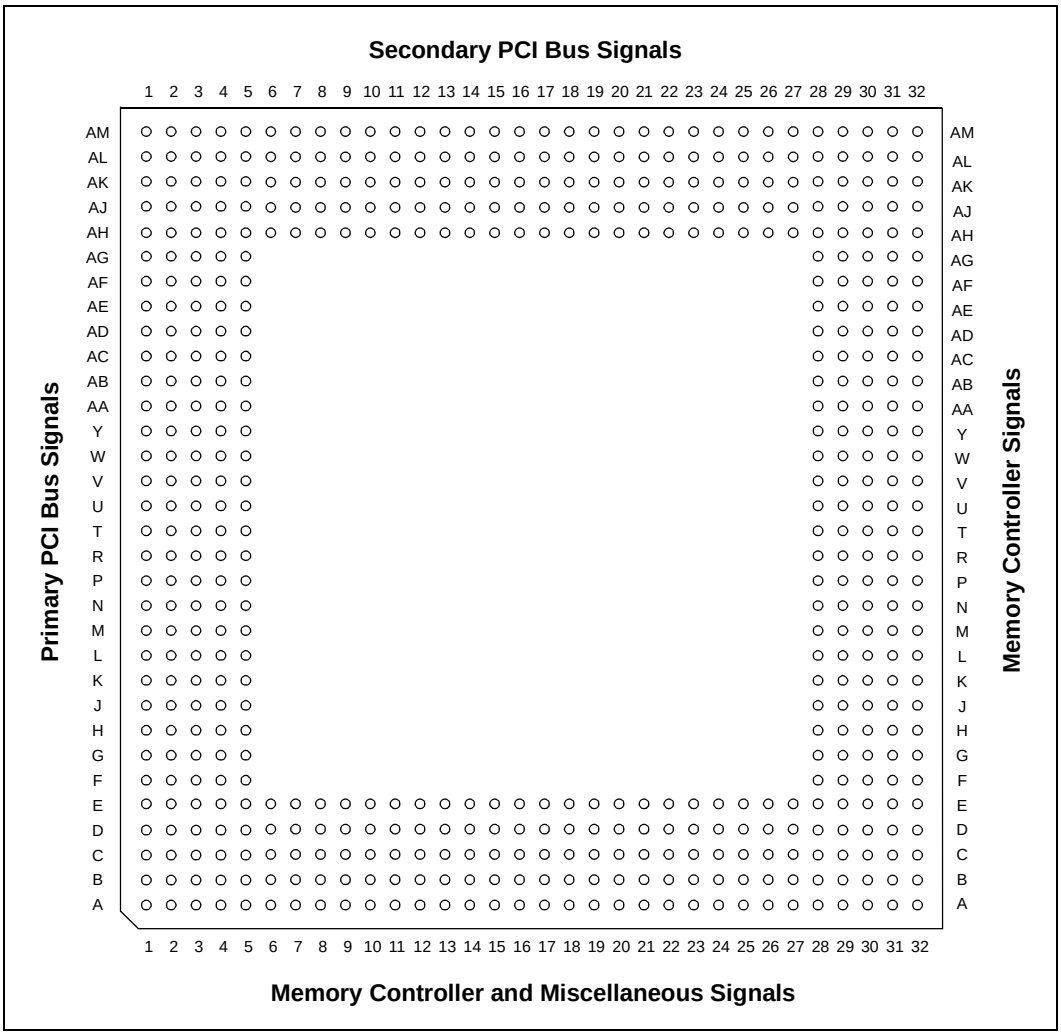
The i960 RN I/O Processor is an Intel I/O processor supporting both 64-bit and 32-bit PCI operation. The i960 RM I/O Processor is an Intel I/O processor only supporting 32-bit PCI operation.

2.0 Intel® 80960RM/RN Processor Ball Map

Intel® i960® RM/RN I/O processor signals, by design, are located on the PBGA package to simplify signal routing and system implementation. Figure 2-1 shows the RM/RN I/O processor major signal sections. To simplify routing and minimize the number of cross traces, keep this layout in mind when placing components in your system. Individual signals within the respective groups have also been laid out to minimize signal crossings.

For detailed signal descriptions refer to the *Tuzigoot Processor Target Specification* document. Contact your Intel sales representative to obtain a copy of the document.

Figure 2-1. 540L H-PBGA Diagram (Bottom View)



2.1 Intel® 80960RM/RN Processor PBGA Signal Ball Map

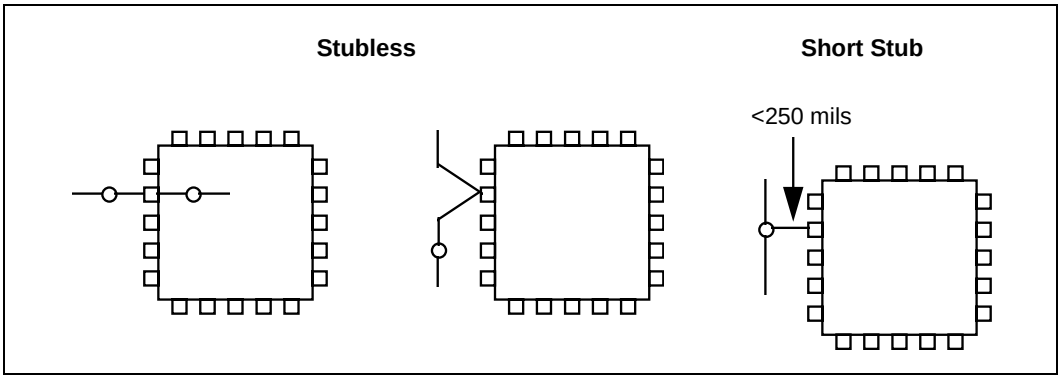
Table F-1 and Table F-2 detail the ballout for the 80960RM and 80960RN processor, respectively. See Appendix F.

3.0 Routing Guidelines

The order in which signals are routed first and last varies from designer to designer. Some prefer to route all clock signals first, while others prefer to route all high speed bus signals first. Either order can be used, provided the guidelines listed here are followed.

Route the RM/RN I/O processor address/data and control signals using a “daisy chain” topology. This topology assumes that no stubs are used to connect any devices on the net. Figure 3-2 shows two possible techniques to achieve a stubless trace. When it is not possible to apply one of these two techniques due to congestion, a very short stub is allowed — preferably not to exceed 250 mils.

Figure 3-2. Examples of Stubless and Short Stub Traces



3.1 Trace Length Limits

For add-in cards, trace lengths from the top of the card edge connector to the RM/RN I/O processor are as follows:

- The maximum trace length for all 32-bit interface signals should not exceed 1.5 inches for 32-bit and 64-bit cards. This includes all signals except those listed as ‘Signal Pins’, ‘Interrupt Pins’, and ‘JTAG Pins’ as per *PCI Local Bus Specification*, Revision 2.1.
- The trace length of the additional signals used in the 64-bit extension are limited to 2 inches on all 64-bit cards.
- The trace length for the PCI CLK signal is 2.5 inches ± 0.1 inch for 32-bit and 64-bit cards and should be routed to only a single load.

4.0 Intel® 80960RM/RN Processor Memory Subsystem

The RM/RN I/O processor integrates a memory controller to provide a direct interface between the RM/RN I/O processor and its local memory subsystem. The memory controller supports:

- Up to 16 Mbytes of 8-bit Flash, ROM, or SRAM
- Between 8 and 128 Mbytes of 64-bit synchronous DRAM (SDRAM)
- Between 4 and 64 Mbytes of 32-bit synchronous DRAM for low cost solutions
- Single-bit error correction, double-bit and nibble detection support (ECC)

The Flash interface provides an 8-bit data bus, 23-bit address bus, and control to support up to two 64 Mbit Bulk-Erase or Boot-Block Flash devices. The Flash devices provide storage for the RM/RN I/O processor initialization code.

The memory controller provides a separate SDRAM interface from the Flash interface. The SDRAM interface consists of a 66 MHz, 64-bit wide data path to support 528 Mbytes/sec throughput. An 8-bit Error Correction Code (ECC) across each 64-bit word improves system reliability.

- The memory controller supports two banks of SDRAM in the form of a single two-bank dual inline memory module (DIMM) or two single-bank DIMMs.
- The memory controller supports a 32-bit SDRAM data interface. This mode enables lower-cost solutions at the cost of system bandwidth.
- The memory controller responds to internal bus memory accesses within its programmed address range and issues the memory request to either the Flash or SDRAM interface.

The memory controller provides four chip enables to the memory subsystem. Two chip enables service the SDRAM subsystem (one per bank) and two service the Flash devices.

Note: If the design does not follow the listed guidelines, then it is very important that the design be simulated. Even if the guidelines are followed it is still recommended that the design be simulated for proper signal integrity, flight time, and cross talk.

4.1 ROM, SRAM, or Flash Guidelines

The RM/RN I/O processor memory controller provides an interface to two banks of static memory ranging from 64 Kbytes to 16 Mbytes. This memory may be SRAM, ROM, or Flash. Optionally, one of the banks may be dedicated to a UART device. Table 4-1 defines all Flash interface signals.

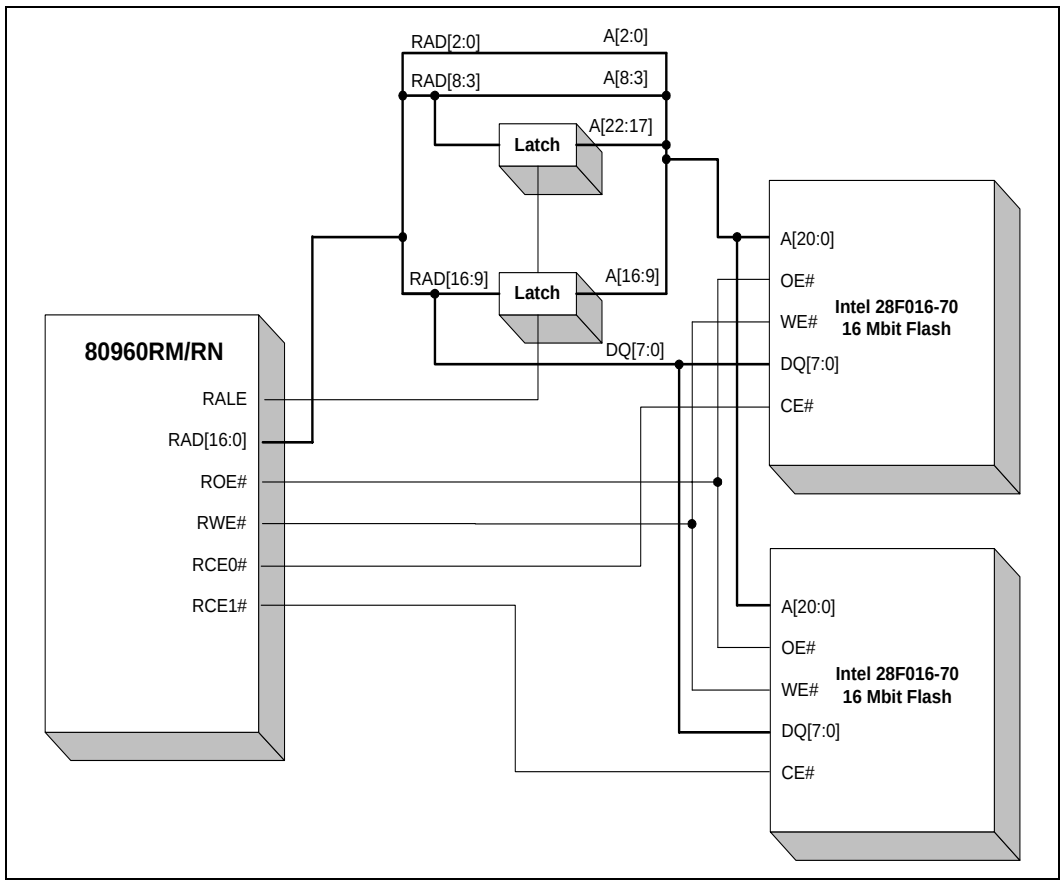
Table 4-1. Flash Interface Signals

Pin Name	Description
RCE[1:0]#	*Chip Enable* - Asserted for all transactions to the Flash device.
RWE#	*Write Enable* - Controls the Flash input data buffers.
ROE#	*Output Enable* - Asserted for reads, deasserted for writes. Controls the Flash output data buffers for write transactions.
RAD[16:0]	*Address/Data bus* - Capable of supporting 16 Mbit of Flash (2Mx8). The data bus is multiplexed on **RAD[16:9]**.
RALE	*Address Latch Enable* - Indicates the transfer of a physical address. **RALE** is asserted during a Flash address cycle and deasserted before the beginning of the data cycle.

4.1.1 Layout Guidelines

Figure 4-3 illustrates how two Flash devices would interface to the RM/RN I/O processor with the memory controller. The Flash subsystem requires an external latch for address and data demultiplexing on **RAD[16:3]**. The data is multiplexed on **RAD[16:9]**.

Figure 4-3. 4 Mbyte Flash Memory System



Flash signal loading should not exceed 50 pF. If the system conforms to I_2O specification, then a minimum 16 Mbit Flash such as Intel's 28F016SA is suggested.

All traces between the RM/RN I/O processor and Flash/SRAM should not exceed 8 inches.

4.1.2 Wait State Profiles

Table 4-2 summarizes various wait state profiles of SRAM and writable non-volatile memory devices.

Table 4-2. ROM, SRAM, or Flash Wait State Profile Programming

Device Speed	Address-to-Data Wait States	Recovery Wait States
≤ 55 ns	4	0
≤ 115 ns	8	4
≤ 175 ns	12	4

4.2 SDRAM Guidelines

The RM/RN I/O processor memory controller supports up to two banks of 66 MHz, 72-bit SDRAM. The memory controller supports 16 Mbit or 64 Mbit technology offering up to 128 Mbytes of ECC protected memory. For low-cost solutions, the memory controller provides a 32-bit SDRAM interface offering up to 64 Mbytes of memory.

Table 4-3 shows the SDRAM interface signals.

Table 4-3. SDRAM Interface Signals

Pin Name	Description
DCLKOUT	*SDRAM Clock Out* - This is the clock to the off-chip SDRAM clock buffer driven by the RM/RN I/O processor. Section 4.2.2 describes the SDRAM clocking strategy.
DCLKIN	*SDRAM Clock In* - This is the clock returning from the off-chip SDRAM clock buffer. Section 4.2.2 describes the SDRAM clocking strategy.
SCKE[1:0]	*Clock enables* - One clock after **SCKE[1:0]** is deasserted, the data is latched on **DQ[63:0]** and **SCB[7:0]**. The burst counters within the SDRAM device are not incremented. Deasserting this signal places the SDRAM in self-refresh mode. For normal operation, **SCKE[1:0]** must be asserted.
SDQM[7:0]	*Data Mask* - On a write, these signals disable the data on a byte-by-byte basis, thus preventing certain bytes from being written. On a read, two clocks after asserting **SDQM[7:0]** the output data bytes from the SDRAM device are disabled.
SCE[1:0]#	*Chip Select* - Must be asserted for all transactions to the SDRAM device. One per bank.
SWE#	*Write Enable* - Controls the SDRAM data input buffers. Asserting **SWE#** causes the data on **DQ[63:0]** and **SCB[7:0]** to be written into the SDRAM devices.
SBA[1:0]	*SDRAM Bank Selects* - Controls which of the internal SDRAM banks to read or write. For 16 Mbit devices (2 banks), only **SBA[0]** is used while 64 Mbit devices use **SBA[1:0]**.
SA[10]	*Address bit 10* - If high during a read or write command, then auto-precharge occurs after the command. During a **row-activate** command, this bit is part of the address.
SA[11:0]	*Address bits 11 through 0* - Indicates the row or column to access depending on the state of **SRAS#** and **SCAS#**.
SRAS#	*Row Address Strobe* - Indicates that the current address on **SA[11:0]** is the row.
SCAS#	*Column Address Strobe* - Indicates that the current address on **SA[11:0]** is the column.
DQ[63:0]	*Data Bus* - 64-bit wide data bus.
SCB[7:0]	*ECC Bus* - 8-bit error correction code which accompanies the data on **DQ[63:0].**

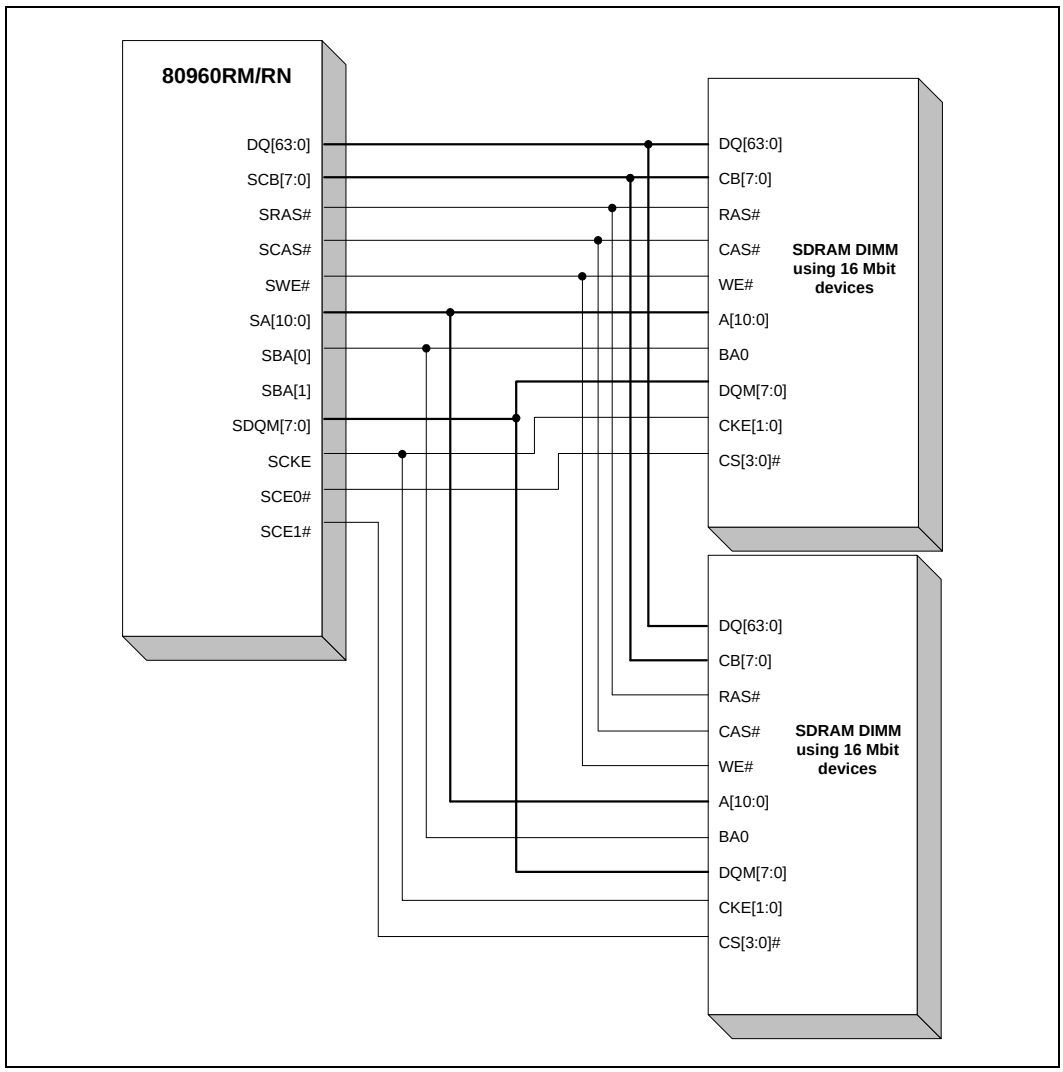
4.2.1 Layout Guidelines

The SDRAM subsystem may be implemented with:

- up to two banks directly connected on the printed circuit board (32, 64, or 72 bits wide)
- up to two 168-pin DIMM sockets (64-bit data bus with or without ECC)
- up to two 144-pin SO-DIMM sockets (64-bit data bus without ECC)

The memory controller supports either one dual-bank DIMM or two single-bank DIMMs. The *4-Clock 66 MHz 72-bit ECC Unbuffered SDRAM DIMM Specification* requires four clock inputs. Figure 4-4 illustrates how two banks of 16 Mbits SDRAM would interface with the RM/RN I/O processor memory controller. **SBA[1]** is only connected for 64 Mbit SDRAM devices. For the clock routing, refer to Figure 4-10.

Figure 4-4. Dual-Bank SDRAM Memory Subsystem



The drive strengths for the SDRAM signals are independently programmable using the SDCR register. Table 4-4 lists some example SDRAM configurations and how the SDCR should be programmed. The RM/RN I/O processor determines the SDRAM configuration with the Serial Presence Detect EEROM (SPD) located on the DIMM. The I^2C bus interfaces the RM/RN I/O processor with the SPD.

Table 4-4. Drive Strength Programmability Options

Bus Width	Memory Size[1] (Mbytes)	Form Factor	Bank 0	Bank 1	SDCR[3] (DQ)	SDCR[4] (CKE0)	SDCR[5] (CKE1)	SDCR[6] (DQM)	SDCR[7] (SA[11:0])
32	4	On-board	2x1M16	None	0	0	0[2]	0	0
	8		4x2M8		0	0	0[2]	0	0
64	8		4x1M16		0	0	0[2]	0	0
	16		8X2M8		0	1	0[2]	0	1
	8	1 Single-sided DIMM	4x1M16		0	0	0[2]	0	0
	16		8x2M8		0	1	0[2]	0	1
	16	1 Double-sided DIMM	4x1M16	4x1M16	1	0	0	1	1
	32		8x2M8	8x2M8	1	1	1	1	1
	16	2 Single-sided DIMMs	4x1M16	4x1M16	1	0	0	1	1
	32		4x1M16	8x2M8	1	0	1	1	1
	24		8x2M8	4x1M16	1	1	0	1	1
	32		8x2M8	8x2M8	1	1	1	1	1
72	16	On-board	9x2M8	None	0	1	0[2]	0	1
	16	1 Single-sided DIMM	9x2M8		0	1	0[2]	0	1
	32	1 Double-sided DIMM	9x2M8	9x2M8	1	1	1	1	1
	32	2 Single-sided DIMMs	9x2M8	9x2M8	1	1	1	1	1

NOTES:
1. The Memory Size column is based on 16 Mbit SDRAM technology. If 64 Mbit SDRAM is populated, then the size will increase appropriately. Each bank's technology may be programmed independently.
2. If one SDRAM bank is unpopulated, then the corresponding **SCKE** and **SCE** is unconnected.

Specific SDRAM signal topologies have been validated for 66 MHz operation. Figure 4-5 through Figure 4-9 illustrate the proven topologies and are recommended. Proper signal integrity analysis should verify any other signal topologies.

To minimize crosstalk, SDRAM signal routing should use a minimum of 4 mils spacing and 4 mils trace width. SDRAM clocks (out of the buffer) should use a minimum of 12 mils spacing and 6 mils trace width.

Figure 4-5. SDRAM DIMM Layout Topology #1

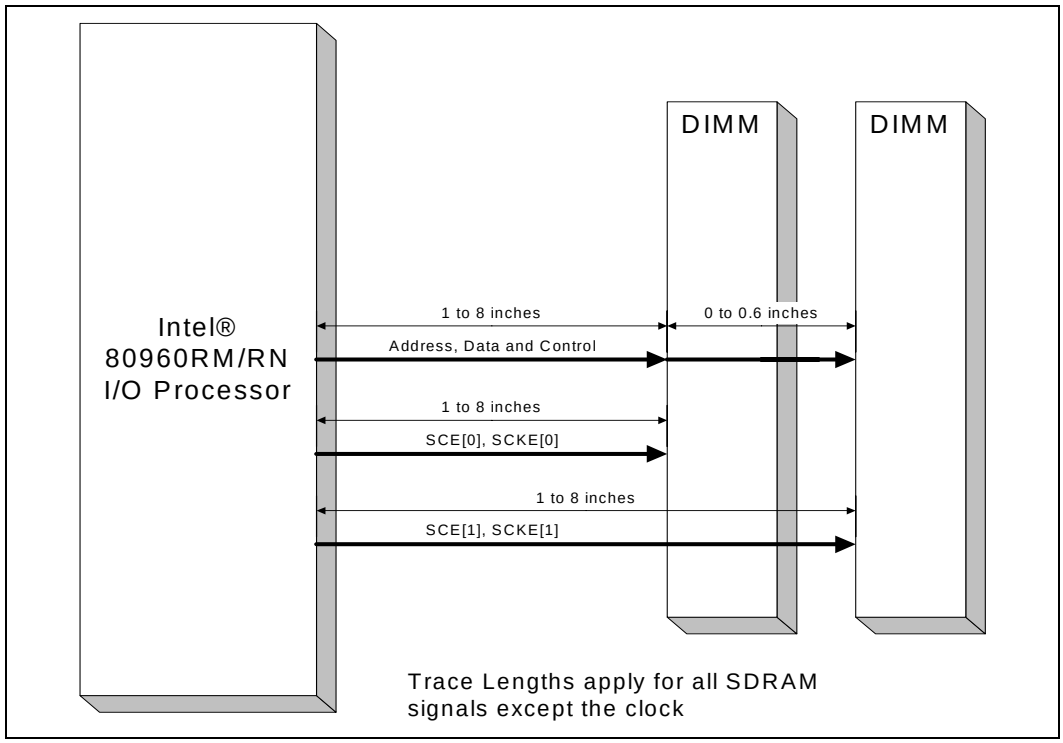


Figure 4-6. SDRAM DIMM Layout Topology #2

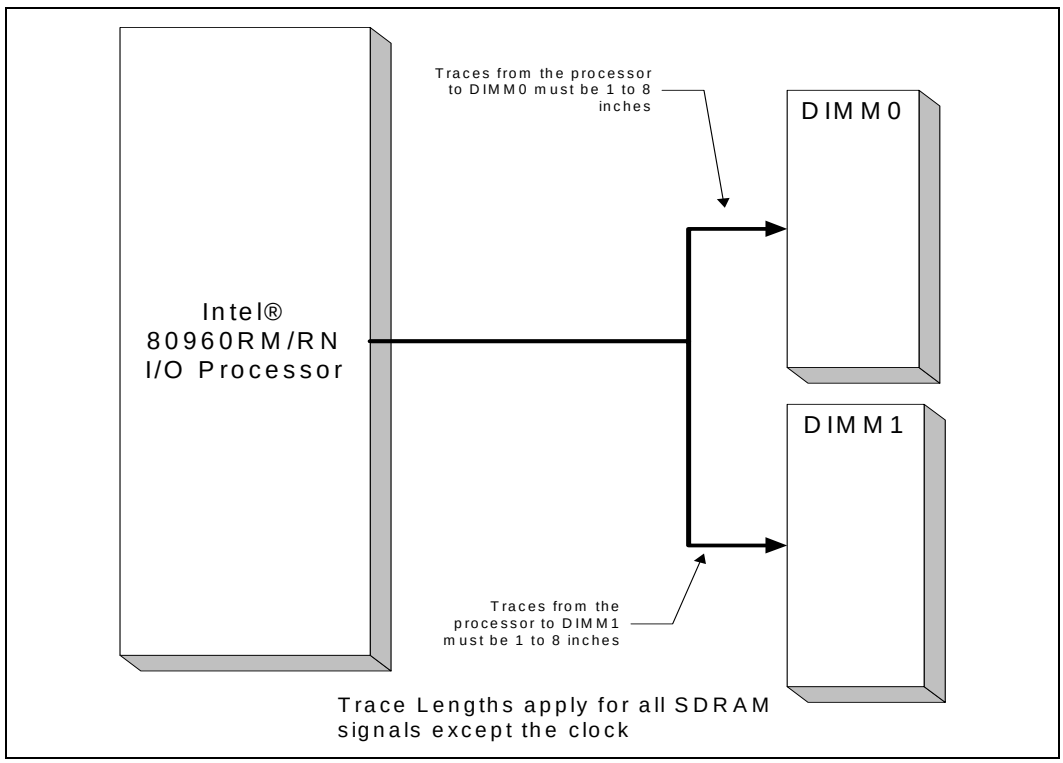


Figure 4-7. Address and Control Topology for Two Discrete SDRAM Devices

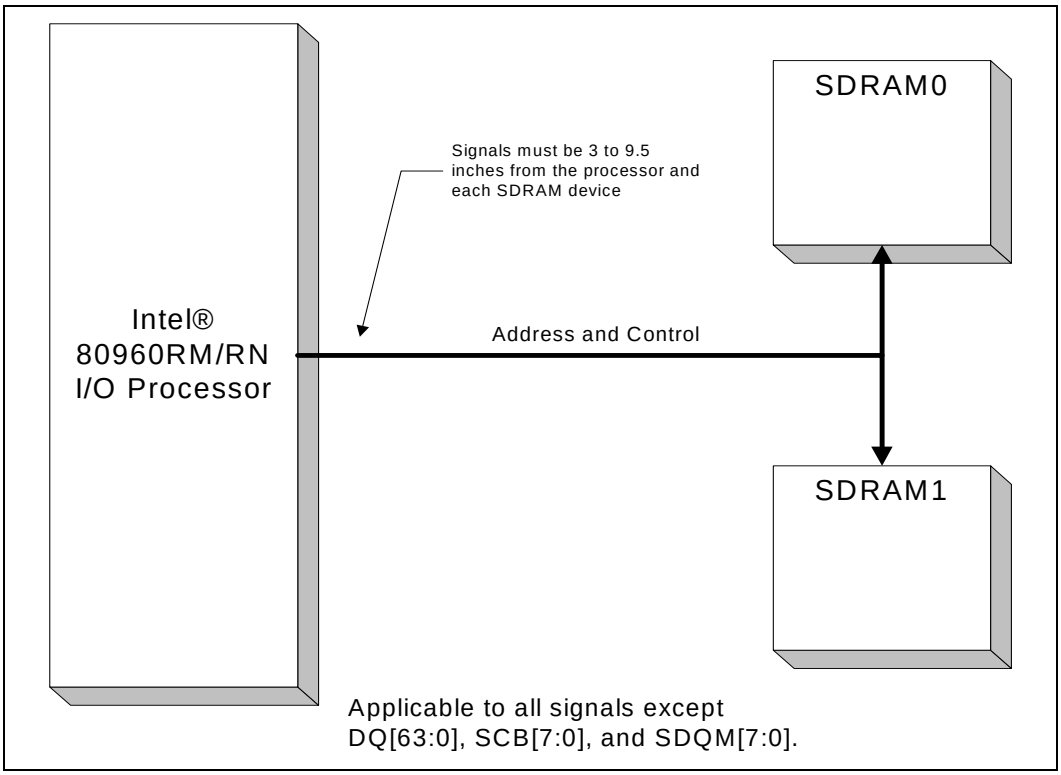


Figure 4-8. Address and Control Topology for Four or More Discrete SDRAM Devices

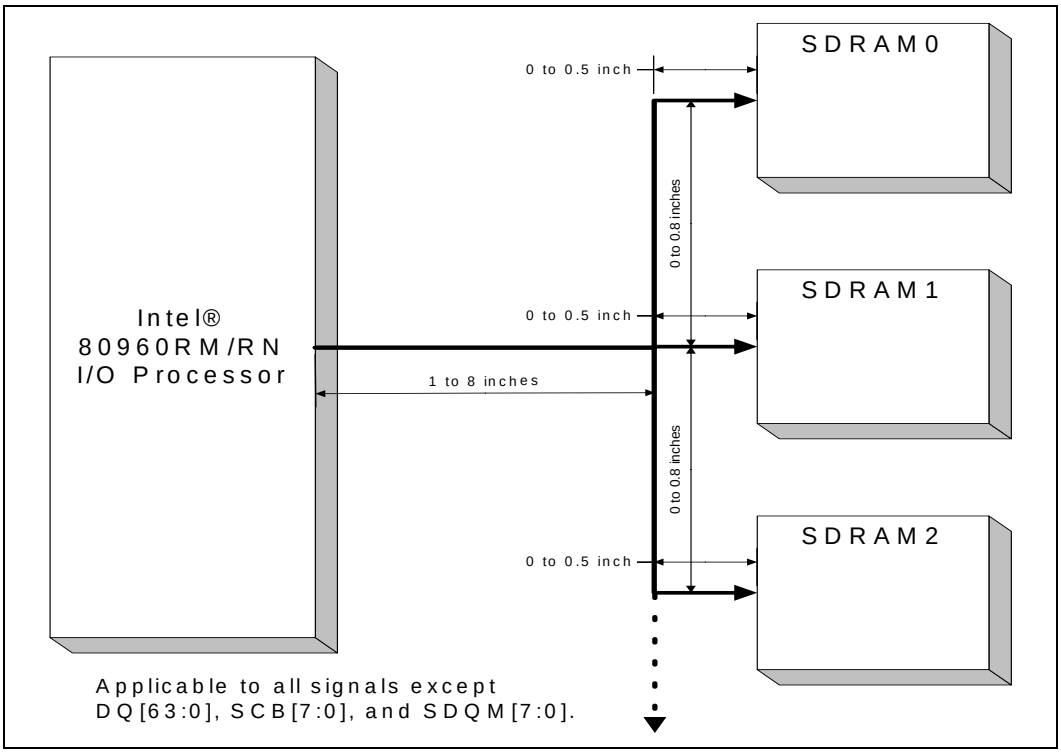
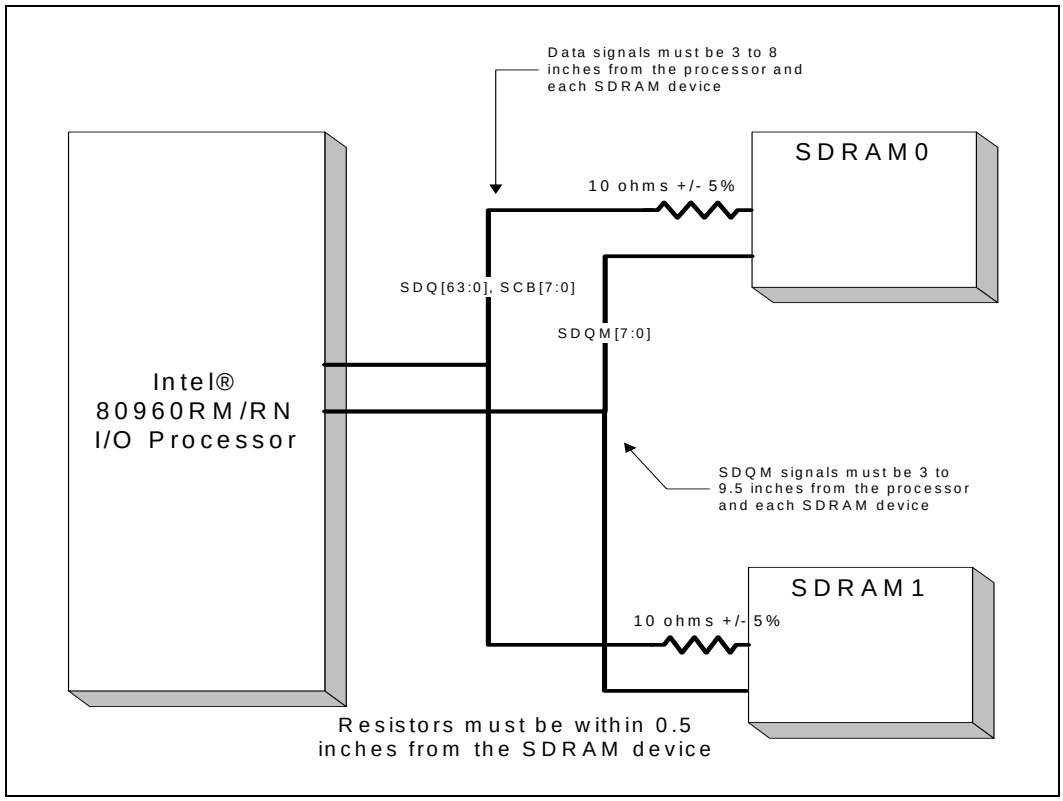


Figure 4-9. Data and DQM Topology for Discrete SDRAM Devices

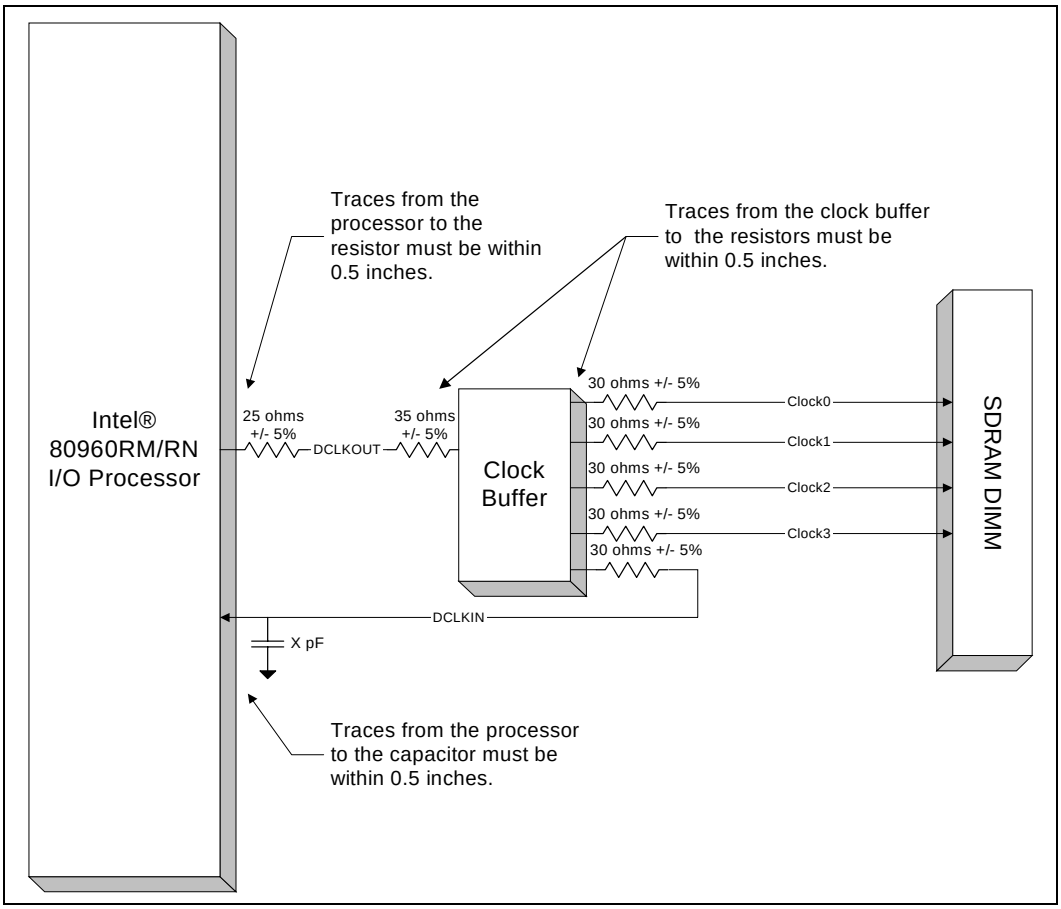


The address and control signals for the SDRAM subsystem include **SA[11:0]**, **SCAS#**, **SCE[1:0]#**, **SCKE[1:0]**, **SRAS#**, and **SWE#**. The SDRAM data signals include **DQ[63:0]**, and **SCB[7:0]**.

4.2.2 SDRAM Clocking and Clock Buffer Specifications

The MCU provides one clock (**DCLKOUT**) to the SDRAM memory subsystem with a 66 MHz frequency. The 72-bit, 2-bank SDRAM DIMM specification requires four clocks to distribute the loading across eighteen x8 SDRAM components. The board designer must buffer **DCLKOUT** external to the RM/RN I/O processor with a Texas Instruments CDC318 or equivalent buffer. Refer to Figure 4-10 for the clock routing diagram. External resistors and capacitors are required for proper signal integrity and clock skew management.

Figure 4-10. Clocking for a Dual-Bank SDRAM DIMM



Note: Any single SDRAM bank will use *two* clock buffer outputs. Four clock buffer outputs are used only when two SDRAM banks are populated.

DCLKOUT and the clock buffer outputs may be between 1 and 8 inches. Each of the four clock buffer outputs must be equal in length. Refer to Table 4-5 for the **DCLKIN** trace length and capacitance requirements. **DCLKIN** requires an external capacitor to match the loading seen on the other clock buffer outputs. *Traces from the processor to the capacitor must be within 0.5 inches.* The **DCLKIN** trace length must be equal to the clock buffer output trace length plus the additional length specified in Table 4-5.

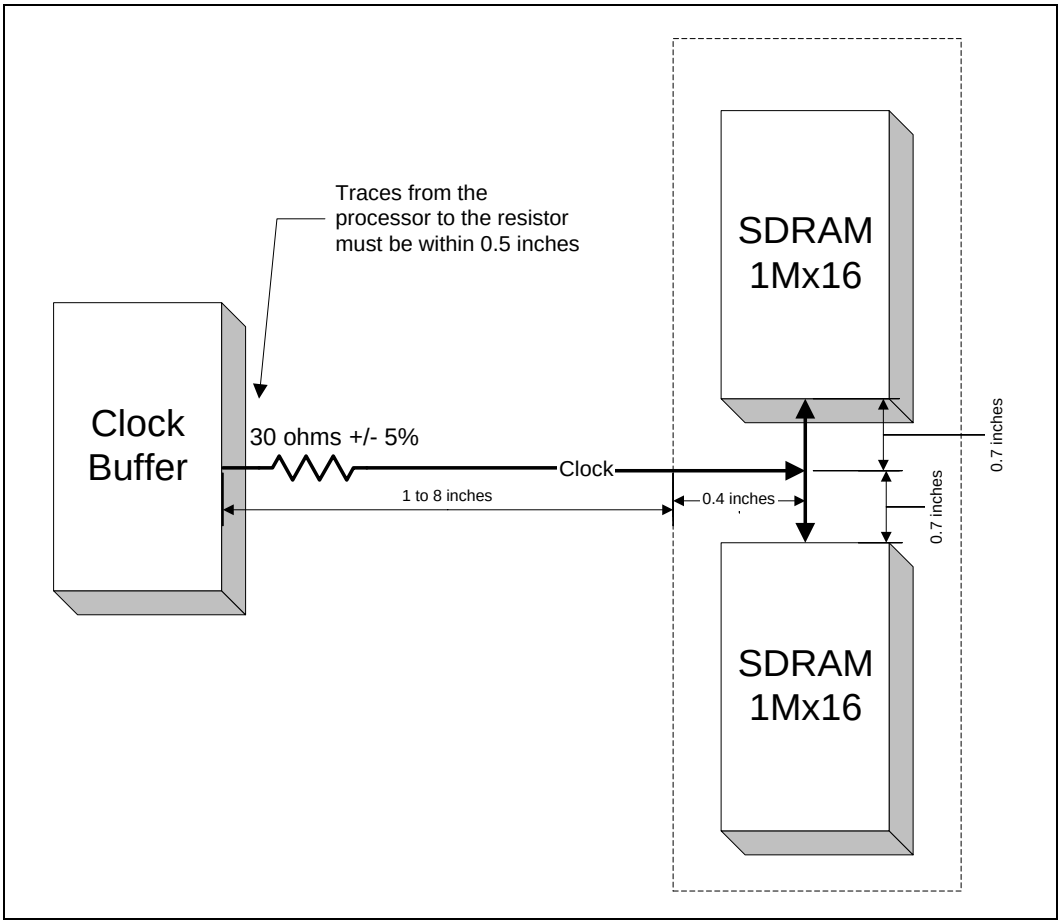
Table 4-5. DCLKIN Routing and Loading Requirements

Memory Configuration	*Additional* DCLKIN Trace Length	DCLKIN Capacitance
168-pin SDRAM DIMM	4.5 +/- 0.1 inches	18 pF
144-pin SO-DIMM	3.4 +/- 0.1 inches	8.2 pF
Two discrete SDRAM devices	1.3 +/- 0.1 inches	3.3 pF
Four discrete SDRAM devices	4.5 +/- 0.1 inches	12 pF
Eight discrete SDRAM devices	4.5 +/- 0.1 inches	12 pF
Nine discrete SDRAM devices	4.5 +/- 0.1 inches	18 pF

Note: The *66 MHz Unbuffered 168-Pin SDRAM DIMM* requires four clock inputs. The lumped capacitance value required on DCLKIN is 18 pf in this reference design.

Any memory configuration using four or more discrete SDRAM components directly on the board must adhere to the same routing requirements specified in the *4-Clock 66 MHz 72-bit ECC Unbuffered SDRAM DIMM Specification*. Figure 4-11 illustrates the routing requirements for the SDRAM input clock when the configuration uses two SDRAM components.

Figure 4-11. Clock Routing for a Two Device SDRAM Subsystem



Suggested clock driver components are listed in Table 4-6. This is neither an endorsement nor a warranty of the performance of the listed product and company.

Table 4-6. SDRAM Clock Buffer Information

Manufacturer	Part Number
Cypress	CY2310NZPVC-1
Motorola	MPC9140SD
Pericom	P16C182
Pericom	P16C180V

4.2.3 SDRAM Power Failure Guidelines

SDRAM technology provides a simple way of enabling data preservation through the **self-refresh** command. When the memory controller issues this command, the SDRAM refreshes itself autonomously with internal logic and timers.

The SDRAM device remains in self-refresh mode as long as:

- The device continues to be powered.
- **SCKE** is held low until the memory controller is ready to control the SDRAM once again.

The board design should ensure power to the SDRAM subsystem with an adequate battery backup and a reliable method for switching between system power and battery power. The memory controller is responsible for deasserting **SCKE[1:0]** when issuing the **self-refresh** command however, while power gradually drops, **SCKE[1:0] MUST** remain deasserted regardless of the state of V_{cc} powering the RM/RN I/O processor.

4.2.4 System Assumptions

The board design should ensure that **P_RST#** is asserted to the RM/RN I/O processor when at least 1 ms of reliable power is remaining. This is required so that the memory controller can execute its power-failure state machine in response to the assertion of **P_RST#**.

4.2.5 External Logic Required for Power Failure

Refer to Figure for a state machine of the external logic required for power failure mode. Actual implementations may vary. This state machine can be implemented in a programmable logic device illustrated in Figure 4-13.

Figure 4-12. External Power Failure State Machine

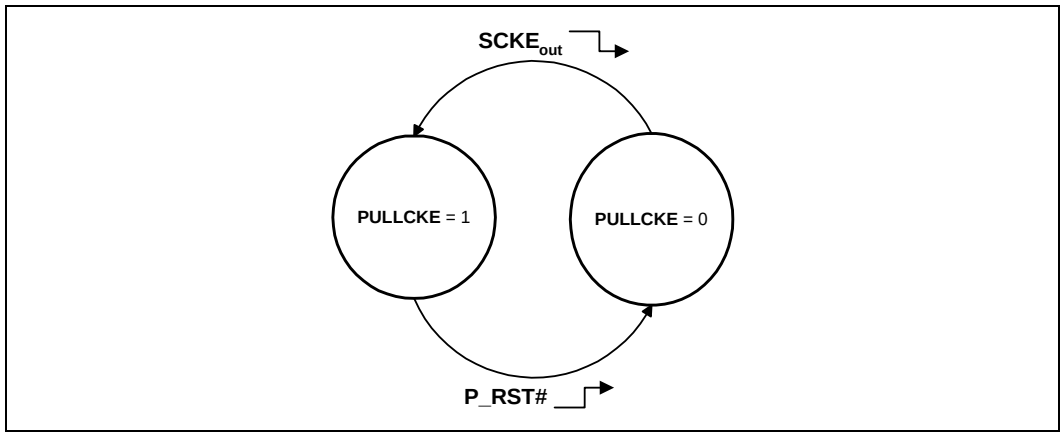
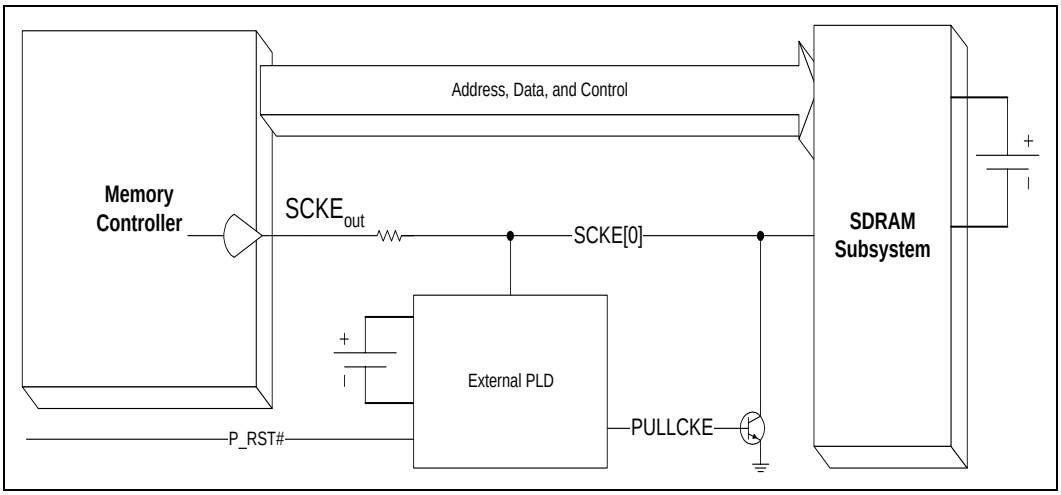


Figure 4-13. External Power Failure Logic in the System



The implementation illustrated in Figure 4-13 requires that all external logic be powered by V_{batt}. The edge detect state machine activates the pull-down when the MCU deasserts **SCKE[1:0]**. As long as V_{batt} is active, **SCKE[1:0]** is held low. Once the memory controller is reset, the rising edge of **P_RST#** deactivates the pull-down. The memory controller will reliably control **SCKE[1:0]** at this point, driving it low. The pull-down is activated within the PLD device. Refer to the IQ80960RM/RN schematics in Appendix E for details.

Note: Figure 4-13 shows logic for one of the **SCKE** signals. The loading of this signal is large enough so that two signals are required (one per SDRAM bank) and the above logic should be replicated for each **SCKE[1:0]**.

5.0 Interrupt Routing

As stated in the *PCI Local Bus Specification,* Revision 2.1 and the *PCI-to-PCI Bridge Architecture Specification,* Revision 1.0, interrupt routing is system-specific. In general, the BIOS maps the device's interrupt line to the RM/RN I/O processor's secondary bus INTx line. The IDSEL address originates from the RM/RN I/O processor's secondary address bus and connects to the device's IDSEL pin or PCI connector slots.

Table 5-7 provides interrupt routing for devices with a single interrupt pin. Multifunction devices, which have more than one interrupt pin, would follow the interrupt routing guidelines shown in Figure 5-14. In this case, replace the connector with the multifunction device.

Table 5-7. Intel® 80960RM/RN Processor Interrupt Routing Signals

Device's IDSEL Signal Pin	Device Interrupt Signal
S_AD16, 20, 24, 28	INTA#
S_AD17, 21, 25, 29	INTB#
S_AD18, 22, 26, 30	INTC#
S_AD19, 23, 27, 31	INTD#

Secondary Address lines **S_AD[25:16]** can be configured for public devices or private devices depending on the Secondary ID Select Register (SISR). **S_AD[31:26]** are for public devices only. When PCI connectors are present on the RM/RN I/O processor's secondary bus, the interrupts rotate on the subsequent PCI connectors as shown in Figure 5-14.

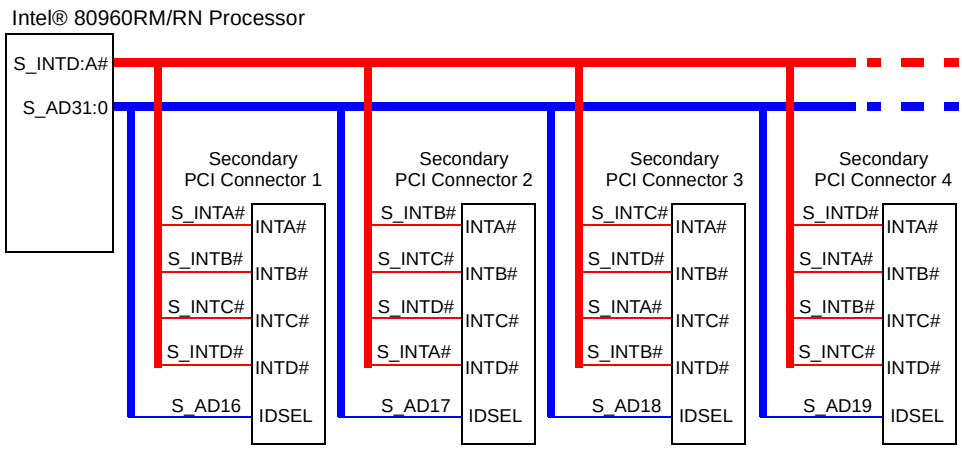
5.1 Intel® 80960RM/RN Processor Implementation on a MotherBoard

When implementing the RM/RN I/O processor onto a motherboard, you must adhere to the Device ID address and interrupt routing scheme used on the primary side of the PCI bus which is dependent on the individual motherboard implementation.

5.2 Intel® 80960RM/RN Processor Implementation on an Add-in Card

When designing the RM/RN I/O processor into an add-in card, refer to Figure 5-14 for Device ID address and interrupt routing.

Figure 5-14. Example Secondary PCI Connector Interrupt Routing



NOTE: Secondary PCI Bus interrupt signals “rotate” on subsequent PCI connectors.

6.0 Clocking Guidelines

RM/RN I/O processor uses P_CLK (synchronous clock) input for clocking. All AC timings on the primary PCI bus and the secondary PCI bus are referenced to the P_CLK input. The system must provide clocks for any devices on the secondary PCI bus and ensure that system level goals for clock skew and jitter are met.

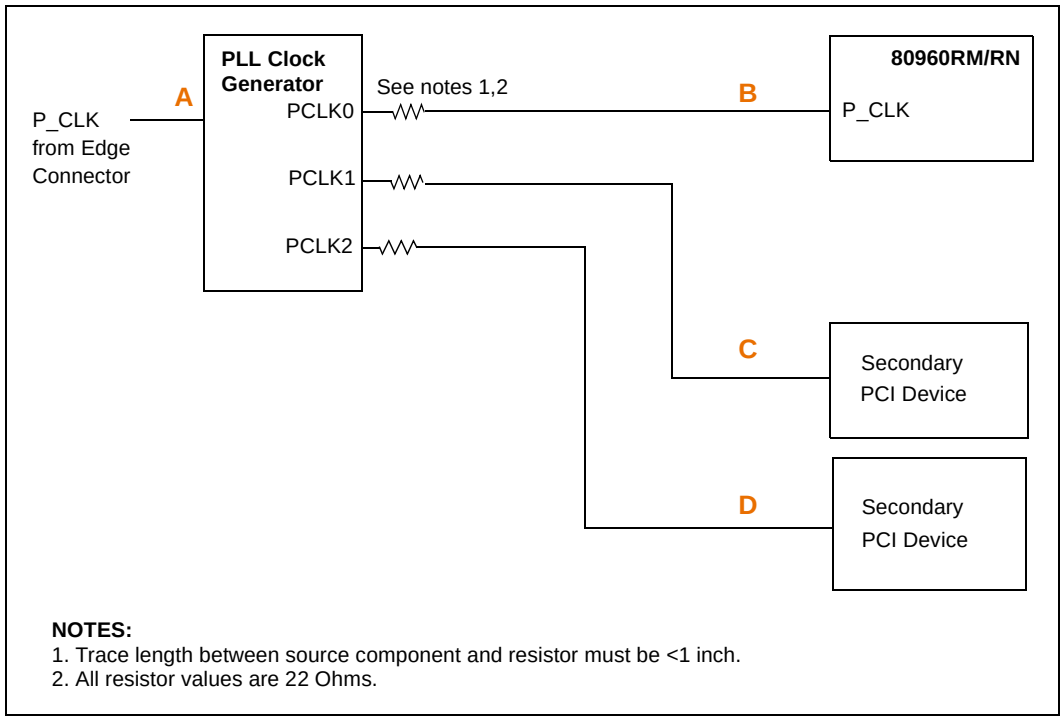
6.1 Layout Guidelines for Add-in Cards

A PCI edge connector provides a singular PCI clock which must only be connected to one load on the add-in card. Add-in cards which contain the RM/RN I/O processor should use a low skew, low jitter clock driver/buffer to make multiple copies of the PCI clock for the RM/RN I/O processor and any devices on the secondary PCI bus. See Figure 6-15. Such clock driver/buffer devices are widely available (typically from Cypress, Motorola, National Semiconductor, etc.)

The PCI bus specification allows a maximum PCI clock skew of 2 ns between any two devices connected on the PCI bus. To minimize skew on the primary PCI bus, place the clock driver device as close as possible to the PCI edge connector. Trace lengths from the PCI edge connector to the clock driver (“A” in Figure 6-15), and from the clock driver to the RM/RN I/O processor P_CLK input (“B” in Figure 6-15) must be as short as physically possible (max length 2.5 inches).

For the secondary PCI bus, allowable skew is 2 ns between the RM/RN I/O processor P_CLK input and any device on the secondary PCI bus. This allows the trace lengths from the clock driver to the secondary PCI clock inputs (“C” and “D” in Figure 6-15) to be longer than the trace to the RM/RN I/O processor P_CLK input to accommodate layout. In general, keep these secondary clock routes shorter than eight inches to provide a skew of less than 2 ns.

Figure 6-15. PCI Add-in Card Example Configuration



6.2 Layout Guidelines for Motherboards

For motherboard implementations, the designer has much more flexibility with PCI clocking, primarily related to controlling the central clock resources. Skew requirements for the motherboard are more stringent due to the uncertainty of having PCI edge connectors on the secondary bus.

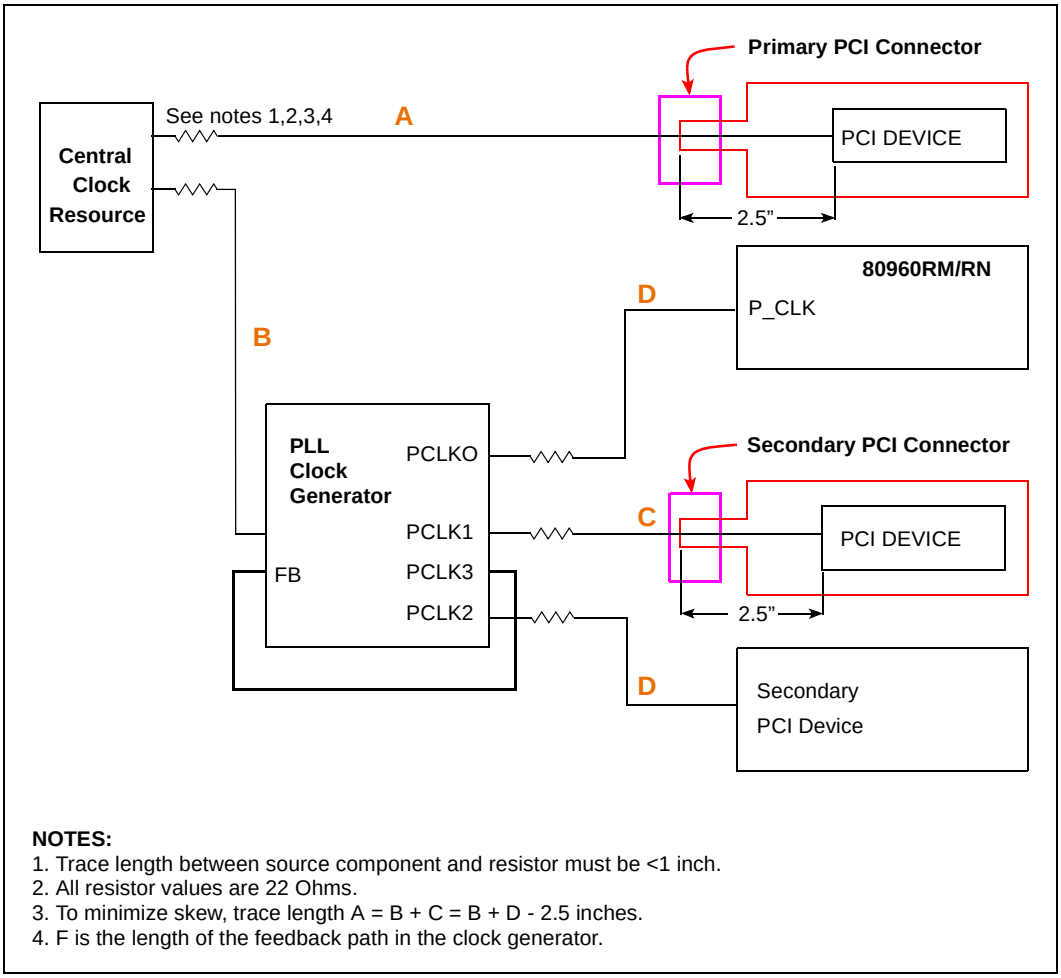
For motherboard implementation designs, it is best to choose a central clocking resource with enough PCI clock outputs to drive all PCI devices in the system, including the RM/RN I/O processor and any PCI devices on the secondary bus. All trace lengths should be equalized to both the primary and secondary PCI devices. If it is not possible to find a central clock resource with enough clock outputs for your design, then use a clock buffer/driver for the secondary PCI bus as shown in Figure 6-16.

To minimize skew for these designs, use the following equation for trace length (see Figure 6-16):

Equation 6-1. A = B + C + F = B + D + F - 2.5 Inches

The total trace length must be under 18 inches. Also, since implementations can be varied, each design must be simulated to meet specifications as per *PCI Local Bus Specification*, Revision 2.1. To minimize skew, clocks to connectors should be 2.5 inches shorter than traces routed to motherboard devices.

Figure 6-16. Motherboard Example Configuration



NOTES:
1. Trace length between source component and resistor must be <1 inch.
2. All resistor values are 22 Ohms.
3. To minimize skew, trace length A = B + C = B + D - 2.5 inches.
4. F is the length of the feedback path in the clock generator.

6.3 Clock Vendors

The low-skew clock buffer components in Table 6-8 are suggested. This is neither an endorsement nor a warranty of the performance of the listed product and/or company.

Table 6-8. Low Skew Clock Buffer Information

Manufacturer	Part Number
Cypress	W217 (new)
Cypress	CY7B9910

7.0 Intel® 80960RM/RN Processor Signals Requiring Pull-Up/Down Resistors

Table 7-9 through Table 7-11 identify the signals that require pull-up and/or pull-down resistors and the recommended resistor values.

Table 7-9. Memory Controller, Core and JTAG Signals

Signal	Resistor Value (in Ohms)	Pull-up or Pull-down	Comments
RAD[6]/RST_MODE#	1.5K	Pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[4]/STEST	2.7K	Pull-up or Pull-down	Pull-up to enable **RAD[4]/STEST**, pull-down to disable.
RAD[3]/RETRY	1.5K	Pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[2]/32BITMEM_EN#	1.5K	Pull-down[2]	Pull-down for 32-bit SDRAM protocol. This signal has an internal pull-up.
RAD[1]/32BITPCI_EN#	1.5K	Pull-down[3]	Pull-down for 32-bit SPCI bus protocol. This signal has an internal pull-up.
NMI#	2.7K	Pull-up	
TRST#	1.5K	Pull-down	Alternatively this signal may be tied to **P_RST#**.

NOTES:
1. Pull-down only if other than default Reset Mode is required.
2. Pull-down only if the memory controller is required to support the 32-bit SDRAM protocol for access to SDRAM memory.
3. Pull-down only if the secondary PCI bus is required to function as a 32-bit bus.

Table 7-10. I^2C Bus Signals

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
SCL	2.7K	pull-up	When I^2C unit is not used
SDA	2.7K	pull-up	When I^2C unit is not used

Table 7-11. PCI Signals (Sheet 1 of 2)

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
S_SERR#	2.7K	pull-up	On Secondary Bus
S_TRDY#	2.7K	pull-up	On Secondary Bus
S_LOCK#	2.7K	pull-up	On Secondary Bus
S_PERR#	2.7K	pull-up	On Secondary Bus
S_DEVSEL#	2.7K	pull-up	On Secondary Bus

Table 7-11. PCI Signals (Sheet 2 of 2)

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
S_ FRAME#	2.7K	pull-up	On Secondary Bus
S_ STOP#	2.7K	pull-up	On Secondary Bus
S_ IRDY#	2.7K	pull-up	On Secondary Bus
S_ INTA#	2.7K	pull-up	On Secondary Bus
S_ INTB#	2.7K	pull-up	On Secondary Bus
S_ INTC#	2.7K	pull-up	On Secondary Bus
S_ INTD#	2.7K	pull-up	On Secondary Bus
XINT4#	2.7K	pull-up	On Secondary Bus
XINT5#	2.7K	pull-up	On Secondary Bus
S_ REQ0#	2.7K	pull-up	On Secondary Bus
S_ REQ1#	2.7K	pull-up	On Secondary Bus
S_ REQ2#	2.7K	pull-up	On Secondary Bus
S_ REQ3#	2.7K	pull-up	On Secondary Bus
S_ REQ4#	2.7K	pull-up	On Secondary Bus
S_ REQ5#	2.7K	pull-up	On Secondary Bus
S_AD[63:32]	2.7K	pull-up	On Secondary Bus
S_C/BE[7:4]#	2.7K	pull-up	On Secondary Bus
S_PAR64	2.7K	pull-up	On Secondary Bus
S_REQ64#	2.7K	pull-up	On Secondary Bus
S_ACK64#	2.7K	pull-up	On Secondary Bus

8.0 Intel® 80960RM/RN Processor Signals Requiring Pull-Up/Down Resistors

Table 8-12 through Table 8-14 identify the signals that require pull-up and/or pull-down resistors and the recommended resistor values.

Table 8-12. Memory Controller, Core and JTAG Signals

Signal	Resistor Value (in Ohms)	Pull-up or Pull-down	Comments
RAD[6]/RST_MODE#	1.5K	Pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[4]/STEST	2.7K	Pull-up or Pull-down	Pull-up to enable **RAD[4]/STEST**, pull-down to disable.
RAD[3]/RETRY	1.5K	Pull-down[1]	Dependent on which reset mode is desired. This signal has an internal pull-up.
RAD[2]/32BITMEM_EN#	1.5K	Pull-down[2]	Pull-down for 32-bit SDRAM protocol. This signal has an internal pull-up.
RAD[1]/32BITPCI_EN#	1.5K	Pull-down[3]	Pull-down for 32-bit SPCI bus protocol. This signal has an internal pull-up.
NMI#	2.7K	Pull-up	
TRST#	1.5K	Pull-down	Alternatively this signal may be tied to **P_RST#**.

NOTES:
1. Pull-down only if other than default Reset Mode is required.
2. Pull-down only if the memory controller is required to support the 32-bit SDRAM protocol for access to SDRAM memory.
3. Pull-down only if the secondary PCI bus is required to function as a 32-bit bus.

Table 8-13. I^2C Bus Signals

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
SCL	2.7K	pull-up	When I^2C unit is not used
SDA	2.7K	pull-up	When I^2C unit is not used

Table 8-14. PCI Signals (Sheet 1 of 2) (Sheet 1 of 2)

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
S_SERR#	2.7K	pull-up	On Secondary Bus
S_TRDY#	2.7K	pull-up	On Secondary Bus
S_LOCK#	2.7K	pull-up	On Secondary Bus
S_PERR#	2.7K	pull-up	On Secondary Bus
S_DEVSEL#	2.7K	pull-up	On Secondary Bus

Table 8-14. PCI Signals (Sheet 2 of 2) (Sheet 2 of 2)

Signal	Resistor value (in Ohms)	Pull-up or Pull-down	Comments
S_ FRAME#	2.7K	pull-up	On Secondary Bus
S_ STOP#	2.7K	pull-up	On Secondary Bus
S_ IRDY#	2.7K	pull-up	On Secondary Bus
S_ INTA#	2.7K	pull-up	On Secondary Bus
S_ INTB#	2.7K	pull-up	On Secondary Bus
S_ INTC#	2.7K	pull-up	On Secondary Bus
S_ INTD#	2.7K	pull-up	On Secondary Bus
XINT4#	2.7K	pull-up	On Secondary Bus
XINT5#	2.7K	pull-up	On Secondary Bus
S_ REQ0#	2.7K	pull-up	On Secondary Bus
S_ REQ1#	2.7K	pull-up	On Secondary Bus
S_ REQ2#	2.7K	pull-up	On Secondary Bus
S_ REQ3#	2.7K	pull-up	On Secondary Bus
S_ REQ4#	2.7K	pull-up	On Secondary Bus
S_ REQ5#	2.7K	pull-up	On Secondary Bus

9.0 Intel® 80960RM/RN Processor 5 V and 3.3 V Design Considerations

9.1 Providing 3.3 V in a 5 V System

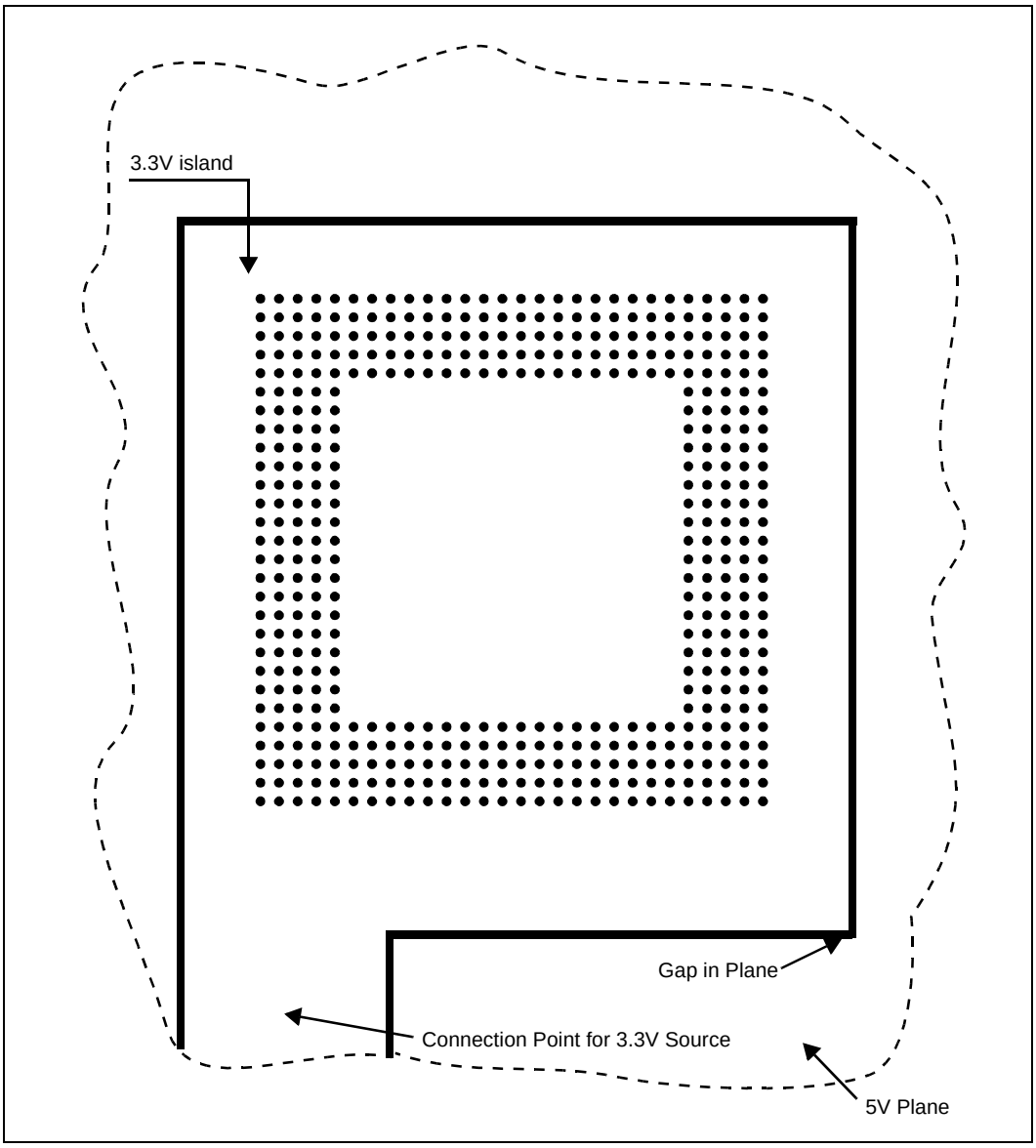
In most system board designs, the 5 V system power supply is routed to board components through a dedicated board layer. With the requirement of a 3.3 V supply for the RM/RN I/O processor, it is not necessary to add a completely new power supply layer to the circuit board. It is possible to create a 3.3 V “island” around the processor in the existing power supply plane.

Figure 9-17 shows a recommended “island” layout. The RM/RN I/O processor 5 V-tolerant input buffers and TTL-compatible outputs allow the processor to interface with existing TTL-compatible external logic, without requiring extra components. Thus, the processor runs at 3.3 V and the system logic can run at 3.3 V or 5 V.

Other important considerations are:

- The “island” must be large enough to include the processor, the required power supply decoupling capacitance, and the necessary connection to the 3.3 V source.
- To minimize signal degradation, the gap between the 3.3 V island and the 5 V plane should be kept to a minimum: typical gap size is about 0.02 inches.
- Minimize the number of traces routed across the power plane gap, since each crossing introduces signal degradation due to the impedance discontinuity that occurs at the gap. For traces that must cross the gap, route them on the side of the board next to the ground plane to reduce or eliminate the signal degradation caused by crossing the gap. If this is not possible, then route the trace to cross the gap at a right angle (90 degrees).
- Use liberal decoupling capacitance between the 5 V plane and the 3.3 V island. Decoupling the island reduces impedance discontinuity.

Figure 9-17. Creating a Power "Island"



9.2 Choosing a Power Source

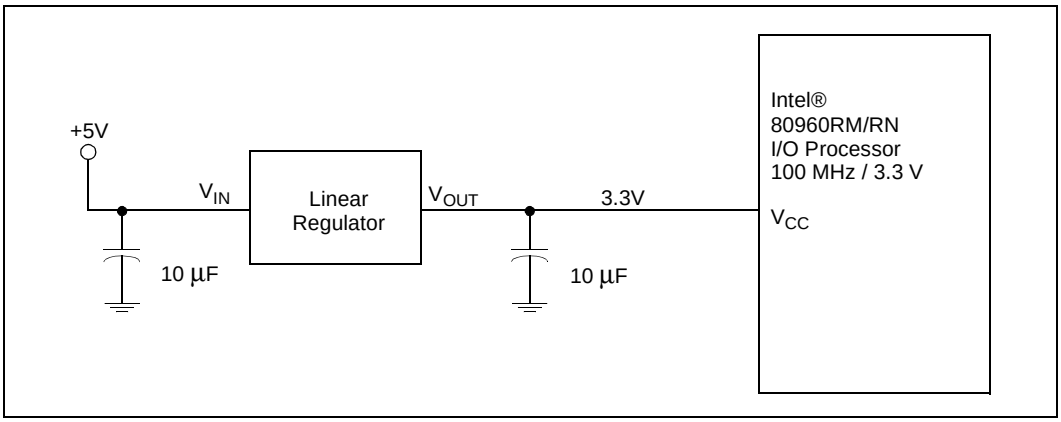
The primary concern that must be addressed when selecting a power source is the maximum load current requirement. The processor power supply must maintain correct voltage regulation at a current of 5.0 A for the RM/RN I/O processor.

Two options for supplying 3.3 V to the processor are:

- Add a 3.3 V tap to the primary system power supply
- Use on-board secondary regulation to derive 3.3 V from the 5 V system power supply

For on-board secondary regulation, a linear voltage regulator performs adequately for most designs as shown in Figure 9-18.

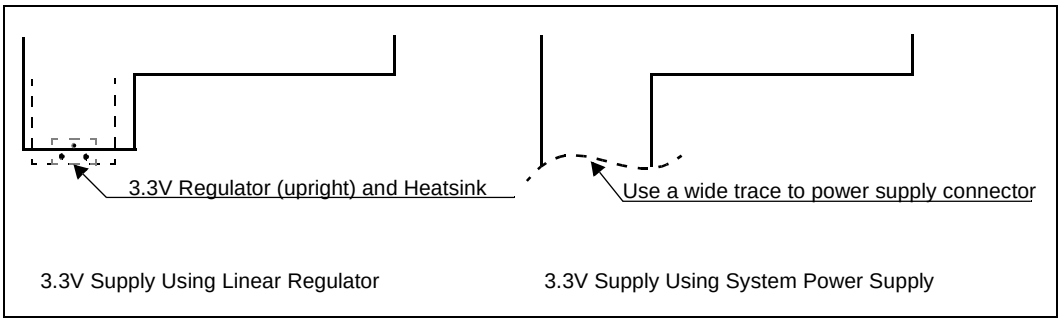
Figure 9-18. Power Supply Circuit



If low heat or power dissipation is a design goal, then the higher complexity and cost of a switching regulator may be warranted. Switching regulators offer better efficiency, thereby lowering regulator power consumption and heat.

Figure 9-19 shows recommended layouts for power supply or linear regulator connection to the 3.3 V “island.”

Figure 9-19. Recommended Power Supply Connection Layout



9.3 PCI Adapter Card Power Source

Currently, PCI Adapter card vendors cannot rely on the PCI connector to provide 3.3V. Hence, any adapter card designed with the RM/RN I/O processor must design an on-board 3.3V regulator for the processor power supply.

9.4 V_{CC5REF} Pin Requirement (V_{DIFF})

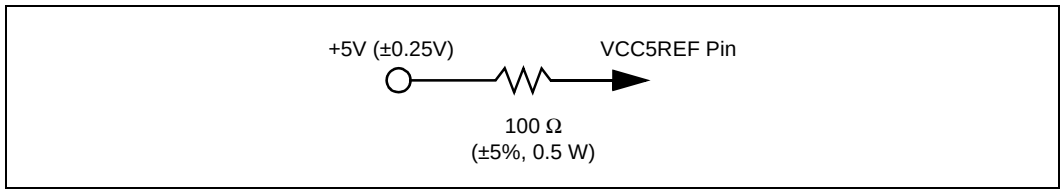
In mixed voltage systems that drive RM/RN I/O processor inputs in excess of 3.3V, the $\mathbf{V_{CC5REF}}$ pin must be connected to the system's 5V supply. To limit current flow into the $\mathbf{V_{CC5REF}}$ pin, there is a limit to the voltage differential between the $\mathbf{V_{CC5REF}}$ pin and the other V_{CC} pins. The voltage differential between the $\mathbf{V_{CC5REF}}$ pin and its 3.3V V_{CC} pins should never exceed 2.25V. Meeting this requirement ensures proper operation and guarantees component reliability. This limit applies to power-up, power-down, and steady-state operation. Table 9-15 outlines this requirement.

Table 9-15. V_{DIFF} Specification for Dual-Power Supply Requirements (3.3 V, 5 V)

Sym	Parameter	Min	Max	Unit	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	$\mathbf{V_{CC5REF}}$ input should not exceed V_{CC} by more than 2.25V during power-up and power-down, or during steady-state operation.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 9-20, a 100 ohm 0.5W series resistor may be used to limit the current into the $\mathbf{V_{CC5REF}}$ pin. This resistor ensures that current drawn by the $\mathbf{V_{CC5REF}}$ pin does not exceed the maximum rating for this pin.

Figure 9-20. V_{CC5REF} Current-Limiting Resistor



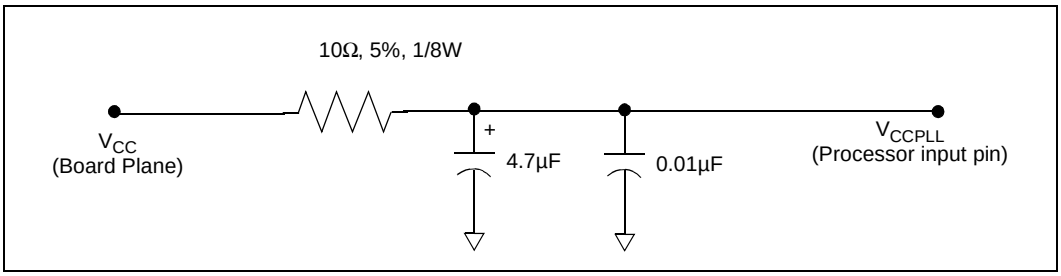
This resistor is not necessary in systems that can guarantee the V_{DIFF} specification. Also, in 3.3V-only systems and systems that drive pins from 3.3V logic, connect the $\mathbf{V_{CC5REF}}$ pin directly to the 3.3V V_{CC} plane.

9.5 V_{CCPLL} Pins Requirement

To reduce clock skew on the processor, the V_{CCPLL} pin for the Phase Lock Loop (PLL) circuit is isolated on the pinout. The low-pass filter, shown in Figure 9-21, reduces noise induced clock jitter and its effects on timing relationships in system designs. The trace lengths between the 4.7 µF capacitor, the 0.01 µF capacitor, and V_{CCPLL} must be as short as possible.

There are three V_{CCPLL} pins on the RM/RN I/O processor: $\mathbf{V_{CCPLL1}}$, $\mathbf{V_{CCPLL2}}$ and $\mathbf{V_{CCPLL3}}$. Each pin requires a low-pass filter. Providing just one low-pass filter and tying it to all three V_{CCPLL} inputs is not recommended.

Figure 9-21. V_{CCPLL} Low-Pass Filter



9.6 Pullups and Pulldown Resistors

RM/RN I/O processor inputs which require a pull-up should have the pullup resistor tied to the appropriate supply voltage. In a 3.3V only design, the resistor should be tied to the 3.3V supply. In a design where the RM/RN I/O processor interface to components operating at 5V, the resistors can be tied to either the 3.3V power island or the 5V supply.

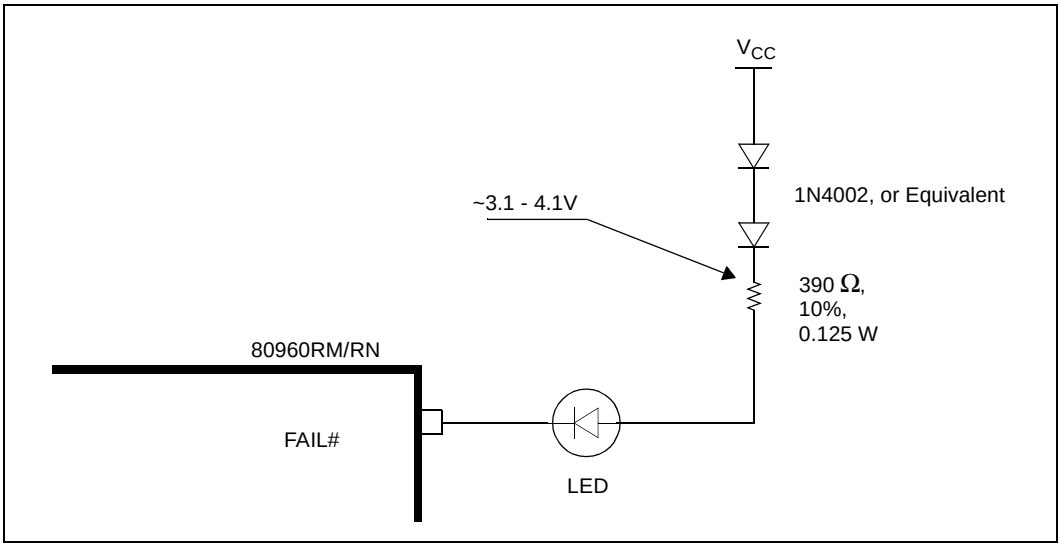
9.7 FAIL#

Many applications use a light emitting diode (LED) to indicate when the FAIL# pin is low (active). However, when an RM/RN I/O processor is in the design, and the FAIL# pin is high (inactive) at 3.3 V, the LED can still be forward biased enough to glow. To ensure the LED extinguishes when FAIL# goes high, Intel recommends the circuit shown in Figure 9-22.

The two diodes dissipate about 1.4 V, so the LED voltage drops too low to glow when the FAIL# pin goes high. Use a low current LED that can operate at 3-5 mA. This design works whether V_{CC} is 5 V or 3.3 V nominal.

An alternative is to eliminate the diodes and power the LED from the 3.3 V V_{CC} supply of the RM/RN I/O processor.

Figure 9-22. Recommended FAIL# Circuit



10.0 Processor Power Supply Decoupling

Processor power supply decoupling is critical for reliable operation. With the 3.3 V ready system, two areas of concern are described in Section 10.1 and Section 10.2:

- High frequency decoupling, necessitated by the processor's high speed operation
- Low frequency decoupling, necessitated by the processor's power saving features

10.1 High Frequency Decoupling

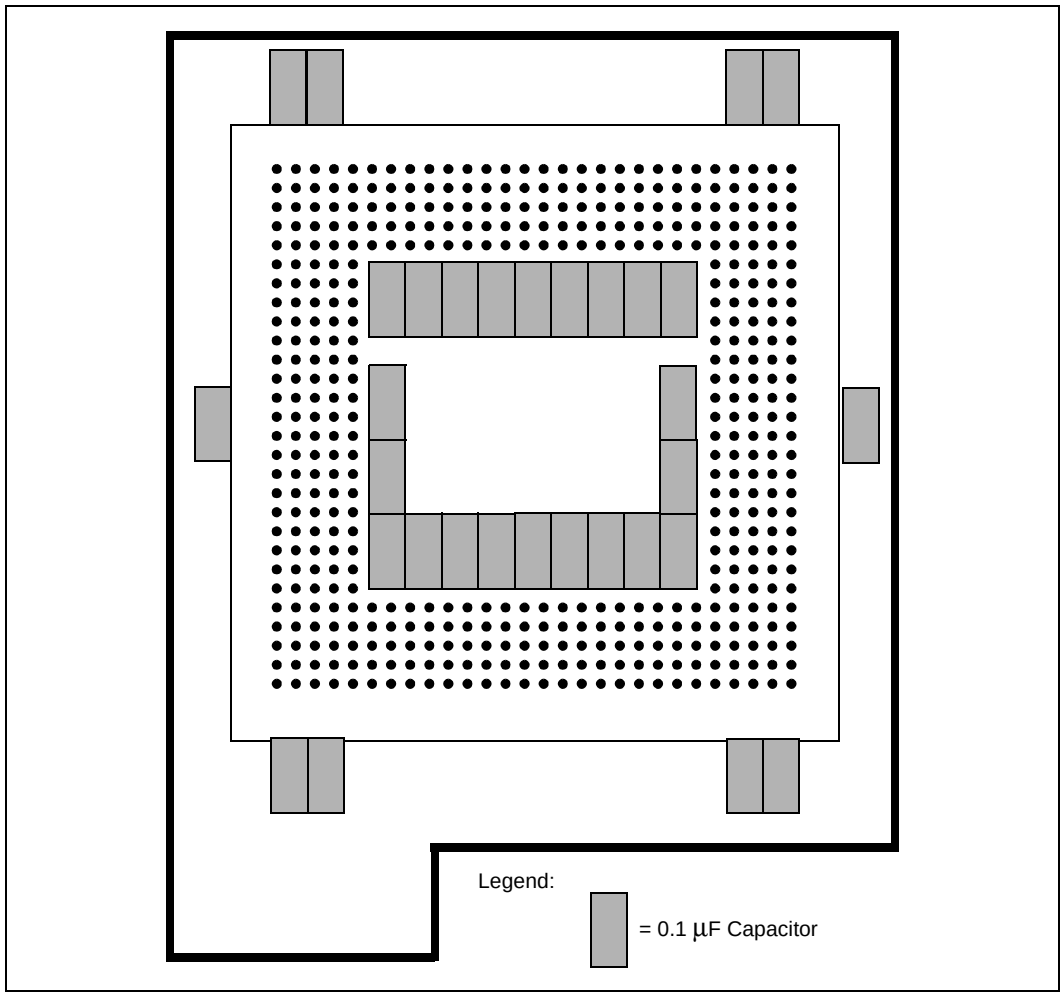
Decoupling capacitors reduce voltage spikes by supplying extra current needed during switching. Decoupling is especially critical on the RM/RN I/O processor because of its 100 MHz internal operation.

A reliable design will include a minimum of thirty-two 0.1 µF surface mount ceramic chip capacitors between power and ground, evenly distributed, around the processor. The capacitors must be placed as close to the processor as possible, attached directly to the power and ground planes, otherwise circuit board inductance will significantly reduce their effectiveness.

Figure 10-23 is an example of how to place high frequency capacitors on the back (solder) side of the motherboard or add-in card. The BGA package in Figure 10-23 is shown for reference only; normally it is not be visible from the back side. The outline around the BGA package is the 3.3 V power island which is only needed on mixed voltage designs. When the design does not permit components on the back side of the PCB, place the decoupling capacitors around the perimeter on the component side of the PCB.

Inadequate high frequency decoupling results in unreliable or inconsistent program behavior. These failures are often intermittent, and are difficult to diagnose and debug.

Figure 10-23. High-Frequency Capacitor Values and Layout



10.2 Bulk Decoupling Capacitance

Bulk, or low-frequency decoupling is needed on the RM/RN I/O processor. If the processor is on a separate power plane “island”, it is necessary to place capacitance on the processor “island.” For bulk decoupling, place two 47 mF surface mount capacitors in parallel, directly between the power and ground planes. Place the capacitors close to the processor, within the power “island”. If other 3.3V components are on the PCB, then the two 47 mF capacitors may be omitted since the other components would have bulk decoupling capacitors. However, the value and number of capacitors required is dependent on the individual board design and layout characteristics.

11.0 Intel® 80960RM/RN Processor Based Reference Design

See Appendix A through Appendix D for schematics and bill of material. OrCAD libraries for the RM/RN I/O processor are available and can be supplied upon request.

12.0 Debug Connector Recommendations

This section describes debug hardware and connectors developed for the RM/RN I/O processor. This includes sockets, headers, logic analyzer interposer, Mictor* signal cross reference lists and JTAG emulator debug connector/pin assignments.

12.1 PBGA Sockets and Headers

Figure 12-24 and Figure 12-25 illustrate surface mount sockets and headers available for the RM/RN I/O processor. See Table 14-22 for socket and header vendor information.

Figure 12-24. 540L PBGA Header

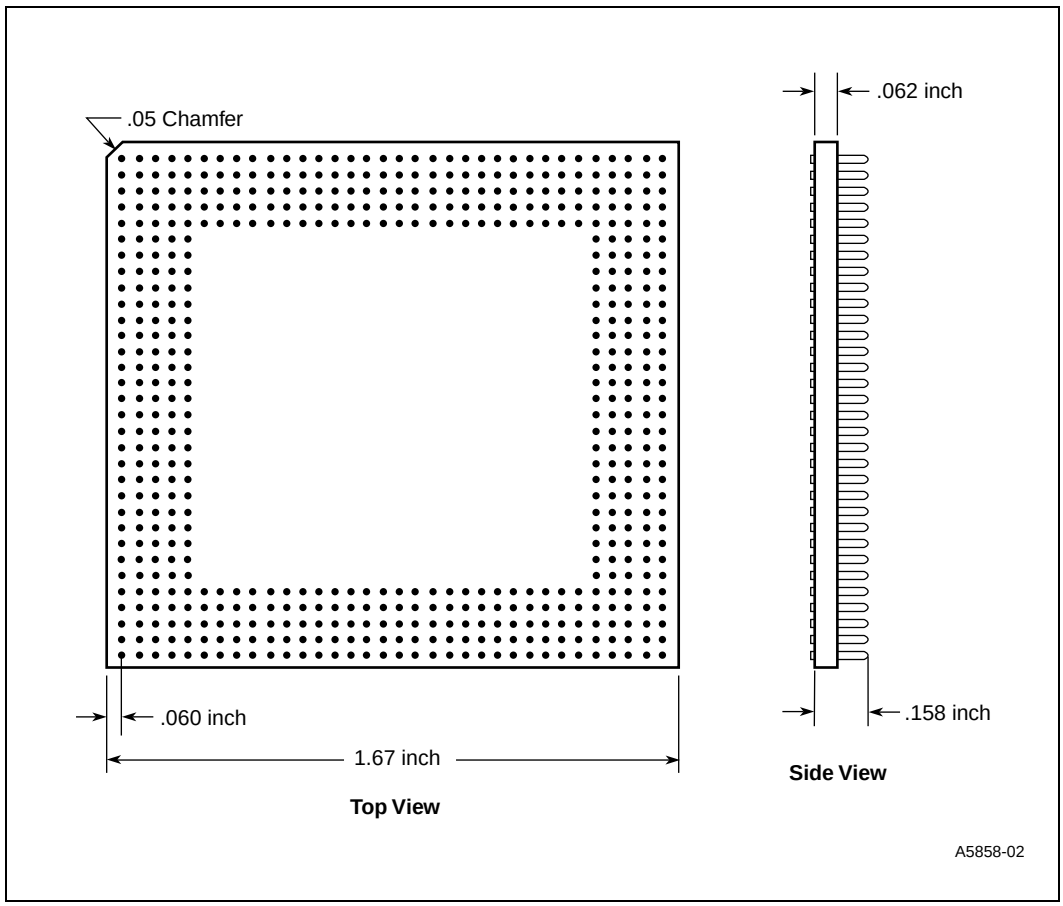
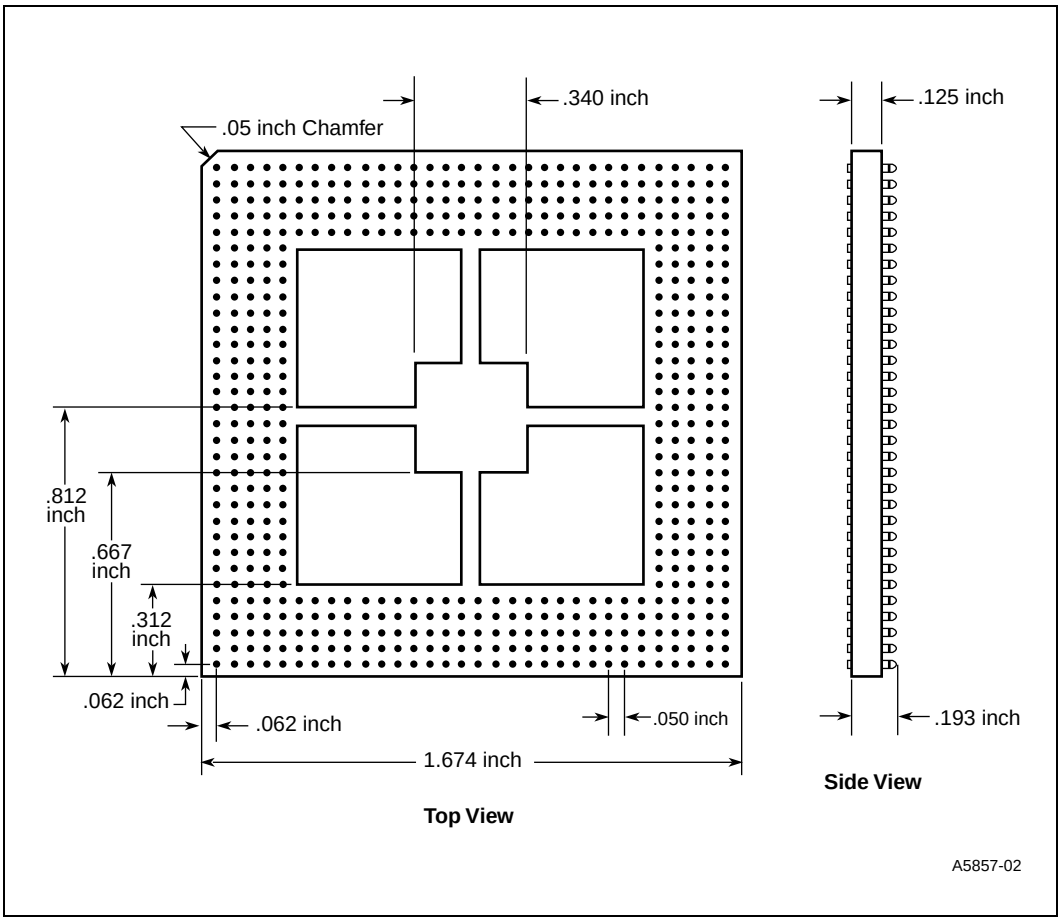


Figure 12-25. 540L PBGA Socket



12.2 Logic Analyzer Connectivity

The Mictor connector is the common connector used by the RM/RN I/O processor for logic analysis connectivity. The Cyclone evaluation board developed for the 80960RM/RN integrates five Mictor connectors to route the appropriate signals for logic analysis and probing. See Table 12-16.

A removable interposer is also available for designs that may not have the available board space for Mictor connectors. See Figure 12-26, Figure 12-27 and Figure 12-28. Refer to Table 14-25 for logic analyzer interposer vendor information.

Table 12-16 is the signal cross-reference list for the RM/RN I/O processor and associated Mictor connectors for the Cyclone board and the flex tape interposer. Pins1,2,37 and 38 are not used.

Table 12-16. Logic Analyzer Header Definitions (Mictor)

PIN	Cyclone J9	Cyclone J11	Cyclone J12	Cyclone J10	Cyclone J8
	Interposer J2	Interposer J3	Interposer J4	Interposer J5	Interposer J1
3	N/C	SDRAMCLK	N/C	N/C	N/C
4	DQ15	SDQM7	DQ31	N/C	RAD15
5	DQ14	SDQM6	DQ30	N/C	RAD14
6	DQ13	SDQM5	DQ29	N/C	RAD13
7	DQ12	SDQM4	DQ28	N/C	RAD12
8	DQ11	SDQM3	DQ27	N/C	RAD11
9	DQ10	SDQM2	DQ26	N/C	RAD10
10	DQ9	SDQM1	DQ25	N/C	RAD9
11	DQ8	SDQM0	DQ24	N/C	RAD8
12	DQ7	SCB7	DQ23	N/C	RAD7
13	DQ6	SCB6	DQ22	N/C	RAD6
14	DQ5	SCB5	DQ21	N/C	RAD5
15	DQ4	SCB4	DQ20	N/C	RAD4
16	DQ3	SCB3	DQ19	SCE0#	RAD3
17	DQ2	SCB2	DQ18	SCE1#	RAD2
18	DQ1	SCB1	DQ17	SBA1	RAD1
19	DQ0	SCB0	DQ16	SBA0	RAD0
20	DQ32	SA0	DQ48	SREQ0#	RAD16
21	DQ33	SA1	DQ49	SREQ1#	N/C
22	DQ34	SA2	DQ50	SREQ2#	N/C
23	DQ35	SA3	DQ51	SREQ3#	RALE
24	DQ36	SA4	DQ52	SREQ4#	RCE0#
25	DQ37	SA5	DQ53	SREQ5#	RCE1#
26	DQ38	SA6	DQ54	SGNT0#	ROE#
27	DQ39	SA7	DQ55	SGNT1#	RWE#
28	DQ40	SA8	DQ56	SGNT2#	N/C
29	DQ41	SA9	DQ57	SGNT3#	N/C
30	DQ42	SA10	DQ58	SGNT4#	N/C
31	DQ43	SA11	DQ59	SGNT5#	N/C
32	DQ44	N/C	DQ60	N/C	N/C
33	DQ45	SWE#	DQ61	N/C	N/C
34	DQ46	SCAS#	DQ62	N/C	N/C
35	DQ47	SRAS#	DQ63	N/C	N/C
36	N/C	N/C	N/C	P_PCICLK	RALE

Figure 12-26. Packard-Hughes Direct Mount (Flex Tape) Interposer - Top View

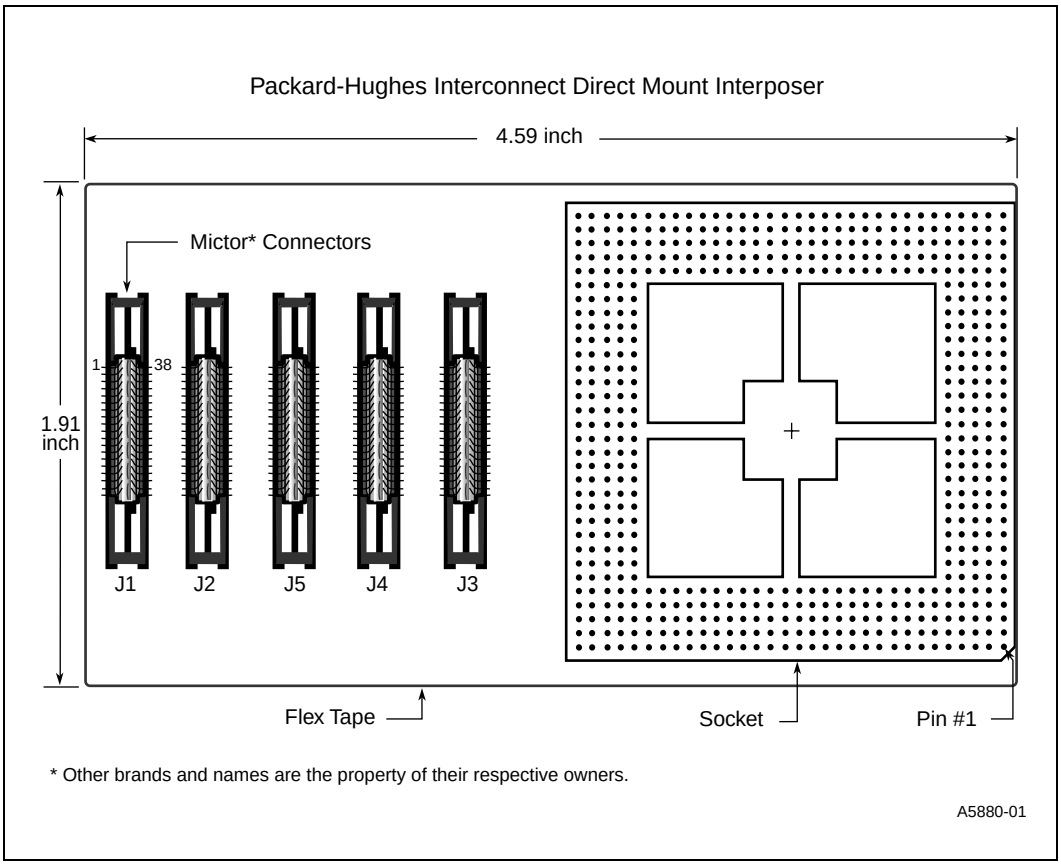


Figure 12-27. Packard-Hughes Direct Mount (Flex Tape) Interposer - Side View

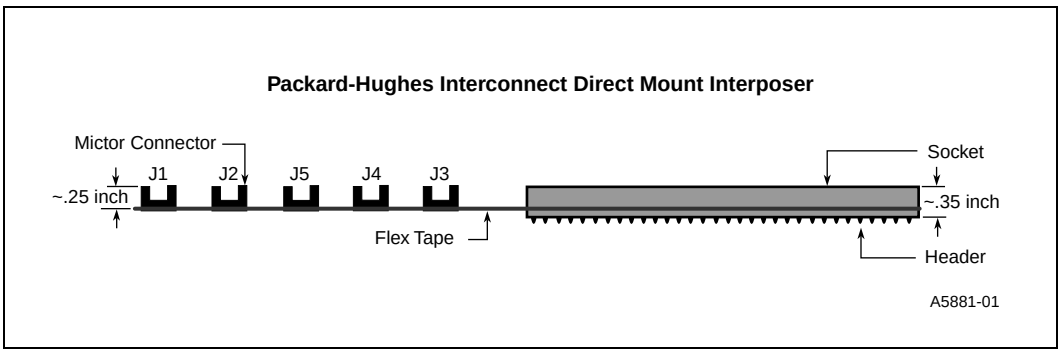


Figure 12-28. Flex Tape Interposer Application (Add-In Card)

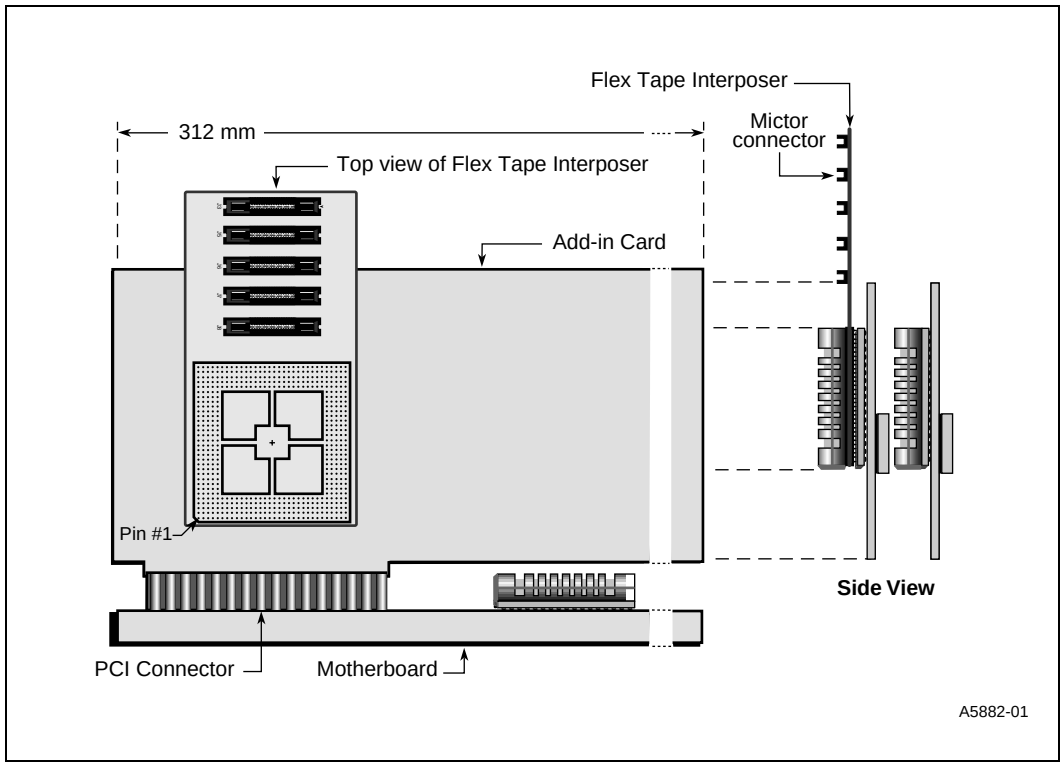


Figure 12-29. Flex Tape Interposer (Top View)

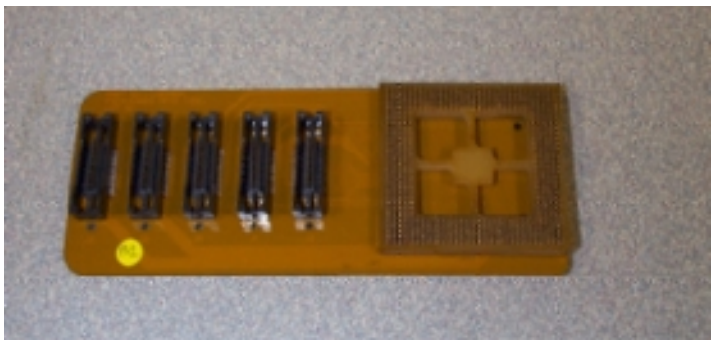


Figure 12-30. Flex Tape Interposer (Side View)

12.3 JTAG Connector and Test Interface

12.3.1 Intel® i960® RM/RN I/O Processor JTAG Emulator

The JTAG emulator for the i960® RM/RN I/O processor is designed to provide a convenient and non-intrusive means of debugging. The JTAG emulator is connected to the processor by means of a simple 16-pin connector. The hardware provided with the JTAG emulator can also be used (with additional software) to test opens and shorts on the processor without the necessity for any additional circuitry, other than a single 16-pin connector once it has been installed onto the PCB. A JTAG emulator provides a designer the ability to download code, read data from registers, single-step the processor, insert breakpoints (both hardware and software) and perform full source level debugging without the need of an intrusive monitor program or a bulky hardware pod.

12.3.2 Intel® i960® RM/RN I/O Processor Target Debug Interface Connector

The i960 microprocessor target should have a 16-pin, two row header connector. Use 3M part number 2516-6002UG or equivalent. The header is made from a keyed plastic shroud with two rows of 8 pins and the spacing between adjacent pins and between the two rows is 0.100”. The header pin assignment is illustrated in Figure 12-31.

Figure 12-31. JTAG Emulator Connector (Top View)

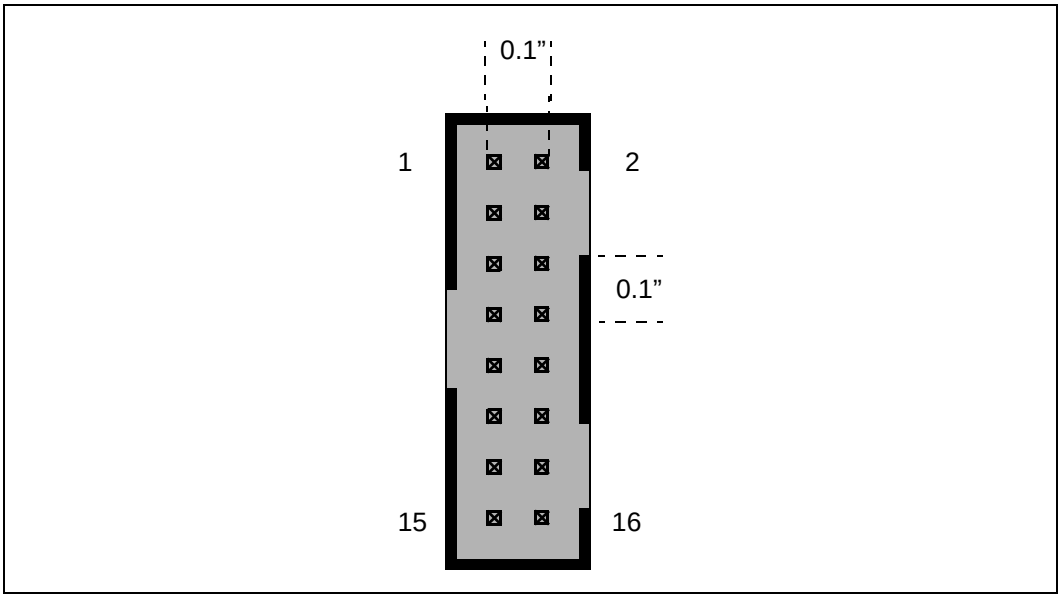


Figure 12-17 describes the interconnections required between the target debug interface connector and the pins/balls of the i960 RM/RN I/O processor family.

Table 12-17. i960® RM/RN I/O Processor Debug Connector Wiring

Header Pin	i960® RM/RN I/O Processor Ball/Direction	Signal Name	Recommended Target Resistor
1	C11	TRST#	1KΩ pull-down
2		GND	
3	A12	TDI	1KΩ pull-up
4		GND	
5	E11	TDO	
6		GND	
7	B11	TMS	1KΩ pull-up
8		GND	
9	C12	TCK	1KΩ pull-up
10		GND	
11	A21	LCDINIT#	1KΩ pull-up
12		GND	
13	A11	I_RST#	
14		GND	
15		PWRVLD	Connected to V_{CC} through 1KΩ series resistor
16		GND	

12.3.3 Connecting The Emulator To The Target

The emulation software uses the first Test Access Port (TAP) on the PC-1149.1/100F boundary-scan controller card to control the i960 RM/RN I/O processor. A cable should be connected from the boundary-scan controller to the i960 RM/RN I/O processor target debug interface connector as shown in the following tables. A cable built to one of the following specifications is supplied with the corresponding emulator.

Table 12-18. i960® RM/RN I/O Processor with PC-1149.1/100F (cable P/N AS01090025-Ax)

PC-1149.1/100F Signal Name	PC-1149.1/100F Pin	Target Signal Name	Target Debug Header Pin
TRST#	1	TRST#	1
GND	2	GND	2
TDO12	3	TDI	3
GND	4	GND	4
TDI12	5	TDO	5
GND	6	GND	6
TMS1	7	TMS	7
GND	8	GND	8
TCK12 (see note)	9	TCK	9
GND	10	GND	10
TMS3	25	LCDINIT#/ RSTIN#	11
GND	12	GND	12
SENSE#	13	I_RST/ RSTOUT#	13
GND	14	GND	14
T_OFF# (see note)	11	PWRVLD	15
GND	16	GND	16

NOTE: Connected to target through 33Ω series resistor.

Table 12-19. i960® RM/RN I/O Processor with PCMCIA-1149.1 (cable P/N AS01090025-Bx)

PCMCIA-1149.1 Signal Name	PCMCIA-1149.1 Pin	Target Signal Name	Target Debug Header Pin
TRST#	8	TRST#	1
GND	9	GND	2
TDO1	7	TDI	3
GND	5	GND	4
TDI1	6	TDO	5
GND	3	GND	6
TMS1	4	TMS	7
GND	1	GND	8
TCK1 (see note)	2	TCK	9
GND	11	GND	10
PIO_0	17	LCDINIT#/ RSTIN#	11
GND	13	GND	12
PIO_1	18	I_RST/ RSTOUT#	13
GND	25	GND	14
PIO_2 (see note)	19	PWRVLD	15
-	No Connection	GND	16

NOTE: Connected to target through 33Ω series resistor.

12.3.4 Other Tools

Other tools are available that are designed to complement the i960 family of JTAG emulators. These include a full complement of boundary-scan hardware and software for testing the 80960RM/RN for opens, shorts, and other manufacturing defects once it has been installed onto the target board. In addition, Corelis has available a preprocessor (PI-PCI32/64) for use with the HP family of logic analyzers that allows a designer to examine the full complement of signals on the PCI bus including all the boundary-scan signals. Since 80960RM/RN designs typically incorporate PCI connectivity, this tool has been proven particularly effective in troubleshooting designs utilizing the 80960RM/RN.

13.0 Design for Manufacturability

The RM/RN I/O processor is offered in a high-thermal BGA (H-PBGA) package. PBGA packaging is explained extensively in the Intel® *Packaging Databook* (Order Number 240800).

14.0 Thermal Solutions

In general, three factors affect the thermal performance of the BGA: package and board materials, package geometry and use environment. The H-PBGA package utilizes a heat spreader or slug across the top of the package to dissipate heat efficiently.

Environmental conditions play a critical role in the thermal performance of PBGAs. Ambient conditions, junction and case temperatures, the device's placement and orientation on a board, in conjunction with the volume and temperature of air flowing past the unit present a broad range of possible thermal solutions. The profiles of the H-PBGA package are characterized in Table 14-20.

Table 14-20. H-PBGA Package Characteristics

Description	Criteria
Die Junction temperature	110 ° C
Case Temperature (maximum)	90 ° C[a]
Ambient temperature	up to 55 ° C
Airflow (on motherboard) from system fan	up to 50 LFM (worst case)
Airflow (on add-in card)	0 LFM (worst case)
Passive heatsink dimensions Acceptable flange adds 5 mm per side on hole direction of fan	Clip = 45 mm x 45 mm < 11 mm (thickness) Flange type =55 mm x 45 mm <11 mm (thickness) with pins.
Maximum heatsink thickness	<11 mm
Clip Hole Pattern	4 holes (3.175 mm diameter), 48.4632 x 34.798 mm rectangular (see Figure 14-33 and Figure 14-34)
Heatsink Flatness	From center of heatsink to 1/2 inch in x and y directions, 2 mils maximum

a. Case temperature is dependent on the ambient temperature and airflow surrounding the processor. Refer to the application note "Thermal Data for the 540-Lead PBGA Package" for more information.

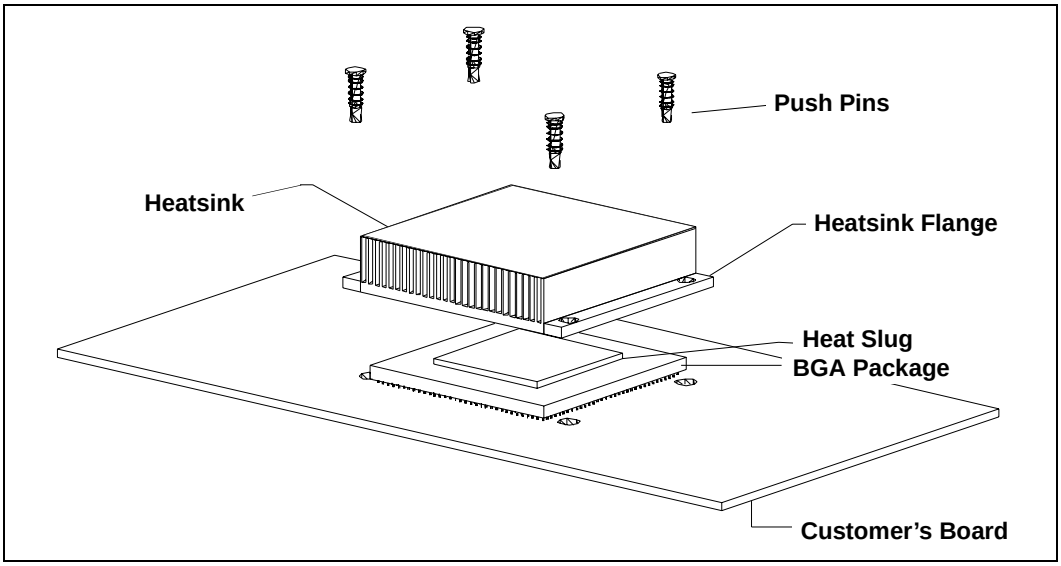
14.1 Thermal Recommendations

Refer to the thermal sections of the *Intel® 80960 RM I/O Processor Datasheet* (273156), the *Intel® 80960 RN I/O Processor Datasheet* (273157), and the *Intel® 80960 RS I/O Processor Datasheet* (273328) and to the thermal section of the *Thermal Data for the 540-Lead PBGA Package Application Note* (273390).

14.2 3-Dimensional View: Processor with Heat Sink Attached

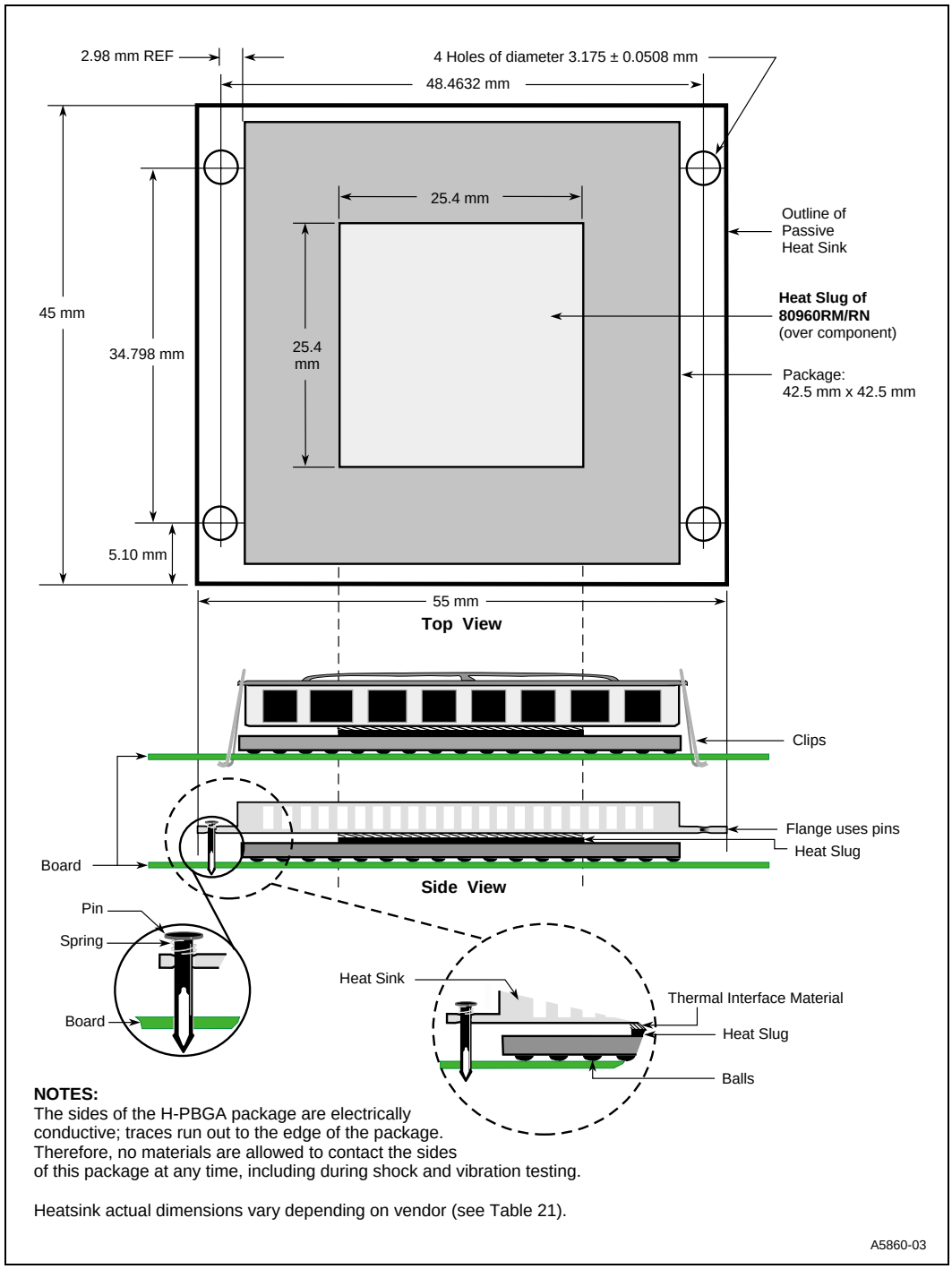
To assist the board designer in component placement, hole placement and dimensions, Figure 14-33 and Figure 14-34 detail specifics. Figure 14-33 details dimensions for board designs requiring a Passive Heat Sink.

Figure 14-32. Conceptual 3-D View of Processor with a Heat Sink



14.3 PCB Heatsink Hole Dimensions

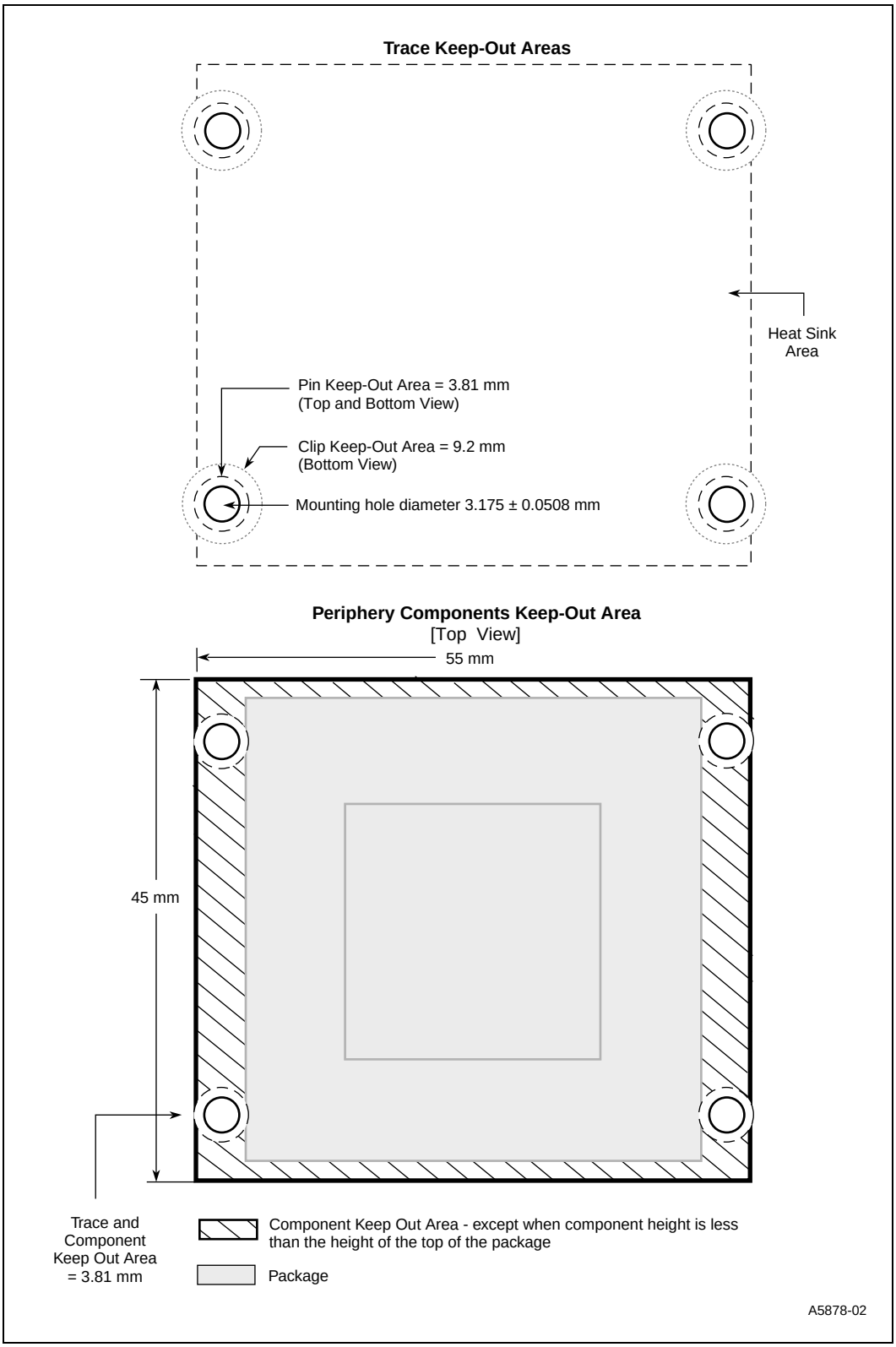
Figure 14-33. Hole Dimensions for Passive Heatsink



NOTES:
The sides of the H-PBGA package are electrically conductive; traces run out to the edge of the package. Therefore, no materials are allowed to contact the sides of this package at any time, including during shock and vibration testing.

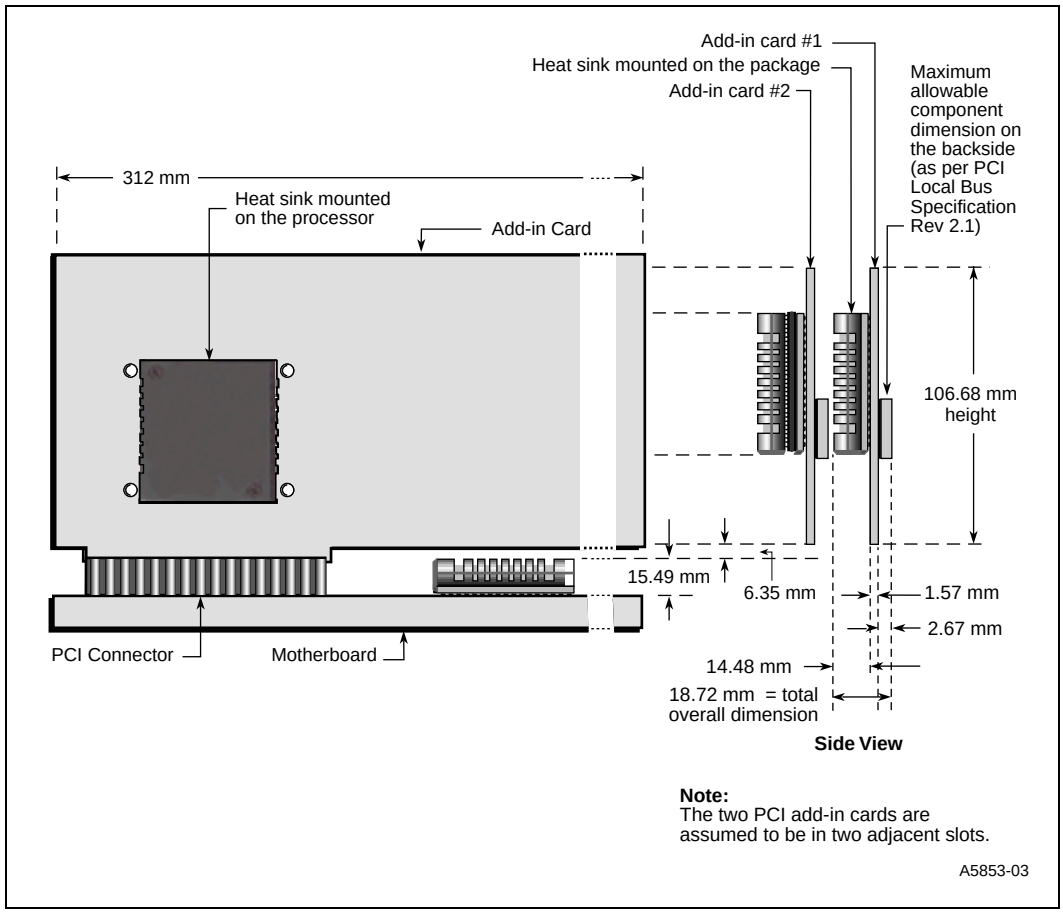
Heatsink actual dimensions vary depending on vendor (see Table 21).

Figure 14-34. Board Level Keep Out Areas



14.4 Clearances of PCI Board and Components

Figure 14-35. Clearances of PCI Board and Components



14.5 Heat Sink Information

Table 14-21 provides a list of suggested sources for heat sinks. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Table 14-21. Heat Sink Vendors and Contacts

Company	Factory Rep	Phone #	Fax #	Heatsink Part #
				Passive
AAVID THERMALLOY, LLC 2021 W. Valley View Lane Dallas Texas 75234-8993 Email:sales@thermalloyusa.com Outside of USA, refer to web page for contact information: http://www.thermalloy.com	Attn: Sales	(972) 243-4321	(972) 241-4656	21933B w/o thermal grease (uses pins) 21935B with Easy Ply (thermal grease (uses pins)

14.5.1 Socket Information

Table 14-22 and Table 14-23 provide vendor details for socket-headers and burn-in sockets for the RM/RN I/O processor. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

14.5.2 Socket-Header Vendor

Table 14-22. Socket-Header Vendor

Company	Factory Represen-tative	Phone/Fax #	Part #	
			BGA 540 Pin Header	BGA 540 Pin Socket Carrier
Adapter Technologies, Inc. 214-218 South 4th St. Perkasie, PA 18944	John Miller	215-258-5750/ 215-258-5760	BGAH-540-0-01-320 1-0277-1	BGA-540-0-02-3201 -0275P-130

14.5.3 Burn-in Socket Vendor

Table 14-23. Burn-in Socket Vendor

Company	Factory Representative	Phone #	Burn-in Socket Part #
Texas Instruments 111 Forbes Blvd. Mansfield, MA 02048	W. Ray Johnson	508-236-5375	ULGA540-005

14.5.4 Shipping Tray Vendor

Table 14-24. Shipping Tray Vendor

Company	Factory Rep	Phone #	Shipping Tray Part #
3M	Ron Goth	602-465-5381	7-0000-21001-184-167

14.5.5 Logic Analyzer Interposer Vendor

Table 14-25. Logic Analyzer Interposer Vendor

Company	Factory Rep	Phone/Fax #	Part #
Packard-Hughes Interconnect 17150 Von Karman Ave Irvine, CA 92614-0968	Sue Wood	714-660-5766 714-660-5825	1126898

14.5.6 JTAG Emulator Vendor

Table 14-26. JTAG Emulator Vendor

Company	Factory Rep	Phone/Fax #	Part #
Corelis	Mike Winters	562-926-6727 562-484-6196	TBD

15.0 References

15.1 Related Documents

Intel documentation is available from your local Intel Sales Representative or Intel Literature Sales.

To obtain Intel literature:
call 1-800-548-4725 or
visit Intel's website at http://www.intel.com

Table 15-27. Related Documentation

Document Title	Intel Order #
Intel Packaging Databook	240800
PCI Local Bus Specification Revision 2.2	PCI Special Interest Group 1-800-433-5177
PC SDRAM Unbuffered DIMM Specification v1.0	http://developer.intel.com/ technology/memory/unb_001.pdf
PCI-to-PCI Bridge Architecture Specification Revision 1.1	PCI Special Interest Group 1-800-433-5177

15.2 Electronic Information

Table 15-28. Electronic Information

Intel's World-Wide Web (WWW) Location:	http://www.intel.com
Customer Support (US and Canada):	800-628-8686

Intel® i960® RM I/O Processor Schematics A

Schematics in this document supersede schematics in Document #AZ1-00886.

Figure 15-36. Decoupling and 3.3 V Power Schematic

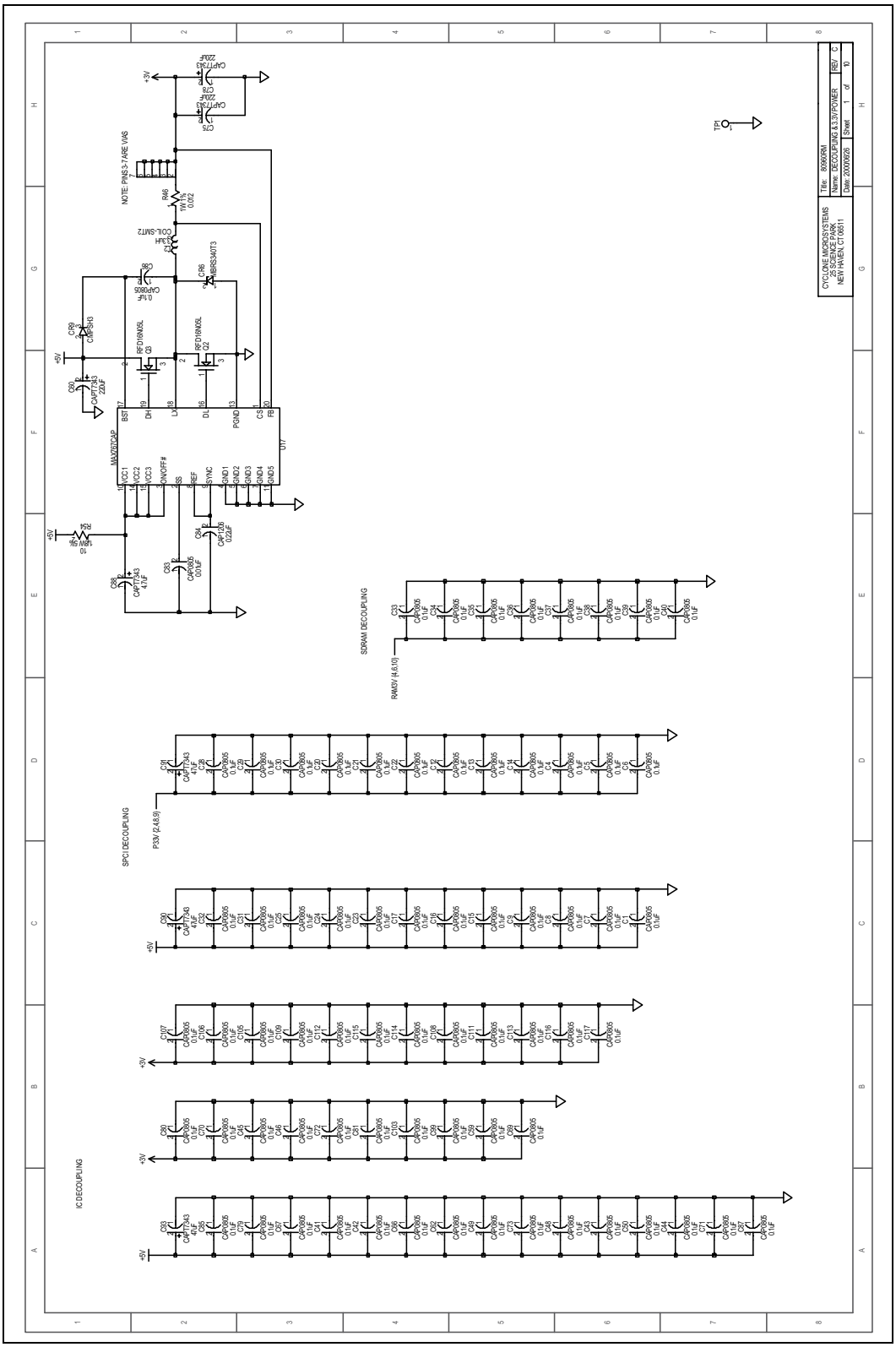


Figure 15-37. Primary PCI Interface Schematic

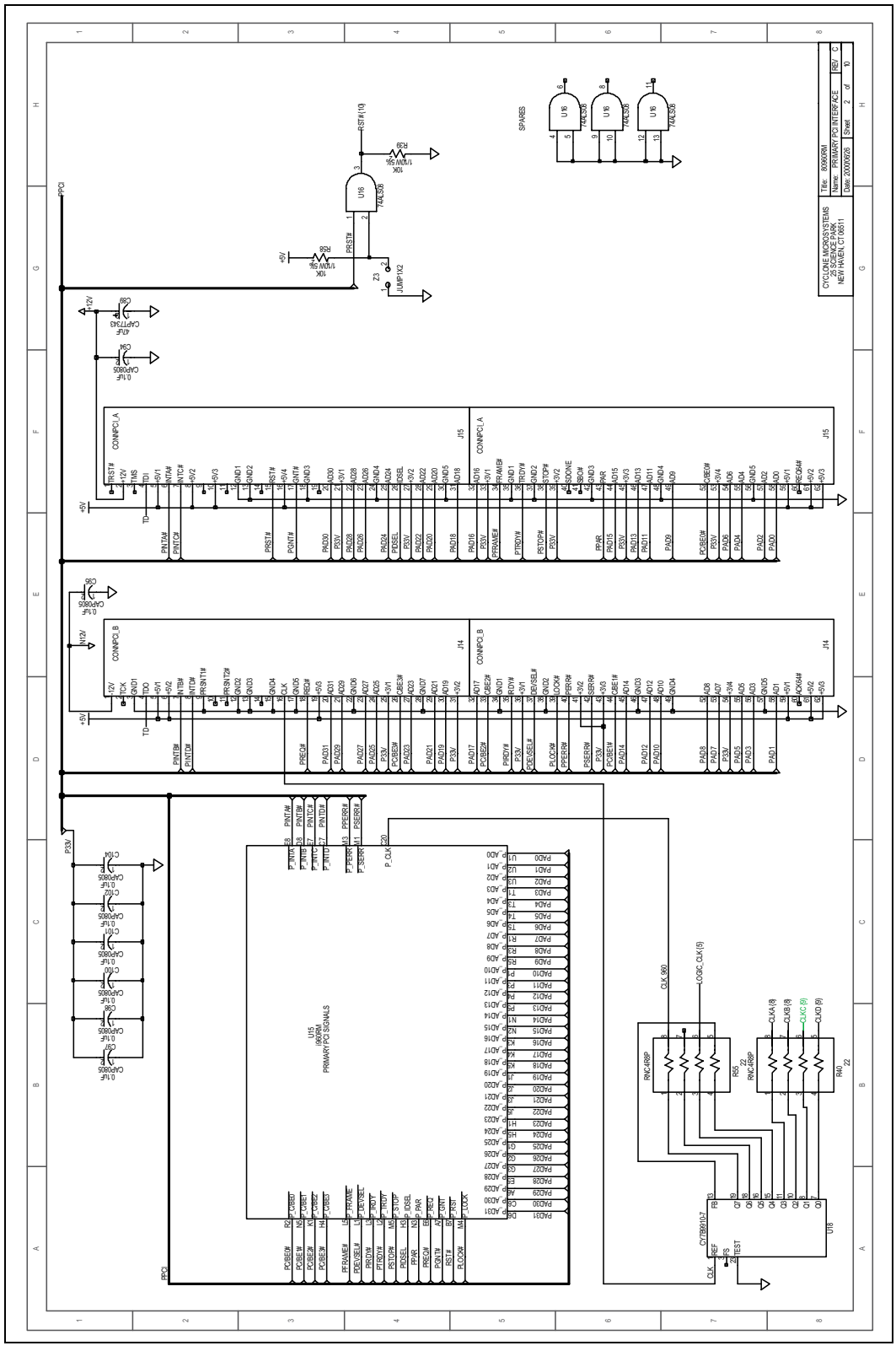


Figure 15-38. Memory Controller Schematic

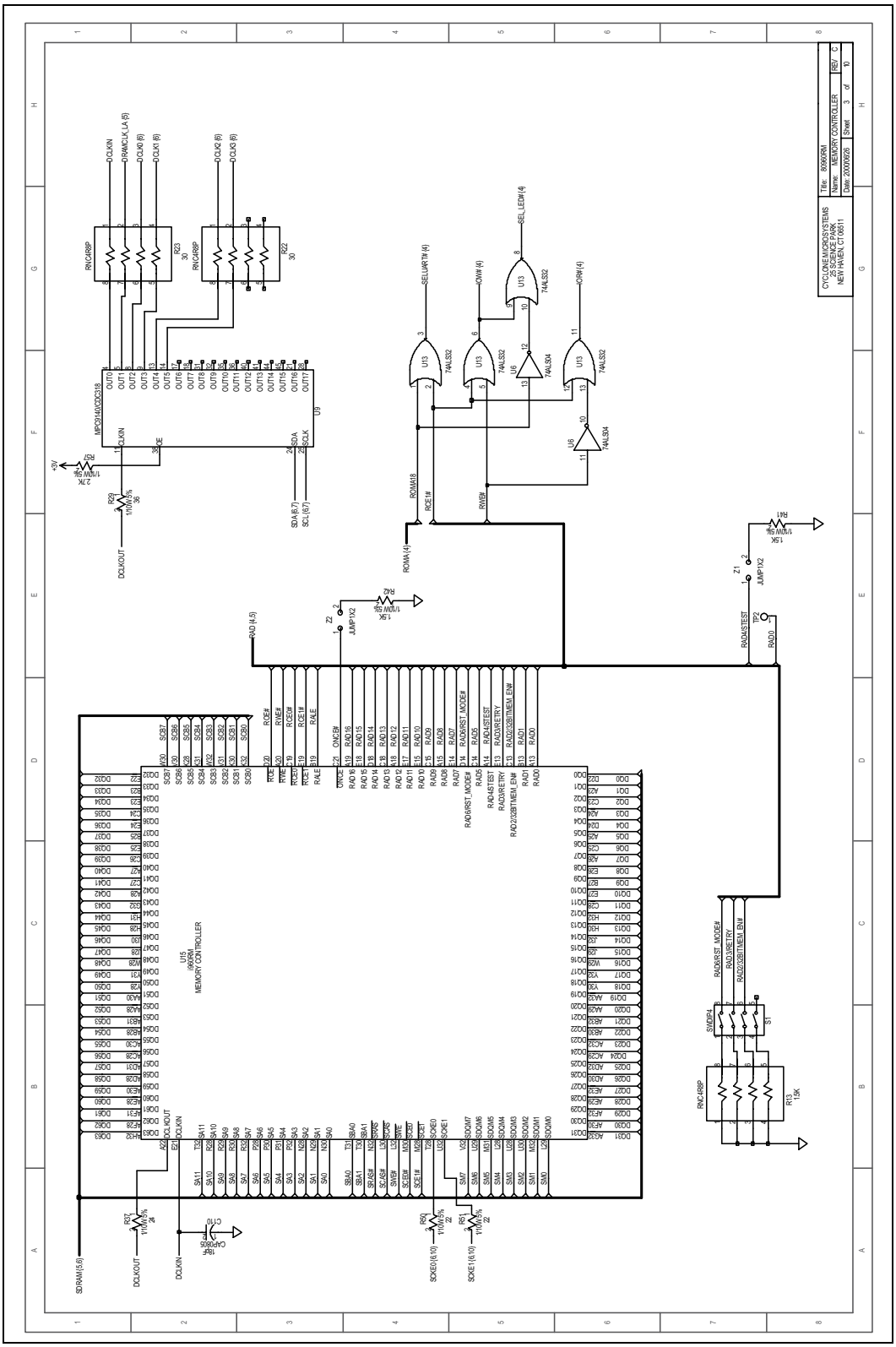


Figure 15-39. Flash ROM, UART and LEDs Schematic

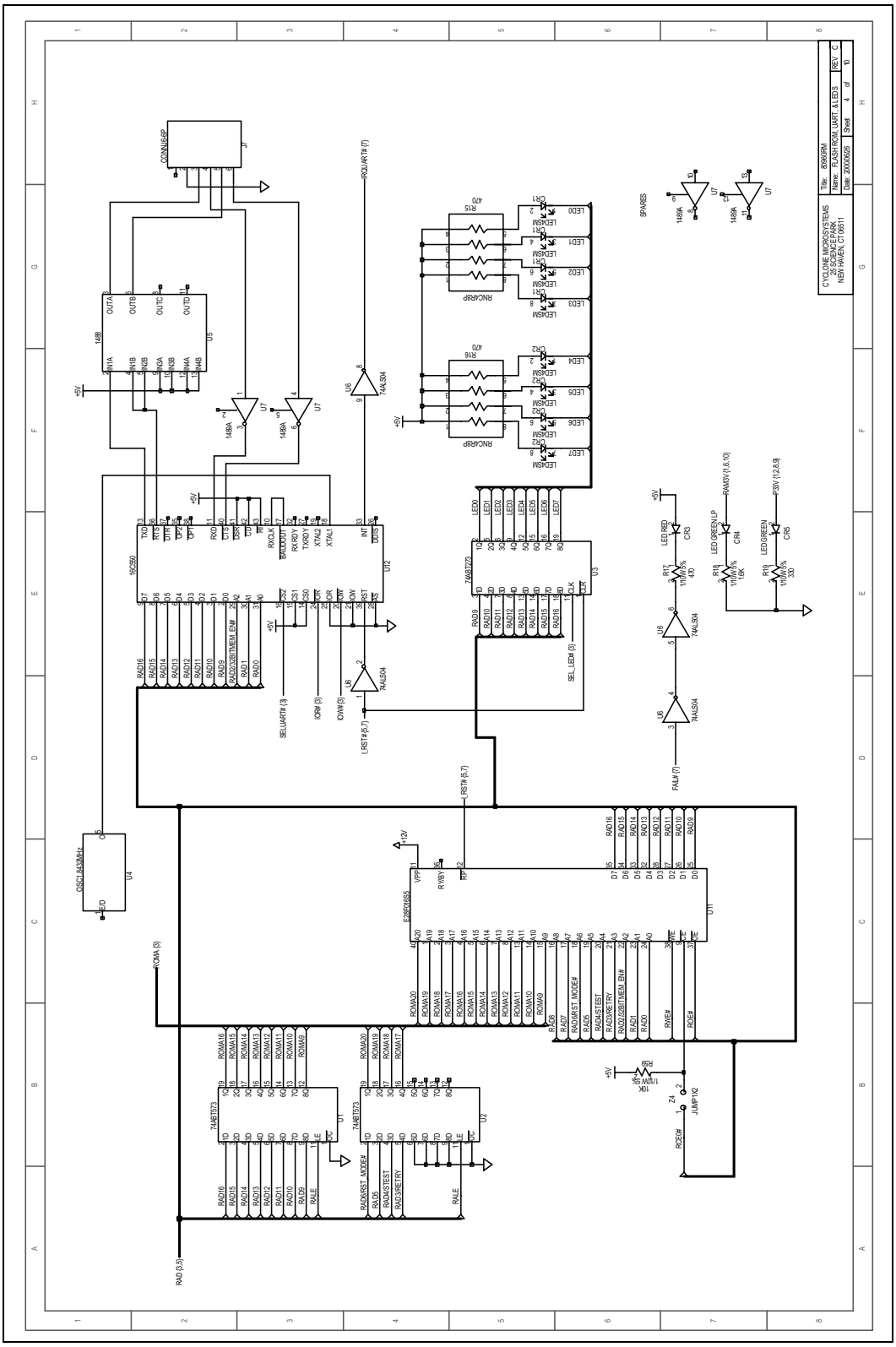


Figure 15-40. Logic Analyzer I/F Schematic

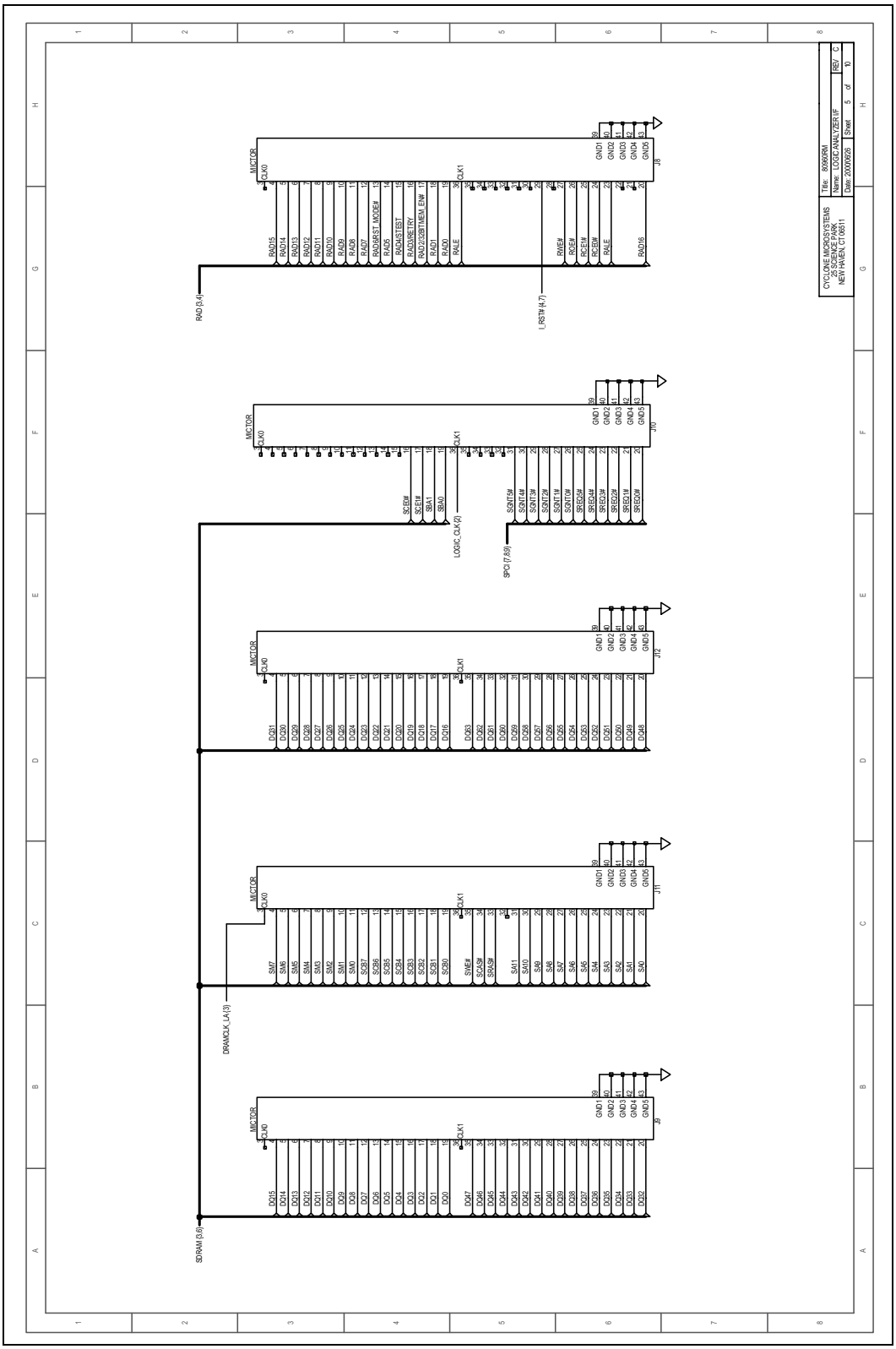


Figure 15-41. SDRAM 168-Pin DIMM Schematic

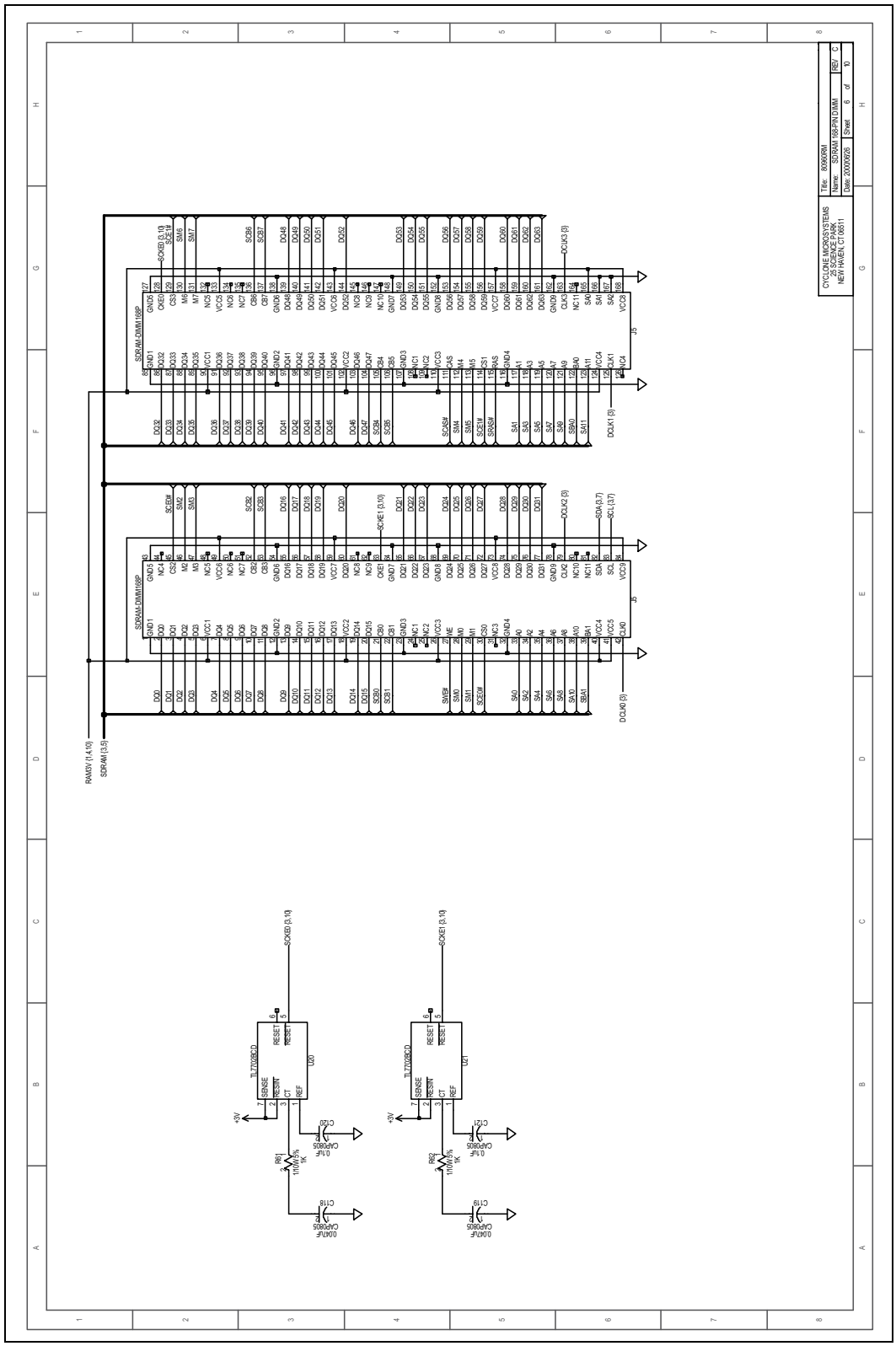


Figure 15-42. Secondary PCI/80960 Core Schematic

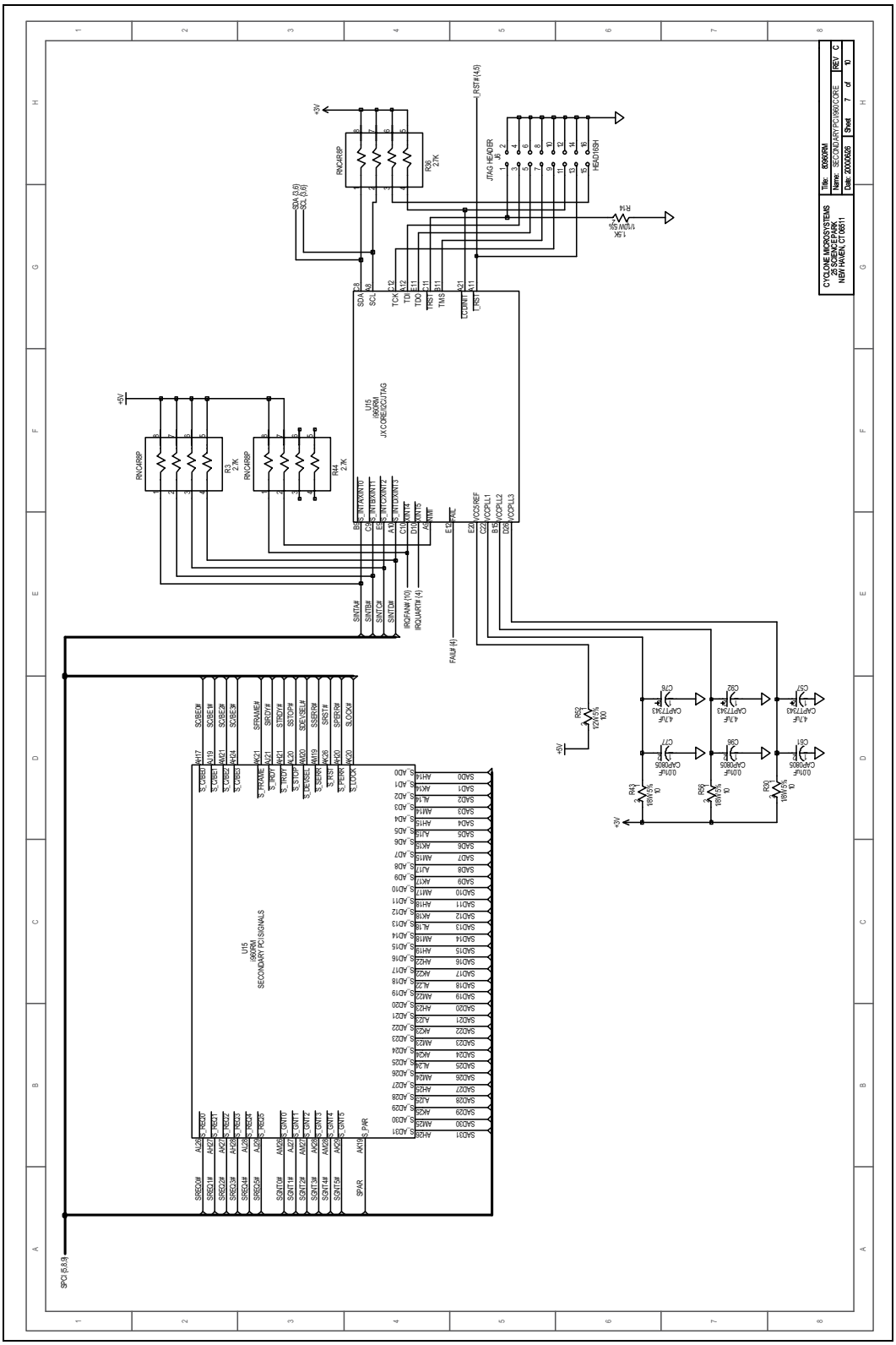


Figure 15-43. Secondary PCI Bus 1/2 Schematic

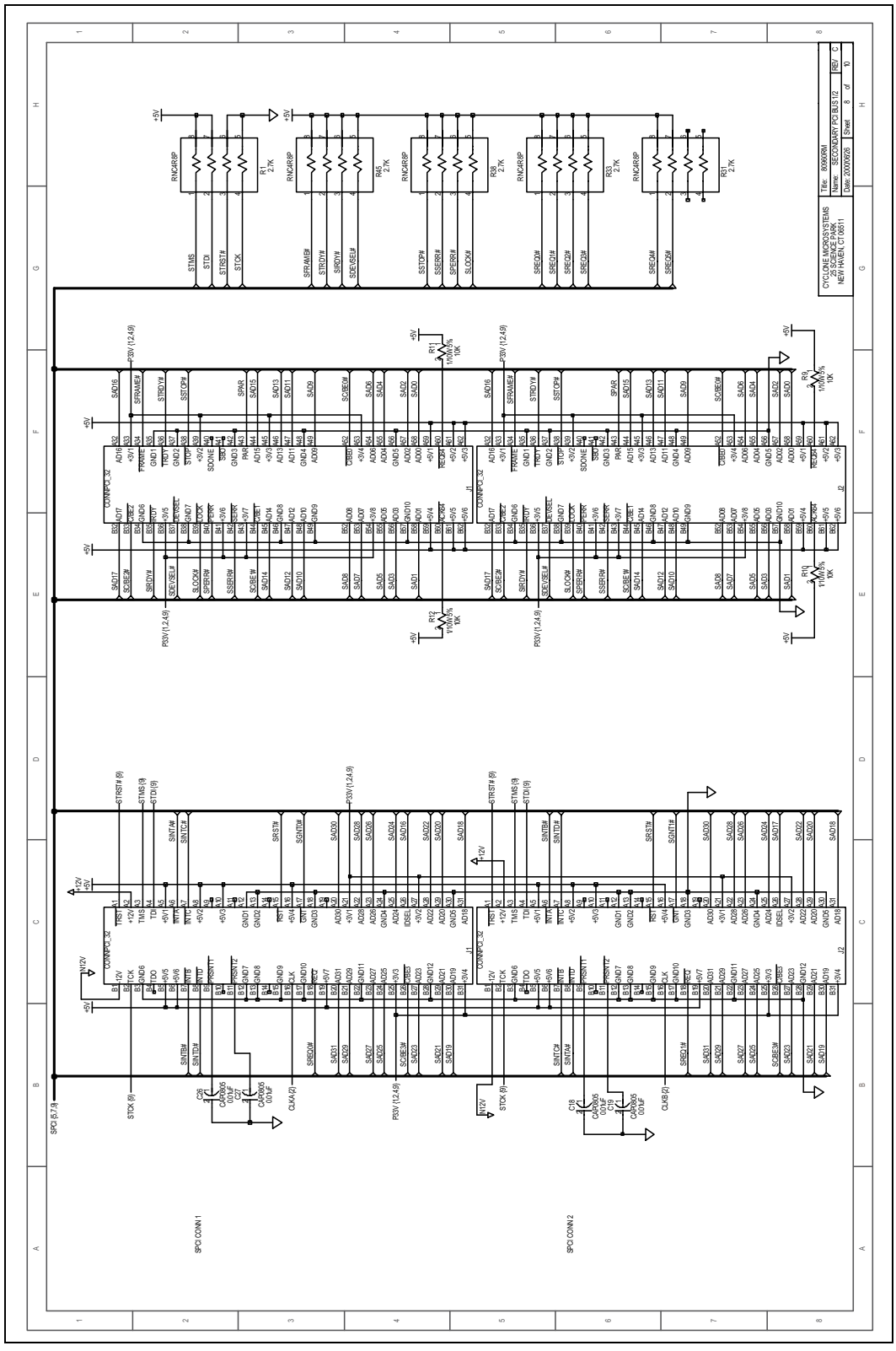


Figure 15-44. Secondary PCI Bus 3/4 Schematic

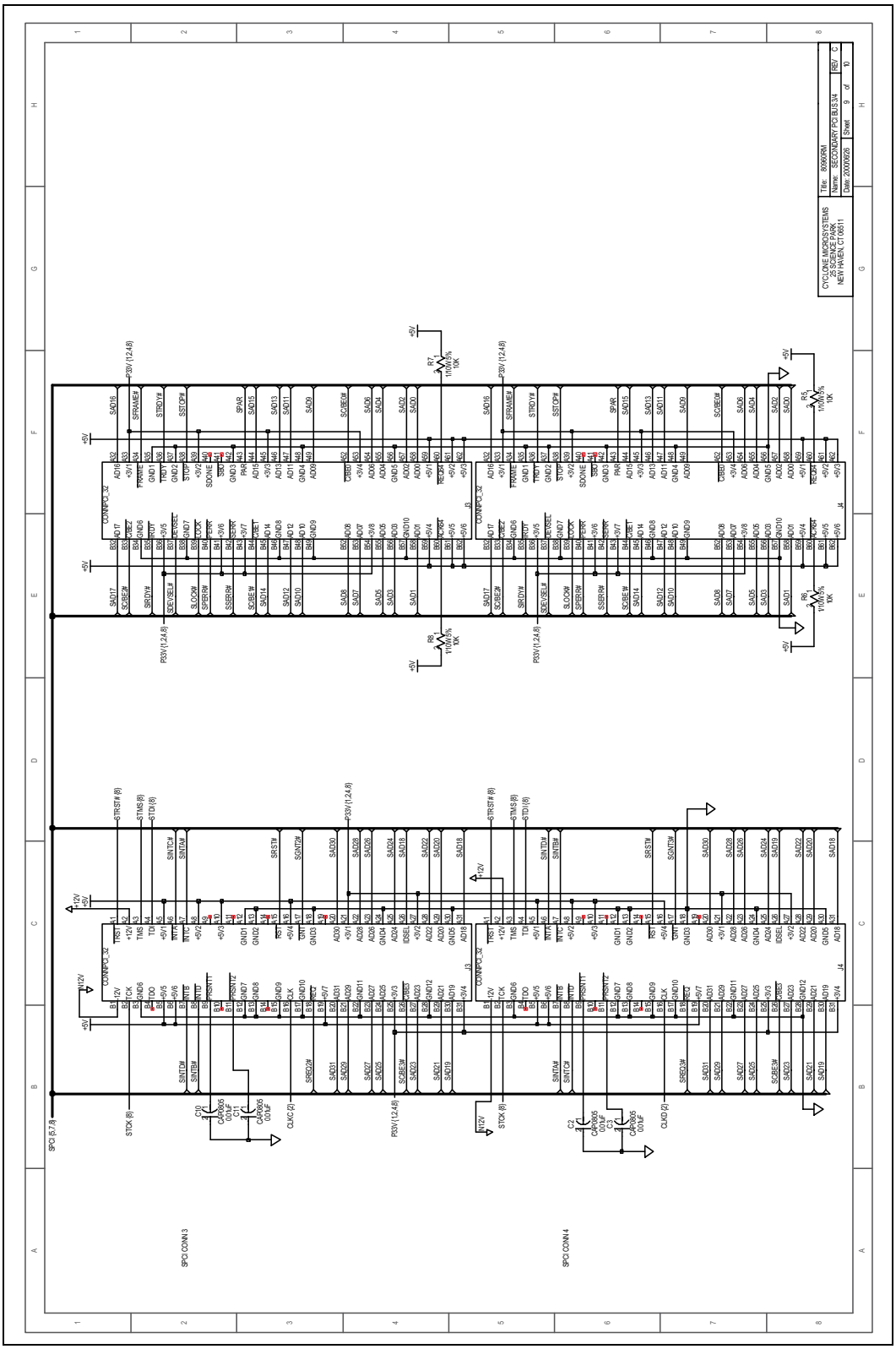
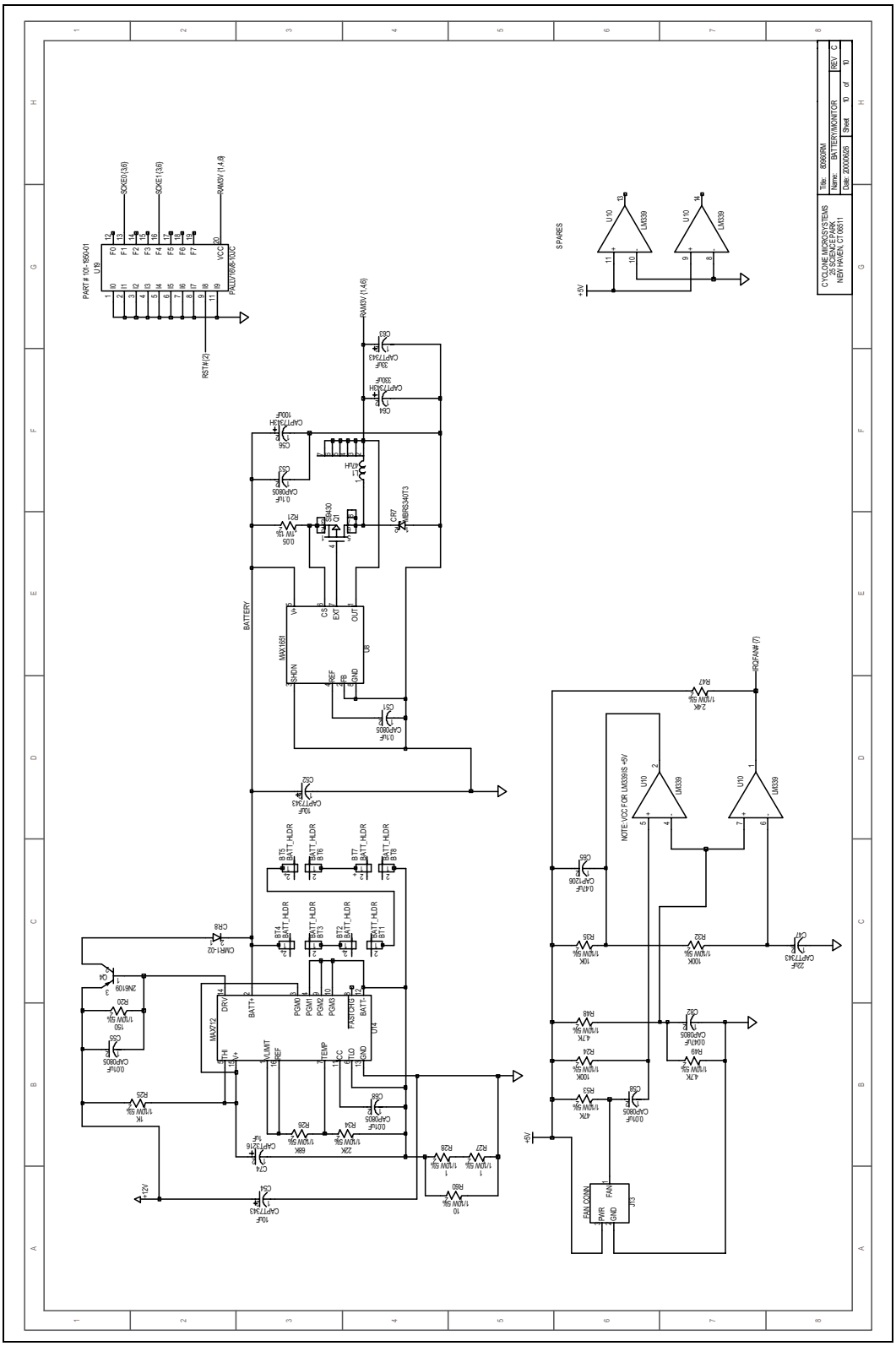


Figure 15-45. Battery Monitor Schematic



Intel® IQ80960RM Board Bill of MaterialB

This appendix identifies all components on the IQ80960RM Evaluation Platform (Table B-1).

Table B-1. Intel® IQ80960RM Bill of Materials (Sheet 1 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
1	1	U13	IC/SM 74ALS32 SOIC-14	National Semiconductor	DM74ALS32M
2	1	U6	IC/SM 74ALS04 SOIC	National Semiconductor	DM74ALS04BM
3	1	U3	IC/SM 74ABT273 SOIC	Texas Instruments	SN74ABT273DW
4	2	U1, U2	IC/SM 74ABT573 SOIC	Texas Instruments	SN74ABT573DW
5	1	U16	IC/SM 74ALS08 SOIC	National Semiconductor	DM74ALS08M
6	1	U5	IC / SM 1488A SOIC	National Semiconductor	DS1488M
7	1	U7	IC / SM 1489A SOIC	National Semiconductor	DS1489AM
8	1	Q1	IC/SM Si9430DY SOIC-8	Siliconix	Si9430DY
9	1	U9	IC/SM LVCMOS Fanout Buffr SSOP	Motorola	MPC9140
10	1	U10	IC/SM LM339 SOIC-14	National Semiconductor	LM339M
11	1	U8	IC/SM MAX1651CSA SOIC-8	Maxim	MAX1651CSA
12	1	U14	IC/SM MAX712CSE SOIC-16	Maxim	MAX712CSE
13	1	U17	IC/SM MAX767CAP SOIC	Maxim	MAX767CAP
14	1	U15	PROCESSOR (frm Intel) i960RM	Intel	
15	1	U12	VLSI I/O UART 16C550 PLCC	Texas Instruments	TL16C550AFN
16	1	C65	CAP SM, 0.47 µF (1206) Philips	Philips	12062F474Z9BB0
17	15	C2, C3, C10, C11, C18, C19, C26, C27, C55, C58, C61, C68, C77, C83, C96	CAP SM, 0.01 µF (0805)	Kemet	C0805C103K5RAC

Table B-1. Intel® IQ80960RM Bill of Materials (Sheet 2 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
18	79	C1, C4, C5, C6, C7, C8, C9, C12, C13, C14, C15, C16, C17, C20, C21, C22, C23, C24, C25, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C48, C49, C50, C51, C53, C59, C62, C66, C67, C69, C70, C71, C73, C79, C80, C81, C85, C86, C87, C94, C95, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C111, C112, C113, C114, C115, C116, C117	CAP SM, 0.1 µF (0805)	Philips	08052R104K8BB2
19	1	C110	CAP SM, 18 pF(0805)	Kemet	C0805C180J5GAC
20	2	R27, R28	R/SM 1/10 W 5% 1 ohm (0805)	Dale	CRCW0805100JT
21	1	R60	R/SM 1/10 W 5% 10 ohm (0805)	Dale	CRCW08051000JT
22	1	R25	R/SM 1/10 W 5% 1 Kohm (0805)	Dale	CRCW08051001FRT
23	12	R5, R6, R7 R8, R9, R10, R11, R12, R35, R39, R58, R59	R/SM 1/10 W 5% 10 Kohm (0805)	Dale	CRCW08051002FRT
24	2	R24, R32	R/SM 1/10 W 5% 100 Kohm (0805)	Dale	CRCW08051003FRT
25	1	R20	R/SM 1/10 W 1% 150 ohm (0805)	Dale	CRCW08051500FRT
26	3	R14, R41, R42	R/SM 1/10 W 5% 1.5 Kohm (0805)	Dale	CRCW0805152JT
27	1	R18	R/SM 1/10 W 5% 1.6 Kohm (0805)	Dale	CRCW0805162JT
28	2	R50, R51	R/SM 1/10 W 5% 22 ohm (0805)	Dale	CRCW0805220JT
29	1	R34	R/SM 1/10 W 5% 22 Kohm (0805)	Dale	CRCW0805223JT

Table B-1. Intel® IQ80960RM Bill of Materials (Sheet 3 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
30	1	R37	R/SM 1/10 W 5% 24 ohm (0805)	Dale	CRCW0805240JT
31	1	R47	R/SM 1/10 W 5% 2.4 Kohm (0805)	Dale	CRCW0805242JT
32	1	R57	R/SM 1/10 W 5% 2.7 Kohm (0805)	Dale	CRCW0805272JT
33	1	R19	R/SM 1/10 W 5% 330 ohm (0805)	Dale	CRCW0805331JT
34	1	R29	R/SM 1/10 W 5% 36 ohm (0805)	Dale	CRCW0805360JT
35	1	R17	R/SM 1/10 W 5% 470 ohm (0805)	Dale	CRCW 0805 471JT
36	2	R48, R49	R/SM 1/10 W 1% 4.7 Kohm (0805)	Dale	CRCW08054701FRT
37	1	R53	R/SM 1/10 W 5% 47 Kohm (0805)	Dale	CRCW0805473JT
38	1	R26	R/SM 1/10 W 5% 68 Kohm (0805)	Dale	CRCW0805683JT
39	4	R30, R43, R54, R56	R/SM 1/8 W 5% 10 ohm chip 1206	Dale	CRCW1206100FT
40	5	J8, J9, J10, J11, J12	CONN SM/TH Mictor 43P Recptcl	AMP	767054-1
41	4	J1, J2, J3, J4[a]	CONN PCI Slot 5V/PCB ThruHole	AMP	145154-4
42	1	J5	CONN DIMM 168P/RAng/Socket/TH	Molex	73790-0059
43	1	J7	CONN TJ6 PCB 6/6 LP through hole	KYCON	GM-N-66
44	1	J13	CONN/FAN ASSY/Socket/ThruHole	AMP	173981-03
45	1	J6	CONN Hdr 16 pin/w shell, pcb	AMP	103308-3
46	4	Z1, Z2, Z3, Z4	Jumper JUMP2X1	Molex	22-54-1402
47	1	L1	Inductor/SM 47 µH 20%	Coilcraft	D03340P-473
48	1	L2	Inductor/SM 3.3 µH 20%	Coilcraft	D03316P-332
49	1	S1	Switch/SM DIP4 Mors# DHS-4S	Mors	DHS-4S
50	1	U4	OSC 1.8432 MHz 1/2 - Through hole	Kyocera	KH0HC1CSE 1.843
51	1	U18	Clock Chip CY7B9910-7SC	Cypress	CY7B9910-7SC
52	1	CR5	LED Green	Hewlett Packard	HLMP-3507$010
53	1	CR3	LED-Red	Hewlett Packard	HLMP3301$010
54	1	CR4	LED Green LP	Hewlett Packard	HLMP4740#010
55	2	CR1, CR2	LED-Red-Small Group	Dialight	555-4001
56	2	Q2, Q3	Transistor/SM N-Channel	Harris	RFD16N05LSM
57	1	Q4	Transistor 2N6109 (Through Hole)	Motorola	2N6109
58	1	U19	SOCKET PLCC20 LP Surface Mount	AMP	822269-1
60	1	U11	SOCKET / SM / TSOP / 40 pin	Meritec	980020-40-02
61	8	BT1, BT2, BT3, BT4, BT5, BT6, BT7, BT8	Battery Clips/PC/Snap-In/AA	Keystone	#92
62	1	U19	PALLV16V8Z-20JI	AMD	PALLV16V8Z-20JI
63	1	U11	MEM Flash E28F016S5-090 TSOP	Intel	E28F016S5-090

Table B-1. Intel® IQ80960RM Bill of Materials (Sheet 4 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
64	8	BT1, BT2, BT3, BT4, BT5, BT6, BT7, BT8	Battery AA NiCd @ 600 mA/Hour	SAFT	NIC-AA-600-SAFT
65	1	U15	HeatSink/Fan Assy 80960RN/RM	Panasonic	UDQFNBEOIF
66	3	C84	CAP SM, 0.22 µF (1206)	Philips	12062E224M9BB2
67	3	C60, C75, C78	CAP TANT SM 220 µF, 10 V (7343)	AVX	TPSE227K010R010
68	4	C89, C90, C91, C93	CAP TANT SM 47 µF, 16 V (7343)	AVX	TPSD476K016R015
69	1	C63	CAP TANT SM 33 µF, 10 V (7343)	Sprague	293D336X9016D2T
70	4	C57, C76, C88, C92	CAP TANT SM 4.7 µF, 35 V (7343)	Sprague	293D475X9035D2T
71	1	C47	CAP TANT SM 22 µF, 20 V (7343)	Sprague	293D226X9020D2T
72	1	C74	CAP TANT SM 1 µF, 16 V (3216)	Sprague	293D105X0016A2T
73	2	C52, C54	CAP TANT SM 10 µF, 25/35 V	Sprague	293D1060025D2T
74	1	C56	CAP TANT SM 100 µF 10 V (7343)	AVX	TPSD107K010R0100
75	1	C64	CAP TANT SM 330 µF 6.3 V (7343)	AVX	TPSE337K063R0100
76	1	C82	CAP SM, 0.047 µF (0805)	Kemet	C0805C473K5RAC
77	1	R46	Res/SM 1 W 1% 0.012 ohm (2512)	Dale	WSL-2512-R012
78	1	R21	Res/SM 1 W 1% 0.05 ohm (2512)	Dale	WSL-2512-R050
79	1	R52	Resistor/SM 1/2 W 5% 100 ohm	Beckmen	BCR 1/2 101 JT
80	7	R1, R31, R33, R36, R38, R44, R45	Resistor Pk SM RNC4R8P 2.7 Kohm	CTS	742083272JTR
81	2	R40, R55	Resistor Pk SM RNC4R8P 22 ohm	CTS	742083220JTR
82	2	R15, R16	Resistor Pk SM RNC4R8P 470 ohm	CTS	742083471JTR
83	1	R13	Resistor Pk SM RNC4R8P 1.5 Kohm	CTS	742083152JTR
84	2	R22, R23	Resistor Pk SM RNC4R8P 30 ohm	CTS	742083300JTR
85	1	CR9	Diode CMPSH3 Surface Mount	Central Semiconductor	CMPSH3
86	2	CR6, CR7	Diode SM / MBRS340T3	Motorola	MBRS340T3
87	1	CR8	Diode/SM 1N4001 (CMR1-02)	Central Semiconductor	CMR1-02
88	1	J5	SDRAM, DIMM, ECC, 2Mx72, 16 MB	Unigen	UG52S7408GSG

a. Connectors for IQ80960RM, CONN PCI 32-BIT 5 V/PCB ThruHole, AMP #145154-4.

Intel® i960® RN I/O Processor Schematics C

Schematics in this document supersede schematics in Document #AZ1-00886.

Figure 15-46. Decoupling and 3.3 V Power Schematic

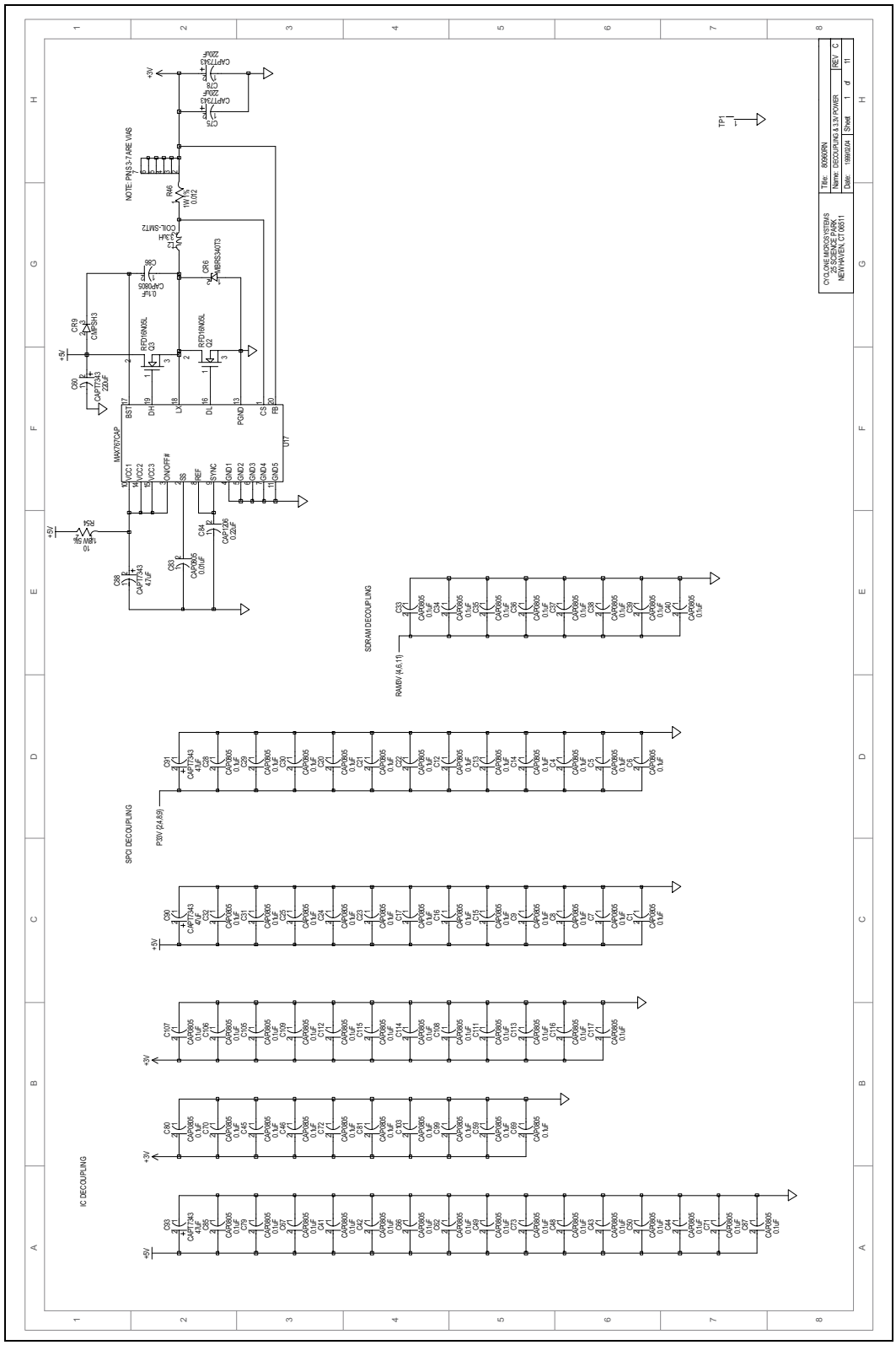


Figure 15-47. Primary PCI Interface Schematic

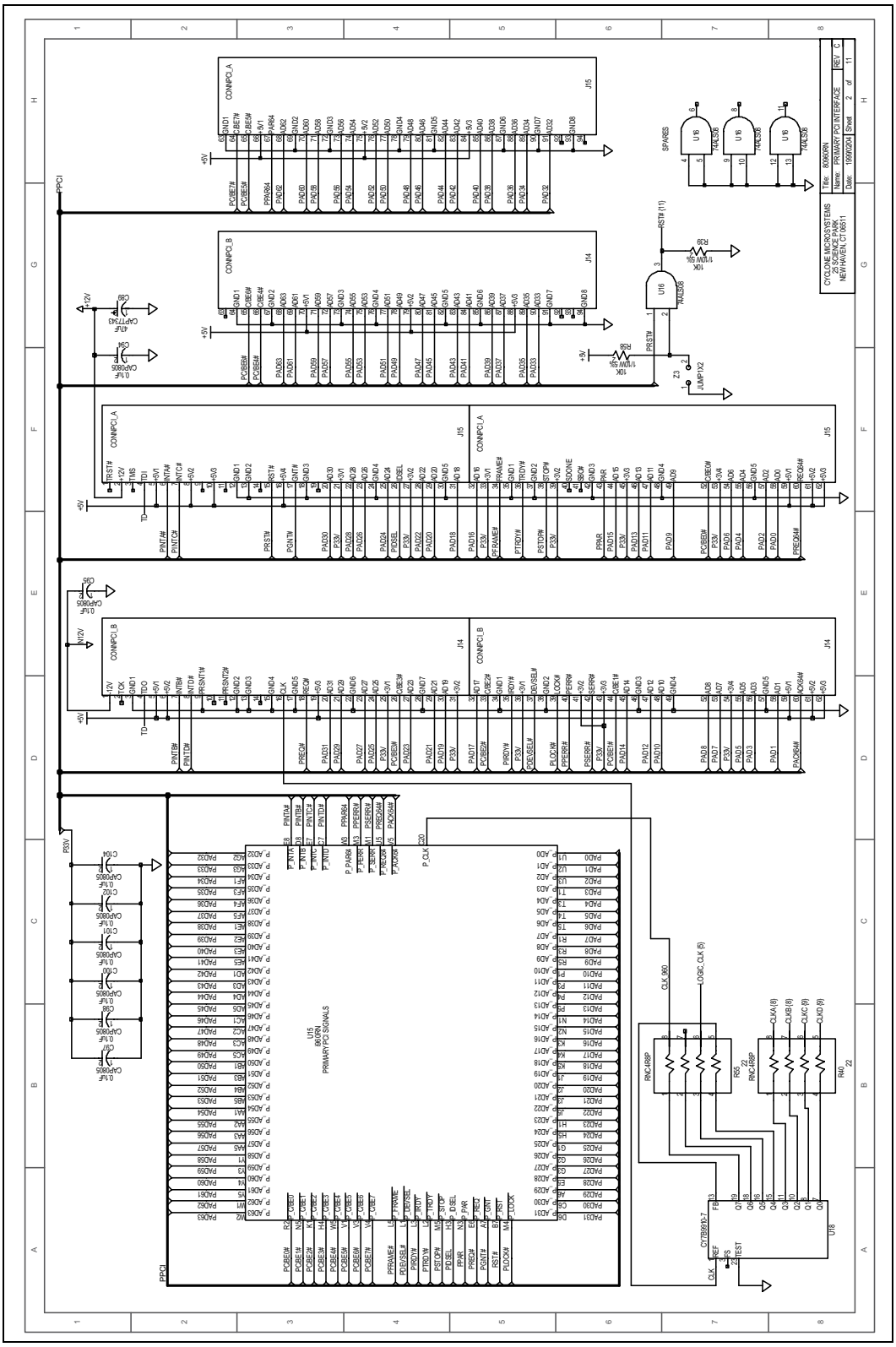


Figure 15-48. Memory Controller Schematic

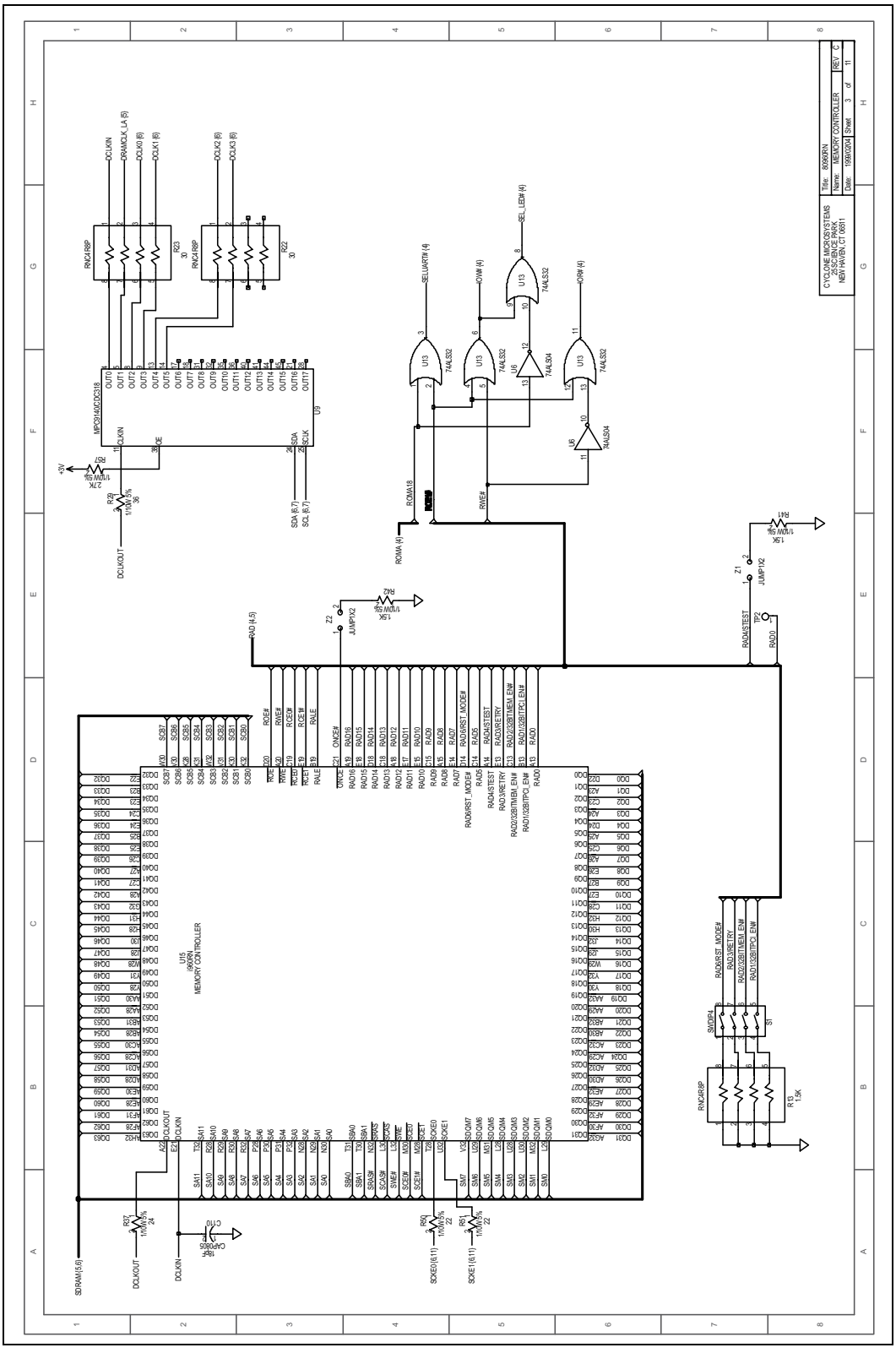


Figure 15-49. Flash ROM, UART and LEDs Schematic

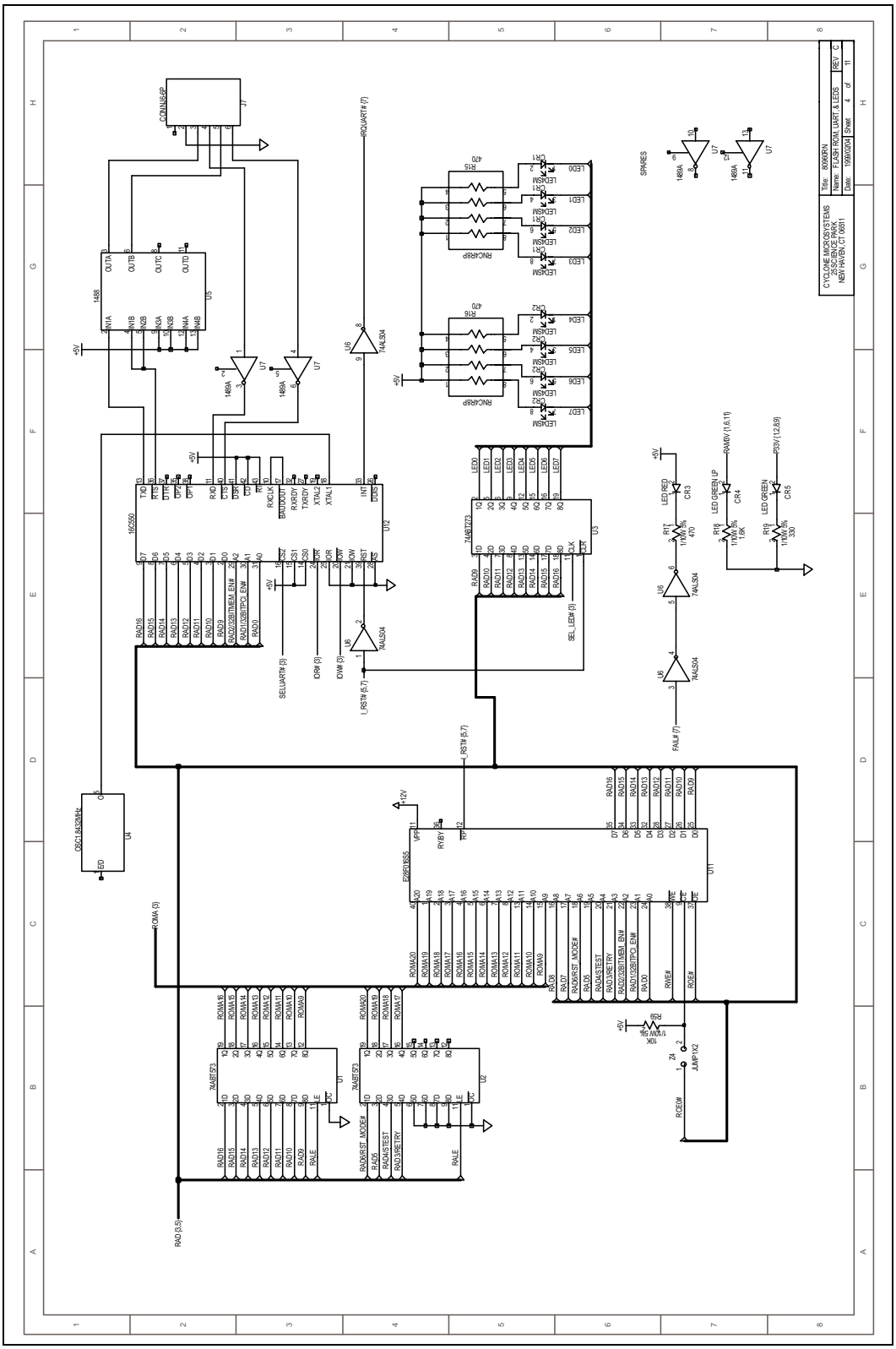


Figure 15-50. Logic Analyzer I/F Schematic

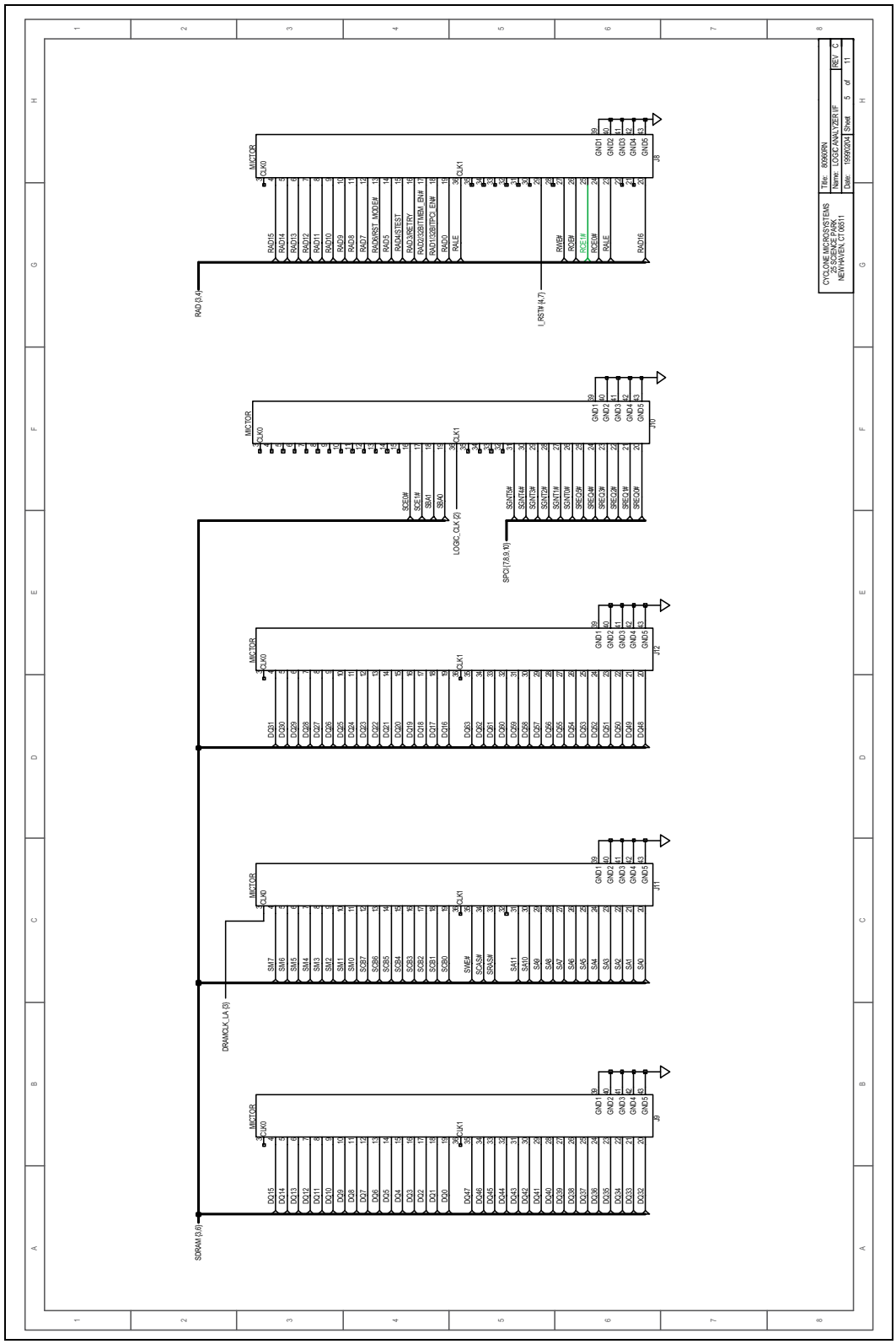


Figure 15-51. SDRAM 168-Pin DIMM Schematic

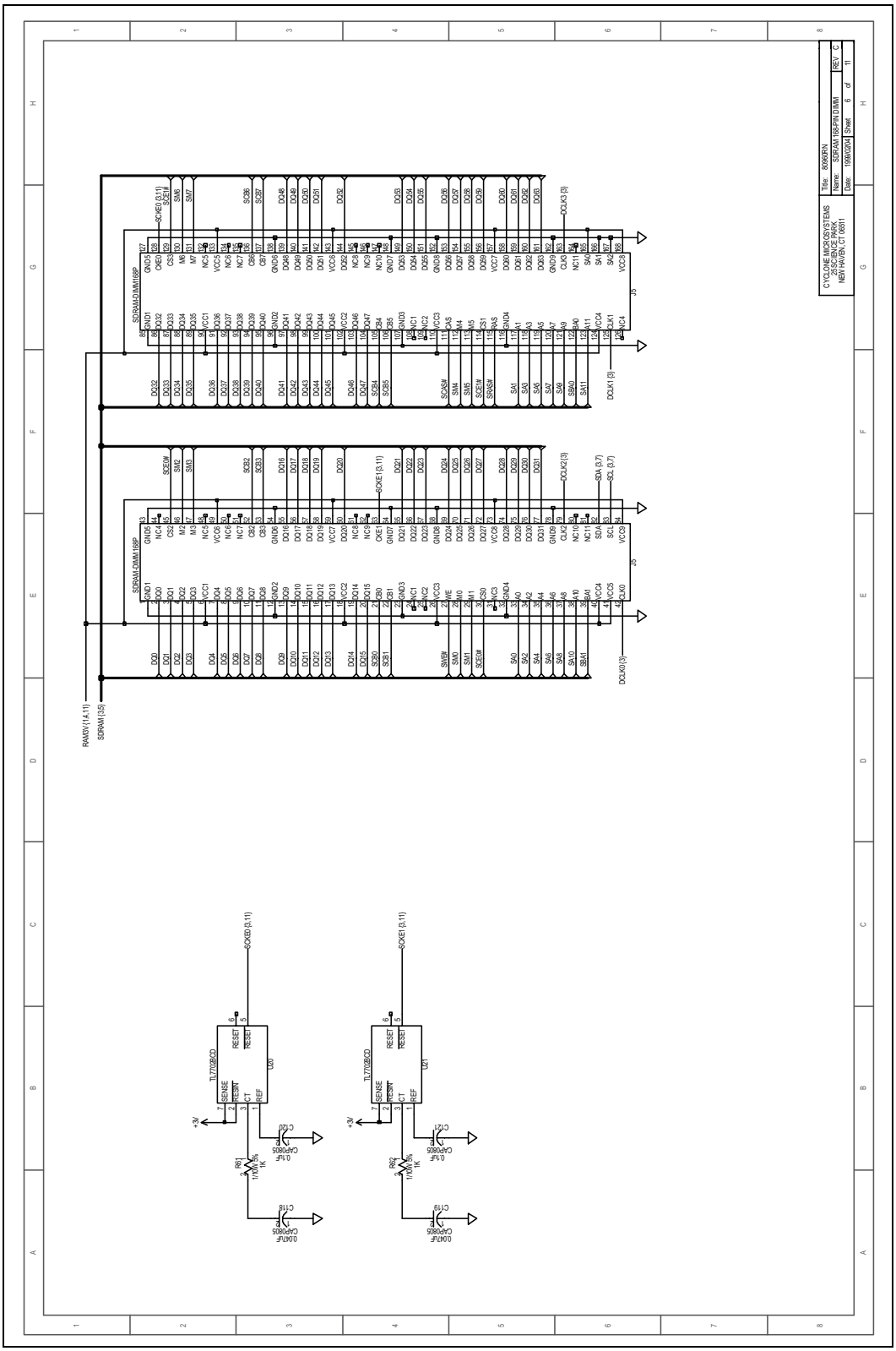


Figure 15-52. Secondary PCI/80960 Core Schematic

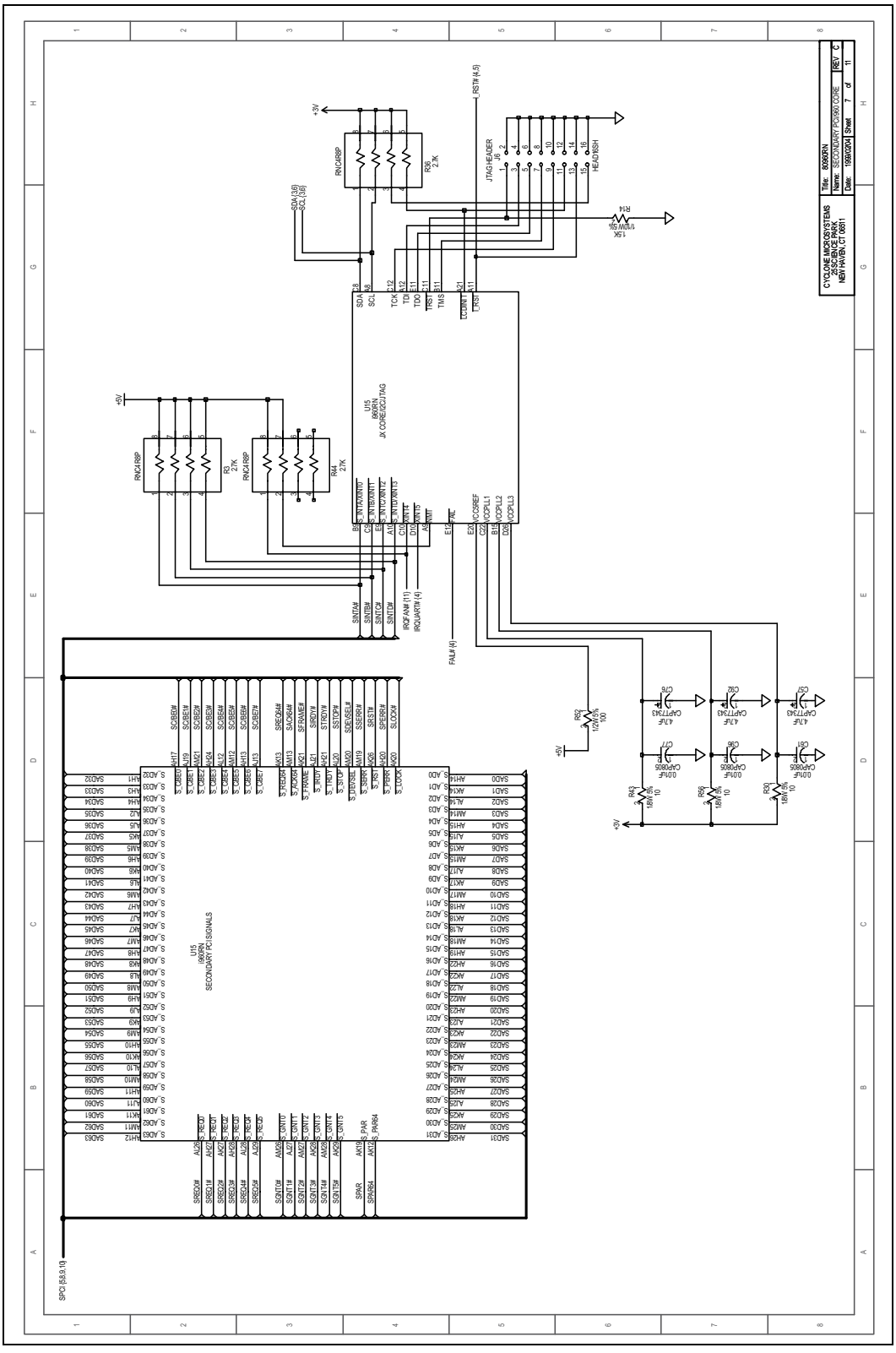


Figure 15-53. Secondary PCI Bus 1/2 Schematic

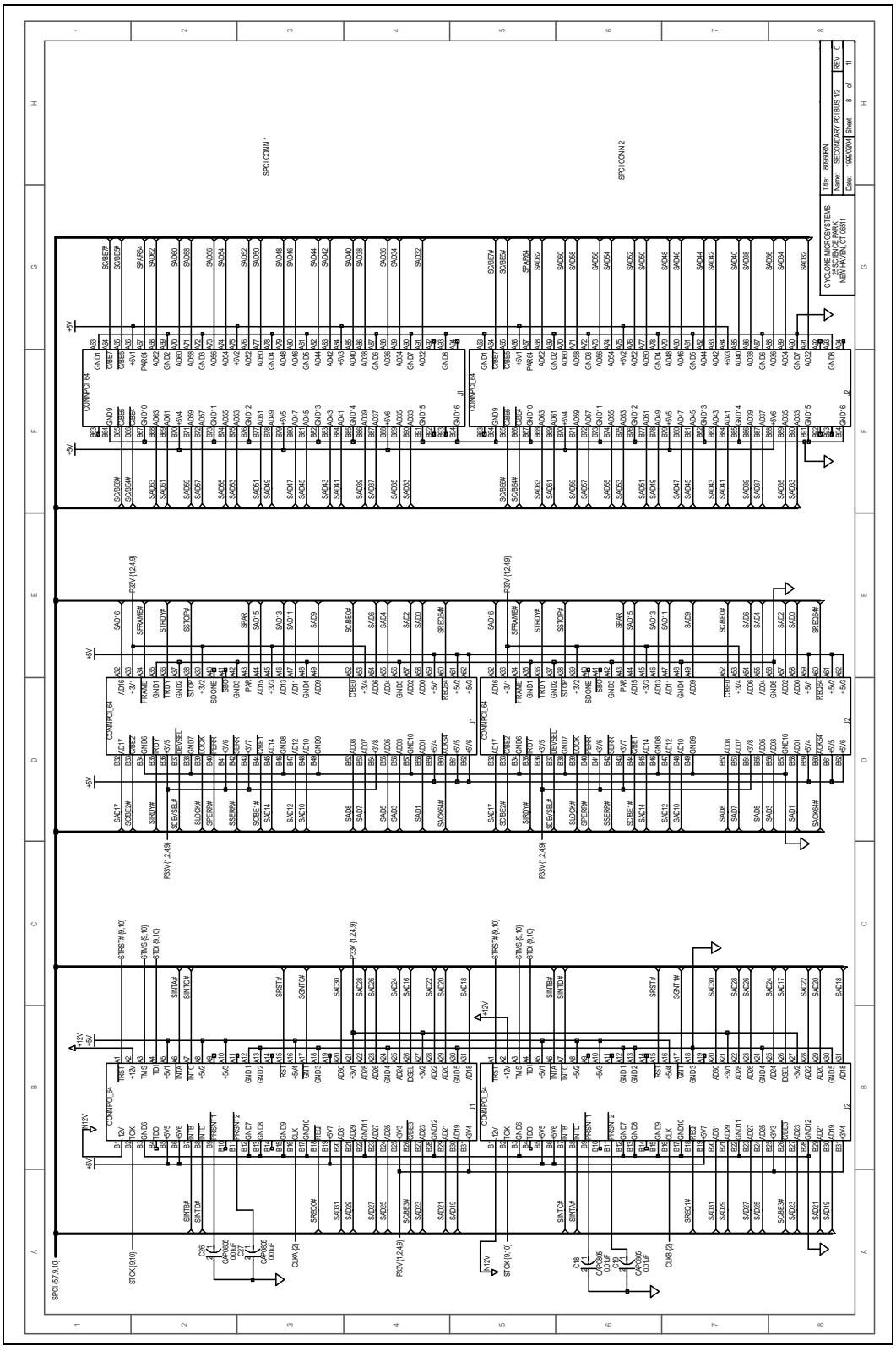


Figure 15-54. Secondary PCI Bus 3/4 Schematic

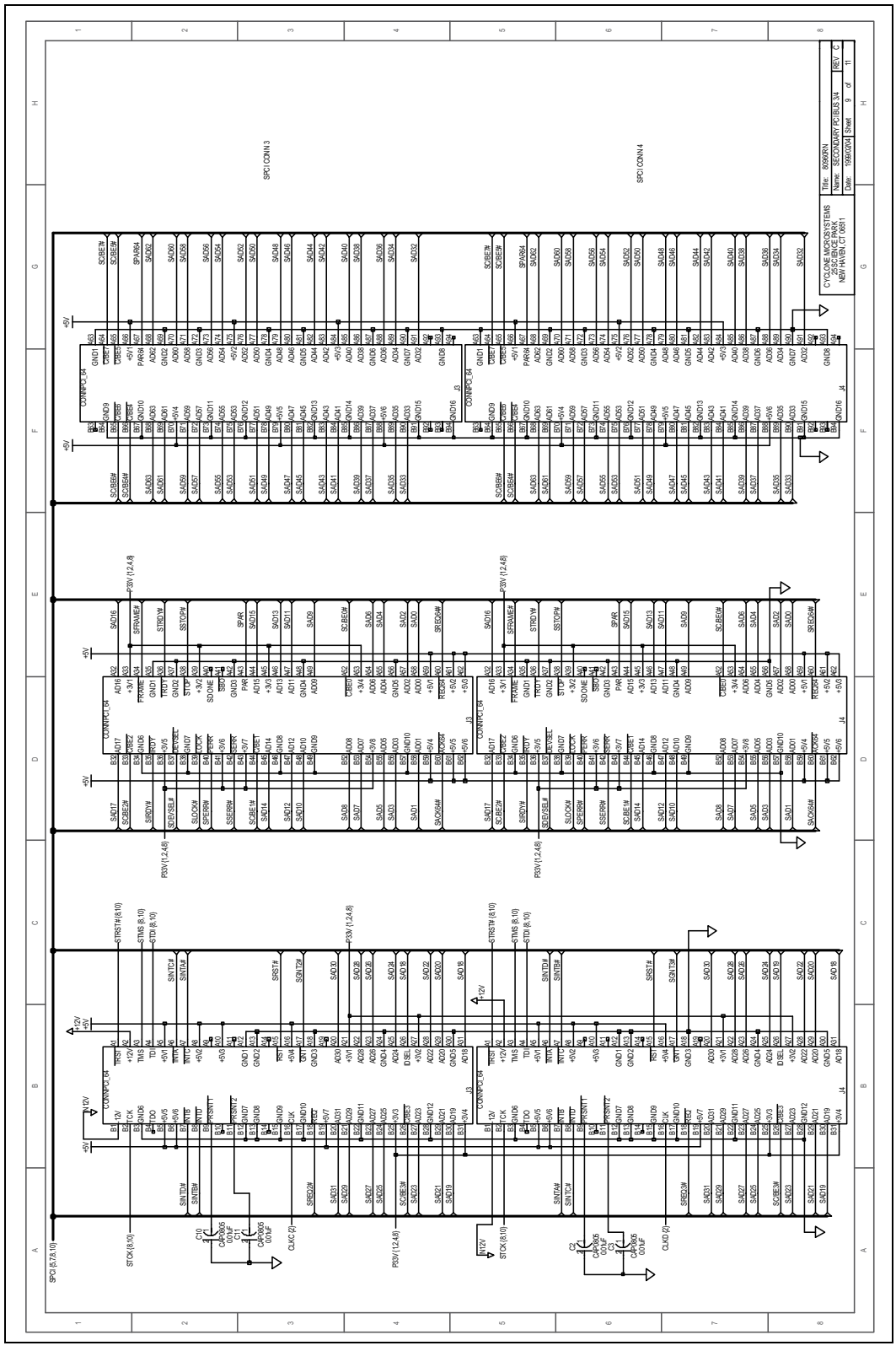


Figure 15-55. SPCI Pull-Ups Schematic

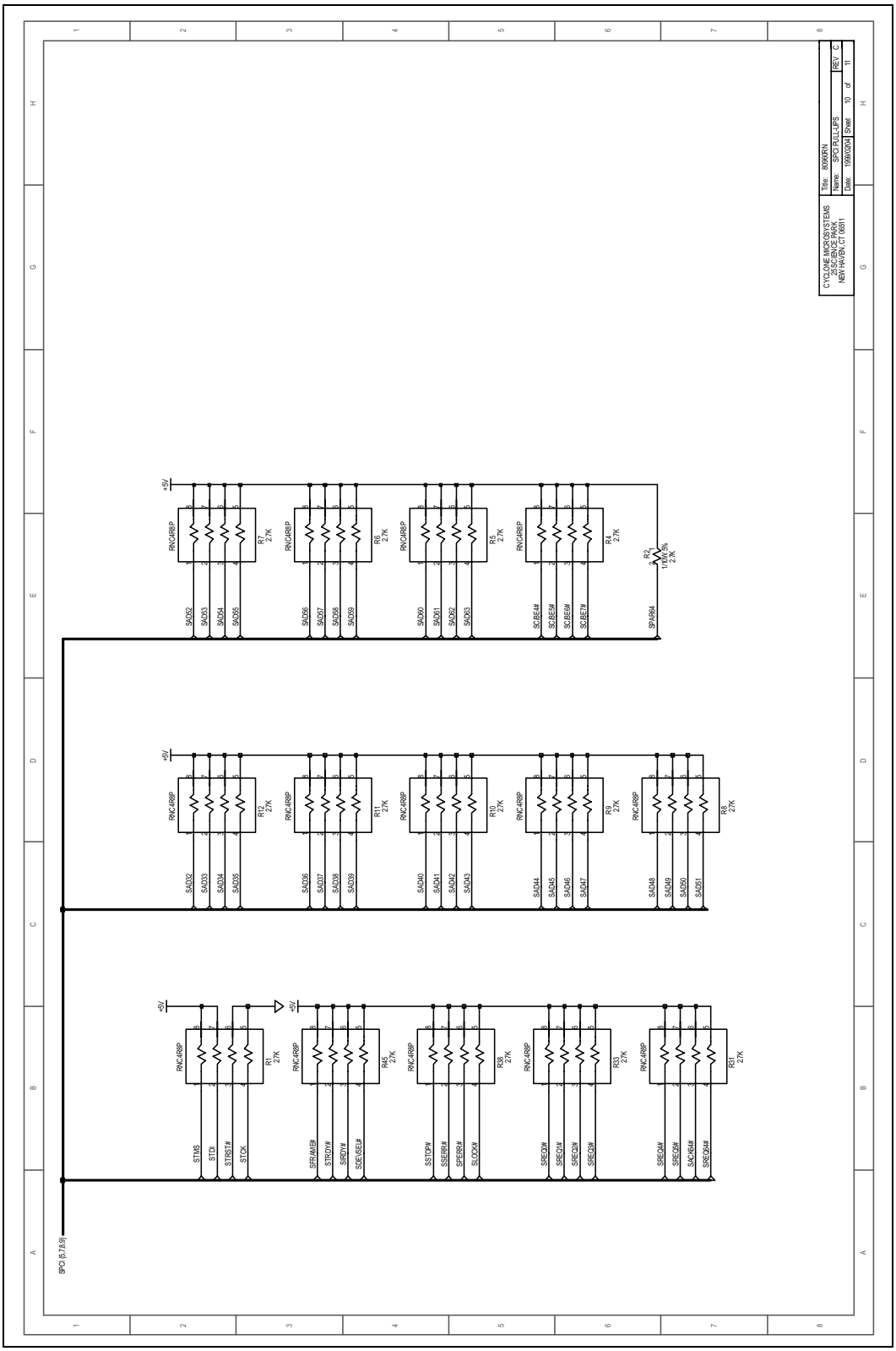
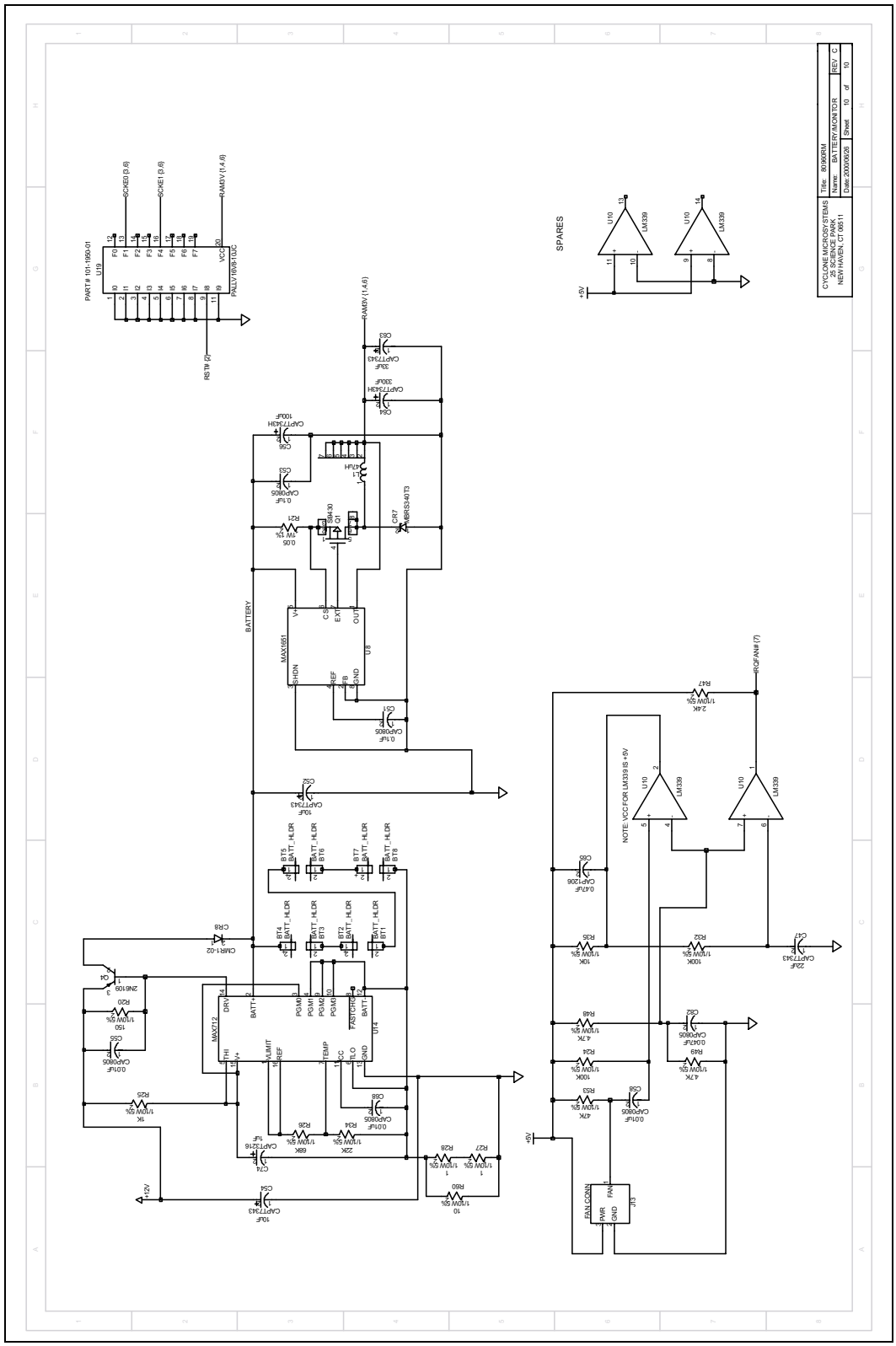


Figure 15-56. Battery/Monitor Schematic



Intel® IQ80960RN Board Bill of MaterialD

This appendix identifies all components on the IQ80960RN Evaluation Platform (Table D-1).

Table D-1. Intel® IQ80960RN Bill of Materials (Sheet 1 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
1	1	U13	IC/SM 74ALS32 SOIC-14	National Semiconductor	DM74ALS32M
2	1	U6	IC/SM 74ALS04 SOIC	National Semiconductor	DM74ALS04BM
3	1	U3	IC/SM 74ABT273 SOIC	Texas Instruments	SN74ABT273DW
4	2	U1,U2	IC/SM 74ABT573 SOIC	Texas Instruments	SN74ABT573DW
5	1	U16	IC/SM 74ALS08 SOIC	National Semiconductor	DM74ALS08M
6	1	U5	IC / SM 1488A SOIC	National Semiconductor	DS1488M
7	1	U7	IC / SM 1489A SOIC	National Semiconductor	DS1489AM
8	1	Q1	IC/SM Si9430DY SOIC-8	Siliconix	Si9430DY
9	1	U9	IC/SM LVCMOS Fanout Buffr SSOP	Motorola	MPC9140
10	1	U10	IC/SM LM339 SOIC-14	National Semiconductor	LM339M
11	1	U8	IC/SM MAX1651CSA SOIC-8	Maxim	MAX1651CSA
12	1	U14	IC/SM MAX712CSE SOIC-16	Maxim	MAX712CSE
13	1	U17	IC/SM MAX767CAP SOIC	Maxim	MAX767CAP
14	1	U15	80960RN PROCESSOR	Intel	
15	1	U12	VLSI I/O UART 16C550 PLCC	Texas Instruments	TL16C550AFN
16	1	C65	CAP SM, 0.47 µF (1206) Philips	Philips	12062F474Z9BB0
17	15	C2, C3, C10, C11, C18, C19, C26, C27, C55, C58, C61, C68, C77, C83, C96	CAP SM, 0.01 µF (0805)	Kemet	C0805C103K5RAC

Table D-1. Intel® IQ80960RN Bill of Materials (Sheet 2 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
18	79	C1, C4, C5, C6, C7, C8, C9, C12, C13, C14, C15, C16, C17, C20, C21, C22, C23, C24, C25, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C48, C49, C50, C51, C53, C59, C62, C66, C67, C69, C70, C71, C73, C79, C80, C81, C85, C86, C87, C94, C95, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C111, C112, C113, C115, C116, C114, C117	CAP SM, 0.1 µF (0805)	Philips	08052R104K8BB2
19	1	C110	CAP SM, 18 pF (0805)	Kemet	C0805C180J5GAC
20	2	R27, R28	R/SM 1/10 W 5% 1 ohm (0805)	Dale	CRCW0805100JT
21	1	R60	R/SM 1/10 W 5% 10 ohm (0805)	Dale	CRCW08051000JT
22	1	R25	R/SM 1/10 W 5% 1 Kohm (0805)	Dale	CRCW08051001FRT
23	4	R35, R39, R58, R59	R/SM 1/10 W 5% 10 Kohm (0805)	Dale	CRCW08051002FRT
24	2	R24, R32	R/SM 1/10 W 5% 100 Kohm (0805)	Dale	CRCW08051003FRT
25	1	R20	R/SM 1/10 W 1% 150 ohm (0805)	Dale	CRCW08051500FRT
26	3	R14, R41, R42	R/SM 1/10 W 5% 1.5 Kohm (0805)	Dale	CRCW0805152JT
27	1	R18	R/SM 1/10 W 5% 1.6 Kohm (0805)	Dale	CRCW0805162JT
28	2	R50, R51	R/SM 1/10 W 5% 22 ohm (0805)	Dale	CRCW0805220JT
29	1	R34	R/SM 1/10 W 5% 22 Kohm (0805)	Dale	CRCW0805223JT
30	1	R37	R/SM 1/10 W 5% 24 ohm (0805)	Dale	CRCW0805240JT
31	1	R47	R/SM 1/10 W 5% 2.4 Kohm (0805)	Dale	CRCW0805242JT
32	2	R2, R57	R/SM 1/10 W 5% 2.7 Kohm (0805)	Dale	CRCW0805272JT

Table D-1. Intel® IQ80960RN Bill of Materials (Sheet 3 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
33	1	R19	R/SM 1/10 W 5% 330 ohm (0805)	Dale	CRCW0805331JT
34	1	R29	R/SM 1/10 W 5% 36 ohm (0805)	Dale	CRCW0805360JT
35	1	R17	R/SM 1/10 W 5% 470 ohm (0805)	Dale	CRCW 0805 471JT
36	2	R48, R49	R/SM 1/10 W 1% 4.7 Kohm (0805)	Dale	CRCW08054701FRT
37	1	R53	R/SM 1/10 W 5% 47 Kohm (0805)	Dale	CRCW0805473JT
38	1	R26	R/SM 1/10 W 5% 68 Kohm (0805)	Dale	CRCW0805683JT
39	4	R30, R43, R54, R56	R/SM 1/8 W 5% 10 ohm chip 1206	Dale	CRCW1206100FT
40	5	J8, J9, J10, J11, J12	CONN SM/TH Mictor 43P Recptcl	AMP	767054-1
41	4	J1, J2, J3, J4[a]	CONN PCI 64BIT 5 V/PCB ThruHole	AMP	145166-4
42	1	J5	CONN DIMM 168P/RAng/Socket/TH	Molex	73790-0059
43	1	J7	CONN TJ6 PCB 6/6 LP through hole	KYCON	GM-N-66
44	1	J13	CONN/FAN ASSY/Socket/ThruHole	AMP	173981-03
45	1	J6	CONN Hdr 16 pin/w shell, pcb	AMP	103308-3
46	4	Z1, Z2, Z3, Z4	Jumper JUMP2X1	Molex	22-54-1402
47	1	L1	Inductor/SM 47µH 20%	Coilcraft	D03340P-473
48	1	L2	Inductor/SM 3.3 µH 20%	Coilcraft	D03316P-332
49	1	S1	Switch/SM DIP4 Mors# DHS-4S	Mors	DHS-4S
50	1	U4	OSC 1.8432 MHz 1/2 - Through hole	Kyocera	KH0HC1CSE 1.843
51	1	U18	Clock Chip CY7B9910-7SC	Cypress	CY7B9910-7SC
52	1	CR5	LED Green	Hewlett Packard	HLMP-3507$010
53	1	CR3	LED-Red	Hewlett Packard	HLMP3301$010
54	1	CR4	LED Green LP	Hewlett Packard	HLMP4740#010
55	2	CR1, CR2	LED-Red-Small Group	Dialight	555-4001
56	2	Q2, Q3	Transistor/SM N-Channel	Harris	RFD16N05LSM
57	1	Q4	Transistor 2N6109 (Through Hole)	Motorola	2N6109
58	1	U19	SOCKET PLCC20 LP Surface Mount	AMP	822269-1
60	8	BT1, BT2, BT3, BT4, BT5, BT6, BT7, BT8	Battery Clips/PC/Snap-In/AA	Keystone	#92
61	1	U19	PALLV16V8Z-20JI	AMD	PALLV16V8Z-20JI
62	1	U11	MEM Flash E28F016S5-090 TSOP	Intel	E28F016S5-090
63	8	BT1, BT2, BT3, BT4, BT5, BT6, BT7, BT8	Battery AA NiCd @ 600 mA/Hour	SAFT	NIC-AA-600-SAFT
64	1	U15	HeatSink/Fan Assy 80960RM/RN	Panasonic	UDQFNBEOIF

Table D-1. Intel® IQ80960RN Bill of Materials (Sheet 4 of 4)

Item	Qty	Location	Part Description	Manufacturer	Manufacturer Part #
65	1	C84	CAP SM, 0.22 µF (1206)	Philips	12062E224M9BB2
66	3	C60, C75, C78	CAP TANT SM 220 µF, 10 V (7343)	AVX	TPSE227K010R010
67	4	C89, C90, C91, C93	CAP TANT SM 47 µF, 16 V (7343)	AVX	TPSD476K016R015
68	1	C63	CAP TANT SM 33 µF, 10 V (7343)	Sprague	293D336X9016D2T
69	4	C57, C76, C88, C92	CAP TANT SM 4.7 µF, 35 V (7343)	Sprague	293D475X9035D2T
70	1	C47	CAP TANT SM 22 µF, 20 V (7343)	Sprague	293D226X9020D2T
71	1	C74	CAP TANT SM 1 µF, 16 V (3216)	Sprague	293D105X0016A2T
72	2	C52, C54	CAP TANT SM 10 µF, 25/35 V	Sprague	293D1060025D2T
73	1	C56	CAP TANT SM 100 µF 10 V (7343)	AVX	TPSD107K010R0100
74	1	C64	CAP TANT SM 330 µF 6.3 V (7343	AVX	TPSE337K063R0100
75	1	C82	CAP SM, 0.047 µF (0805)	Kemet	C0805C473K5RAC
76	1	R46	Res/SM 1 W 1% 0.012 ohm (2512)	Dale	WSL-2512-R012
77	1	R21	Res/SM 1 W 1% 0.05 ohm (2512)	Dale	WSL-2512-R050
78	1	R52	Resistor/SM 1/2 W 5% 100 ohm	Beckmen	BCR 1/2 101 JT
79	16	R1, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R33, R36, R38, R44, R45,	Resistor Pk SM RNC4R8P 2.7 Kohm	CTS	742083272JTR
80	2	R40, R55	Resistor Pk SM RNC4R8P 22 ohm	CTS	742083220JTR
81	2	R15, R16	Resistor Pk SM RNC4R8P 470 ohm	CTS	742083471JTR
82	1	R13	Resistor Pk SM RNC4R8P 1.5 Kohm	CTS	742083152JTR
83	2	R22, R23	Resistor Pk SM RNC4R8P 30 ohm	CTS	742083300JTR
84	1	CR9	Diode CMPSH3 Surface Mount	Central Semiconductor	CMPSH3
85	2	CR6, CR7	Diode SM / MBRS340T3	Motorola	MBRS340T3
86	1	CR8	Diode/SM 1N4001 (CMR1-02)	Central Semiconductor	CMR1-02
87	1	J5	SDRAM, DIMM, ECC, 2Mx72, 16 MB	Unigen	UG52S7408GSG

a. Connectors for IQ80960RN, CONN PCI 32-BIT 5 V/PCB ThruHole, AMP #145154-4.

Intel® IQ80960RM/RN SDRAM Battery Backup PLD Equations E

```
MODULE BATT

//TITLE          SDRAM Battery Backup Enable
//PATTERN101-1809-01
//REVISION
//AUTHORJ. Neumann
//COMPANYCyclone Microsystems Inc.
//DATE           10/30/97
//CHIP           PALLV16V8Z-20JI
// 1/20/98 Modify target device to PALLV16V8Z-20JI

//Initial release.

        PRSTn       PIN 9;//Primary PCI reset
        SCKE0           PIN 13; //SDRAM bank 0 clock enable
        SCKE1           PIN 16; //SDRAM bank 1 clock enable
        OUT0            PIN 14; //SCKE0 output enable
        OUT1            PIN 17; //SCKE1 output enable

EQUATIONS

// If SDRAM clock enable goes low, SDRAM clock enable
// must be held low to ensure that the SDRAM is held in auto refresh mode.
// Reset going high will release the hold on SCKE.

        OUT0 = SCKE0.PIN & PRSTn//SCKE is the set term, PRSTn is the reset term
            # SCKE0.PIN & OUT0.PIN
            # !SCKE0.PIN & PRSTn;

        SCKE0 = 0;
        SCKE0.OE = !OUT0;//When OUT = 0, SCKE is grounded
                                        //When OUT = 1, SCKE is high impedance

        OUT1 = SCKE1.PIN & PRSTn
            # SCKE1.PIN & OUT1.PIN
            # !SCKE1.PIN & PRSTn;

        SCKE1 = 0;

        SCKE1.OE = !OUT1;
```

Intel® 80960RM/RN Processor PBGA Signal Ball Map F

Table F-1 details the ballout for the 80960RM processor.

Table F-1. 540-Lead H-PBGA Pinout — Intel® i960® RM I/O Processor Processor (Sheet 1 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	V_{SS}	A32	V_{SS}	B31	V_{CC}
A2	V_{SS}	B1	V_{SS}	B32	V_{SS}
A3	V_{SS}	B2	V_{CC}	C1	V_{SS}
A4	V_{SS}	B3	V_{CC}	C2	V_{CC}
A5	V_{SS}	B4	V_{CC}	C3	V_{CC}
A6	P_AD29	B5	V_{CC}	C4	V_{SS}
A7	P_GNT#	B6	V_{CC}	C5	V_{CC}
A8	SCL	B7	P_RST#	C6	P_AD30
A9	NMI#	B8	V_{CC}	C7	P_INTD#
A10	XINT3#	B9	XINT0#	C8	SDA
A11	I_RST#	B10	V_{CC}	C9	XINT1#
A12	TDI	B11	TMS	C10	XINT4#
A13	RAD00	B12	V_{CC}	C11	TRST#
A14	RAD04	B13	RAD01	C12	TCK
A15	RAD08	B14	V_{CC}	C13	RAD02
A16	N/C	B15	V_{CCPLL2}	C14	RAD05
A17	V_{CC}	B16	V_{CC}	C15	RAD09
A18	RAD12	B17	V_{CC}	C16	V_{CC}
A19	RAD16	B18	V_{CC}	C17	V_{SS}
A20	RWE#	B19	RALE	C18	RAD13
A21	LCDINIT#	B20	V_{CC}	C19	RCE0#
A22	DCLKOUT	B21	V_{SS}	C20	P_CLK
A23	DQ01	B22	V_{CC}	C21	ONCE#
A24	DQ03	B23	DQ33	C22	V_{CCPLL1}
A25	DQ05	B24	V_{CC}	C23	DQ02
A26	DQ07	B25	DQ37	C24	DQ35
A27	DQ40	B26	V_{CC}	C25	DQ06
A28	DQ42	B27	DQ09	C26	DQ39
A29	V_{CC}	B28	V_{CC}	C27	DQ41
A30	V_{SS}	B29	V_{CC}	C28	DQ11
A31	V_{SS}	B30	V_{CC}	C29	V_{CC}

Table F-1. 540-Lead H-PBGA Pinout — Intel® i960® RM I/O Processor Processor (Sheet 2 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
C30	V_{CC}	E5	P_AD28	G2	P_AD26
C31	V_{CC}	E6	P_REQ#	G3	P_AD27
C32	V_{SS}	E7	P_INTC#	G4	V_{SS}
D1	V_{SS}	E8	P_INTA#	G5	N/C
D2	V_{CC}	E9	XINT2#	G28	V_{SS}
D3	V_{SS}	E10	V_{CC}	G29	V_{SS}
D4	V_{SS}	E11	TDO	G30	V_{CC}
D5	V_{SS}	E12	FAIL#	G31	V_{CC}
D6	P_AD31	E13	RAD03	G32	DQ43
D7	V_{SS}	E14	RAD07	H1	P_AD23
D8	P_INTB#	E15	RAD10	H2	V_{CC}
D9	V_{SS}	E16	V_{SS}	H3	P_IDSEL
D10	XINT5#	E17	RAD11	H4	P_C/BE3#
D11	V_{SS}	E18	RAD15	H5	P_AD24
D12	V_{CC}	E19	RCE1#	H28	DQ45
D13	V_{SS}	E20	V_{CC5REF}	H29	V_{SS}
D14	RAD06	E21	DCLKIN	H30	DQ13
D15	V_{SS}	E22	DQ32	H31	DQ44
D16	V_{SS}	E23	DQ34	H32	DQ12
D17	V_{SS}	E24	DQ36	J1	P_AD19
D18	RAD14	E25	DQ38	J2	P_AD20
D19	V_{SS}	E26	DQ08	J3	P_AD21
D20	ROE#	E27	DQ10	J4	V_{SS}
D21	V_{SS}	E28	V_{SS}	J5	P_AD22
D22	DQ00	E29	V_{SS}	J28	DQ47
D23	V_{SS}	E30	V_{SS}	J29	DQ15
D24	DQ04	E31	V_{CC}	J30	DQ46
D25	V_{SS}	E32	V_{SS}	J31	V_{CC}
D26	V_{CCPLL3}	F1	V_{SS}	J32	DQ14
D27	V_{SS}	F2	V_{CC}	K1	P_C/BE2#
D28	V_{SS}	F3	V_{CC}	K2	V_{CC}
D29	V_{SS}	F4	V_{CC}	K3	P_AD16
D30	V_{CC}	F5	V_{SS}	K4	P_AD17
D31	V_{CC}	F28	V_{SS}	K5	P_AD18
D32	V_{CC}	F29	V_{SS}	K28	SCB5
E1	V_{SS}	F30	V_{SS}	K29	V_{SS}
E2	V_{CC}	F31	V_{SS}	K30	SCB1
E3	V_{CC}	F32	V_{SS}	K31	SCB4
E4	V_{SS}	G1	P_AD25	K32	SCB0

Table F-1. 540-Lead H-PBGA Pinout — Intel® i960® RM I/O Processor Processor (Sheet 3 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
L1	P_DEVSEL#	P32	SA03	V31	SCB2
L2	P_TRDY#	R1	P_AD07	V32	SDQM7
L3	P_IRDY#	R2	P_C/BE0#	W1	P_AD62/ N/C
L4	V_{SS}	R3	P_AD08	W2	P_AD63/ N/C
L5	P_FRAME#	R4	V_{SS}	W3	P_PAR64/ N/C
L28	SDQM4	R5	P_AD09	W4	V_{SS}
L29	SDQM0	R28	SA10	W5	P_C/BE4#|| N/C
L30	SCAS#	R29	SA09	W28	DQ48
L31	V_{CC}	R30	SA08	W29	DQ16
L32	SWE#	R31	V_{CC}	W30	SCB7
M1	P_SERR#	R32	SA07	W31	V_{CC}
M2	V_{CC}	T1	P_AD03	W32	SCB3
M3	P_PERR#	T2	V_{CC}	Y1	P_AD58/ N/C
M4	P_LOCK#	T3	P_AD04	Y2	V_{CC}
M5	P_STOP#	T4	P_AD05	Y3	P_AD59/ N/C
M28	SCE1#	T5	P_AD06	Y4	P_AD60/ N/C
M29	V_{SS}	T28	SCKE0	Y5	P_AD61/ N/C
M30	SCE0#	T29	V_{SS}	Y28	DQ50
M31	SDQM5	T30	SBA1	Y29	V_{SS}
M32	SDQM1	T31	SBA0	Y30	DQ18
N1	P_AD14	T32	SA11	Y31	DQ49
N2	P_AD15	U1	P_AD00	Y32	DQ17
N3	P_PAR	U2	P_AD01	AA1	P_AD54/ N/C
N4	V_{SS}	U3	P_AD02	AA2	P_AD55/ N/C
N5	P_C/BE1#	U4	V_{SS}	AA3	P_AD56/ N/C
N28	SA02	U5	P_REQ64#/ N/C	AA4	V_{SS}
N29	SA01	U28	SDQM3	AA5	P_AD57/ N/C
N30	SA00	U29	SDQM6	AA28	DQ52
N31	V_{CC}	U30	SDQM2	AA29	DQ20
N32	SRAS#	U31	V_{CC}	AA30	DQ51
P1	P_AD10	U32	SCKE1	AA31	V_{CC}
P2	V_{CC}	V1	N/C	AA32	DQ19
P3	P_AD11	V2	V_{CC}	AB1	P_AD50/ N/C
P4	P_AD12	V3	N/C	AB2	V_{CC}
P5	P_AD13	V4	N/C	AB3	N/C
P28	SA06	V5	N/C	AB4	N/C
P29	V_{SS}	V28	N/C	AB5	N/C
P30	SA05	V29	V_{SS}	AB28	DQ54
P31	SA04	V30	SCB6	AB29	V_{SS}

Table F-1. 540-Lead H-PBGA Pinout — Intel® i960® RM I/O Processor Processor (Sheet 4 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AB30	DQ22	AF29	V_{SS}	AH26	S_AD31
AB31	DQ53	AF30	DQ30	AH27	S_REQ1#
AB32	DQ21	AF31	DQ61	AH28	S_REQ3#
AC1	P_AD46/ N/C	AF32	DQ29	AH29	V_{SS}
AC2	P_AD47/ N/C	AG1	NC1/ N/C	AH30	V_{CC}
AC3	P_AD48/ N/C	AG2	P_AD32/ N/C	AH31	V_{CC}
AC4	V_{SS}	AG3	P_AD33/ N/C	AH32	DQ63
AC5	P_AD49/ N/C	AG4	V_{SS}	AJ1	V_{CC}
AC28	DQ56	AG5	V_{SS}	AJ2	S_AD35/ N/C
AC29	DQ24	AG28	V_{SS}	AJ3	V_{SS}
AC30	DQ55	AG29	V_{SS}	AJ4	V_{SS}
AC31	V_{CC}	AG30	V_{CC}	AJ5	S_AD36/ N/C
AC32	DQ23	AG31	V_{CC}	AJ6	V_{SS}
AD1	P_AD42/ N/C	AG32	DQ31	AJ7	S_AD44/ N/C
AD2	V_{CC}	AH1	S_AD32/ N/C	AJ8	V_{SS}
AD3	P_AD43/ N/C	AH2	V_{CC}	AJ9	S_AD52/ N/C
AD4	P_AD44/ N/C	AH3	S_AD33/ N/C	AJ10	V_{SS}
AD5	P_AD45/ N/C	AH4	S_AD34/ N/C	AJ11	S_AD60/ N/C
AD28	DQ58	AH5	V_{SS}	AJ12	V_{SS}
AD29	V_{SS}	AH6	S_AD39/ N/C	AJ13	S_C/BE7#|| N/C
AD30	DQ26	AH7	S_AD43/ N/C	AJ14	V_{SS}
AD31	DQ57	AH8	S_AD47/ N/C	AJ15	S_AD05
AD32	DQ25	AH9	S_AD51/ N/C	AJ16	V_{SS}
AE1	P_AD38/ N/C	AH10	S_AD55/ N/C	AJ17	S_AD08
AE2	P_AD39/ N/C	AH11	S_AD59/ N/C	AJ18	V_{SS}
AE3	P_AD40/ N/C	AH12	S_AD63/ N/C	AJ19	S_C/BE1#
AE4	V_{SS}	AH13	S_C/BE6#|| N/C	AJ20	V_{SS}
AE5	P_AD41/ N/C	AH14	S_AD00	AJ21	S_IRDY#
AE28	DQ60	AH15	S_AD04	AJ22	V_{SS}
AE29	DQ28	AH16	V_{SS}	AJ23	S_AD21
AE30	DQ59	AH17	S_C/BE0#	AJ24	V_{SS}
AE31	V_{CC}	AH18	S_AD11	AJ25	S_AD28
AE32	DQ27	AH19	S_AD15	AJ26	V_{SS}
AF1	N/C	AH20	S_PERR#	AJ27	S_GNT1#
AF2	V_{CC}	AH21	S_TRDY#	AJ28	V_{SS}
AF3	N/C	AH22	S_AD16	AJ29	S_REQ5#
AF4	N/C	AH23	S_AD20	AJ30	V_{CC}
AF5	N/C	AH24	S_C/BE3#	AJ31	V_{CC}
AF28	DQ62	AH25	S_AD27	AJ32	V_{SS}

Table F-1. 540-Lead H-PBGA Pinout — Intel® i960® RM I/O Processor Processor (Sheet 5 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AK1	V_{SS}	AL1	V_{SS}	AM1	V_{SS}
AK2	V_{CC}	AL2	V_{CC}	AM2	V_{SS}
AK3	V_{CC}	AL3	V_{CC}	AM3	V_{SS}
AK4	V_{SS}	AL4	V_{CC}	AM4	V_{CC}
AK5	S_AD37/ N/C	AL5	V_{CC}	AM5	N/C
AK6	S_AD40/ N/C	AL6	N/C	AM6	N/C
AK7	S_AD45/ N/C	AL7	V_{CC}	AM7	N/C
AK8	S_AD48/ N/C	AL8	N/C	AM8	N/C
AK9	S_AD53/ N/C	AL9	V_{CC}	AM9	N/C
AK10	S_AD56/ N/C	AL10	N/C	AM10	N/C
AK11	S_AD61/ N/C	AL11	V_{CC}	AM11	N/C
AK12	S_PAR64/ N/C	AL12	N/C	AM12	N/C
AK13	S_REQ64#/ N/C	AL13	V_{CC}	AM13	N/C
AK14	S_AD01	AL14	S_AD02	AM14	S_AD03
AK15	S_AD06	AL15	V_{CC}	AM15	S_AD07
AK16	V_{SS}	AL16	N/C	AM16	V_{CC}
AK17	S_AD09	AL17	V_{CC}	AM17	S_AD10
AK18	S_AD12	AL18	S_AD13	AM18	S_AD14
AK19	S_PAR	AL19	V_{CC}	AM19	S_SERR#
AK20	S_LOCK#	AL20	S_STOP#	AM20	S_DEVSEL#
AK21	S_FRAME#	AL21	V_{CC}	AM21	S_C/BE2#
AK22	S_AD17	AL22	S_AD18	AM22	S_AD19
AK23	S_AD22	AL23	V_{CC}	AM23	S_AD23
AK24	S_AD24	AL24	S_AD25	AM24	S_AD26
AK25	S_AD29	AL25	V_{CC}	AM25	S_AD30
AK26	S_RST#	AL26	S_REQ0#	AM26	S_GNT0#
AK27	S_REQ2#	AL27	V_{CC}	AM27	S_GNT2#
AK28	S_GNT3#	AL28	S_REQ4#	AM28	S_GNT4#
AK29	S_GNT5#	AL29	V_{CC}	AM29	V_{SS}
AK30	V_{CC}	AL30	V_{CC}	AM30	V_{SS}
AK31	V_{CC}	AL31	V_{CC}	AM31	V_{SS}
AK32	V_{SS}	AL32	V_{SS}	AM32	V_{SS}

Table F-2 details the ballout for the 80960RN processor.

Table F-2. 540-Lead H-PBGA Pinout — Intel® i960® RN I/O Processor Processor (Sheet 1 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
A1	V_{SS}	B6	V_{CC}	C11	TRST#
A2	V_{SS}	B7	P_RST#	C12	TCK
A3	V_{SS}	B8	V_{CC}	C13	RAD02
A4	V_{SS}	B9	XINT0#	C14	RAD05
A5	V_{SS}	B10	V_{CC}	C15	RAD09
A6	P_AD29	B11	TMS	C16	V_{CC}
A7	P_GNT#	B12	V_{CC}	C17	V_{SS}
A8	SCL	B13	RAD01	C18	RAD13
A9	NMI#	B14	V_{CC}	C19	RCE0#
A10	XINT3#	B15	V_{CCPLL2}	C20	P_CLK
A11	I_RST#	B16	V_{CC}	C21	ONCE#
A12	TDI	B17	V_{CC}	C22	V_{CCPLL1}
A13	RAD00	B18	V_{CC}	C23	DQ02
A14	RAD04	B19	RALE	C24	DQ35
A15	RAD08	B20	V_{CC}	C25	DQ06
A16	N/C	B21	V_{SS}	C26	DQ39
A17	V_{CC}	B22	V_{CC}	C27	DQ41
A18	RAD12	B23	DQ33	C28	DQ11
A19	RAD16	B24	V_{CC}	C29	V_{CC}
A20	RWE#	B25	DQ37	C30	V_{CC}
A21	LCDINIT#	B26	V_{CC}	C31	V_{CC}
A22	DCLKOUT	B27	DQ09	C32	V_{SS}
A23	DQ01	B28	V_{CC}	D1	V_{SS}
A24	DQ03	B29	V_{CC}	D2	V_{CC}
A25	DQ05	B30	V_{CC}	D3	V_{SS}
A26	DQ07	B31	V_{CC}	D4	V_{SS}
A27	DQ40	B32	V_{SS}	D5	V_{SS}
A28	DQ42	C1	V_{SS}	D6	P_AD31
A29	V_{CC}	C2	V_{CC}	D7	V_{SS}
A30	V_{SS}	C3	V_{CC}	D8	P_INTB#
A31	V_{SS}	C4	V_{SS}	D9	V_{SS}
A32	V_{SS}	C5	V_{CC}	D10	XINT5#
B1	V_{SS}	C6	P_AD30	D11	V_{SS}
B2	V_{CC}	C7	P_INTD#	D12	V_{CC}
B3	V_{CC}	C8	SDA	D13	V_{SS}
B4	V_{CC}	C9	XINT1#	D14	RAD06
B5	V_{CC}	C10	XINT4#	D15	V_{SS}

Table F-2. 540-Lead H-PBGA Pinout — Intel® i960® RN I/O Processor Processor (Sheet 2 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
D16	V_{SS}	E23	DQ34	H32	DQ12
D17	V_{SS}	E24	DQ36	J1	P_AD19
D18	RAD14	E25	DQ38	J2	P_AD20
D19	V_{SS}	E26	DQ08	J3	P_AD21
D20	ROE#	E27	DQ10	J4	V_{SS}
D21	V_{SS}	E28	V_{SS}	J5	P_AD22
D22	DQ00	E29	V_{SS}	J28	DQ47
D23	V_{SS}	E30	V_{SS}	J29	DQ15
D24	DQ04	E31	V_{CC}	J30	DQ46
D25	V_{SS}	E32	V_{SS}	J31	V_{CC}
D26	V_{CCPLL3}	F01	V_{SS}	J32	DQ14
D27	V_{SS}	F02	V_{CC}	K1	P_C/BE2#
D28	V_{SS}	F03	V_{CC}	K2	V_{CC}
D29	V_{SS}	F04	V_{CC}	K3	P_AD16
D30	V_{CC}	F05	V_{SS}	K4	P_AD17
D31	V_{CC}	F28	V_{SS}	K5	P_AD18
D32	V_{CC}	F29	V_{SS}	K28	SCB5
E1	V_{SS}	F30	V_{SS}	K29	V_{SS}
E2	V_{CC}	F31	V_{SS}	K30	SCB1
E3	V_{CC}	F32	V_{SS}	K31	SCB4
E4	V_{SS}	G1	P_AD25	K32	SCB0
E5	P_AD28	G2	P_AD26	L1	P_DEVSEL#
E6	P_REQ#	G3	P_AD27	L2	P_TRDY#
E7	P_INTC#	G4	V_{SS}	L3	P_IRDY#
E8	P_INTA#	G5	N/C	L4	V_{SS}
E9	XINT2#	G28	V_{SS}	L5	P_FRAME#
E10	V_{CC}	G29	V_{SS}	L28	SDQM4
E11	TDO	G30	V_{CC}	L29	SDQM0
E12	FAIL#	G31	V_{CC}	L30	SCAS#
E13	RAD03	G32	DQ43	L31	V_{CC}
E14	RAD07	H1	P_AD23	L32	SWE#
E15	RAD10	H2	V_{CC}	M1	P_SERR#
E16	V_{SS}	H3	P_IDSEL	M2	V_{CC}
E17	RAD11	H4	P_C/BE3#	M3	P_PERR#
E18	RAD15	H5	P_AD24	M4	P_LOCK#
E19	RCE1#	H28	DQ45	M5	P_STOP#
E20	V_{CC5REF}	H29	V_{SS}	M28	SCE1#
E21	DCLKIN	H30	DQ13	M29	V_{SS}
E22	DQ32	H31	DQ44	M30	SCE0#

Table F-2. 540-Lead H-PBGA Pinout — Intel® i960® RN I/O Processor Processor (Sheet 3 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
M31	SDQM5	T30	SBA1	Y29	V_{SS}
M32	SDQM1	T31	SBA0	Y30	DQ18
N1	P_AD14	T32	SA11	Y31	DQ49
N2	P_AD15	U1	P_AD00	Y32	DQ17
N3	P_PAR	U2	P_AD01	AA1	P_AD54
N4	V_{SS}	U3	P_AD02	AA2	P_AD55
N5	P_C/BE1#	U4	V_{SS}	AA3	P_AD56
N28	SA02	U5	P_REQ64#	AA4	V_{SS}
N29	SA01	U28	SDQM3	AA5	P_AD57
N30	SA00	U29	SDQM6	AA28	DQ52
N31	V_{CC}	U30	SDQM2	AA29	DQ20
N32	SRAS#	U31	V_{CC}	AA30	DQ51
P1	P_AD10	U32	SCKE1	AA31	V_{CC}
P2	V_{CC}	V1	P_C/BE5#	AA32	DQ19
P3	P_AD11	V2	V_{CC}	AB1	P_AD50
P4	P_AD12	V3	P_C/BE6#	AB2	V_{CC}
P5	P_AD13	V4	P_C/BE7#	AB3	P_AD51
P28	SA06	V5	P_ACK64#	AB4	P_AD52
P29	V_{SS}	V28	N/C	AB5	P_AD53
P30	SA05	V29	V_{SS}	AB28	DQ54
P31	SA04	V30	SCB6	AB29	V_{SS}
P32	SA03	V31	SCB2	AB30	DQ22
R1	P_AD07	V32	SDQM7	AB31	DQ53
R2	P_C/BE0#	W1	P_AD62	AB32	DQ21
R3	P_AD08	W2	P_AD63	AC1	P_AD46
R4	V_{SS}	W3	P_PAR64	AC2	P_AD47
R5	P_AD09	W4	V_{SS}	AC3	P_AD48
R28	SA10	W5	P_C/BE4#	AC4	V_{SS}
R29	SA09	W28	DQ48	AC5	P_AD49
R30	SA08	W29	DQ16	AC28	DQ56
R31	V_{CC}	W30	SCB7	AC29	DQ24
R32	SA07	W31	V_{CC}	AC30	DQ55
T1	P_AD03	W32	SCB3	AC31	V_{CC}
T2	V_{CC}	Y1	P_AD58	AC32	DQ23
T3	P_AD04	Y2	V_{CC}	AD1	P_AD42
T4	P_AD05	Y3	P_AD59	AD2	V_{CC}
T5	P_AD06	Y4	P_AD60	AD3	P_AD43
T28	SCKE0	Y5	P_AD61	AD4	P_AD44
T29	V_{SS}	Y28	DQ50	AD5	P_AD45

Table F-2. 540-Lead H-PBGA Pinout — Intel® i960® RN I/O Processor Processor (Sheet 4 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AD28	DQ58	AH5	V_{SS}	AJ12	V_{SS}
AD29	V_{SS}	AH6	S_AD39	AJ13	S_C/BE7#
AD30	DQ26	AH7	S_AD43	AJ14	V_{SS}
AD31	DQ57	AH8	S_AD47	AJ15	S_AD05
AD32	DQ25	AH9	S_AD51	AJ16	V_{SS}
AE1	P_AD38	AH10	S_AD55	AJ17	S_AD08
AE2	P_AD39	AH11	S_AD59	AJ18	V_{SS}
AE3	P_AD40	AH12	S_AD63	AJ19	S_C/BE1#
AE4	V_{SS}	AH13	S_C/BE6#	AJ20	V_{SS}
AE5	P_AD41	AH14	S_AD00	AJ21	S_IRDY#
AE28	DQ60	AH15	S_AD04	AJ22	V_{SS}
AE29	DQ28	AH16	V_{SS}	AJ23	S_AD21
AE30	DQ59	AH17	S_C/BE0#	AJ24	V_{SS}
AE31	V_{CC}	AH18	S_AD11	AJ25	S_AD28
AE32	DQ27	AH19	S_AD15	AJ26	V_{SS}
AF1	P_AD34	AH20	S_PERR#	AJ27	S_GNT1#
AF2	V_{CC}	AH21	S_TRDY#	AJ28	V_{SS}
AF3	P_AD35	AH22	S_AD16	AJ29	S_REQ5#
AF4	P_AD36	AH23	S_AD20	AJ30	V_{CC}
AF5	P_AD37	AH24	S_C/BE3#	AJ31	V_{CC}
AF28	DQ62	AH25	S_AD27	AJ32	V_{SS}
AF29	V_{SS}	AH26	S_AD31	AK1	V_{SS}
AF30	DQ30	AH27	S_REQ1#	AK2	V_{CC}
AF31	DQ61	AH28	S_REQ3#	AK3	V_{CC}
AF32	DQ29	AH29	V_{SS}	AK4	V_{SS}
AG1	N/C	AH30	V_{CC}	AK5	S_AD37
AG2	P_AD32	AH31	V_{CC}	AK6	S_AD40
AG3	P_AD33	AH32	DQ63	AK7	S_AD45
AG4	V_{SS}	AJ1	V_{CC}	AK8	S_AD48
AG5	V_{SS}	AJ2	S_AD35	AK9	S_AD53
AG28	V_{SS}	AJ3	V_{SS}	AK10	S_AD56
AG29	V_{SS}	AJ4	V_{SS}	AK11	S_AD61
AG30	V_{CC}	AJ5	S_AD36	AK12	S_PAR64
AG31	V_{CC}	AJ6	V_{SS}	AK13	S_REQ64#
AG32	DQ31	AJ7	S_AD44	AK14	S_AD01
AH1	S_AD32	AJ8	V_{SS}	AK15	S_AD06
AH2	V_{CC}	AJ9	S_AD52	AK16	V_{SS}
AH3	S_AD33	AJ10	V_{SS}	AK17	S_AD09
AH4	S_AD34	AJ11	S_AD60	AK18	S_AD12

Table F-2. 540-Lead H-PBGA Pinout — Intel® i960® RN I/O Processor Processor (Sheet 5 of 5)

Ball #	Signal	Ball #	Signal	Ball #	Signal
AK19	S_PAR	AL13	V_{CC}	AM7	S_AD46
AK20	S_LOCK#	AL14	S_AD02	AM8	S_AD50
AK21	S_FRAME#	AL15	V_{CC}	AM9	S_AD54
AK22	S_AD17	AL16	N/C	AM10	S_AD58
AK23	S_AD22	AL17	V_{CC}	AM11	S_AD62
AK24	S_AD24	AL18	S_AD13	AM12	S_C/BE5#
AK25	S_AD29	AL19	V_{CC}	AM13	S_ACK64#
AK26	S_RST#	AL20	S_STOP#	AM14	S_AD03
AK27	S_REQ2#	AL21	V_{CC}	AM15	S_AD07
AK28	S_GNT3#	AL22	S_AD18	AM16	V_{CC}
AK29	S_GNT5#	AL23	V_{CC}	AM17	S_AD10
AK30	V_{CC}	AL24	S_AD25	AM18	S_AD14
AK31	V_{CC}	AL25	V_{CC}	AM19	S_SERR#
AK32	V_{SS}	AL26	S_REQ0#	AM20	S_DEVSEL#
AL1	V_{SS}	AL27	V_{CC}	AM21	S_C/BE2#
AL2	V_{CC}	AL28	S_REQ4#	AM22	S_AD19
AL3	V_{CC}	AL29	V_{CC}	AM23	S_AD23
AL4	V_{CC}	AL30	V_{CC}	AM24	S_AD26
AL5	V_{CC}	AL31	V_{CC}	AM25	S_AD30
AL6	S_AD41	AL32	V_{SS}	AM26	S_GNT0#
AL7	V_{CC}	AM1	V_{SS}	AM27	S_GNT2#
AL8	S_AD49	AM2	V_{SS}	AM28	S_GNT4#
AL9	V_{CC}	AM3	V_{SS}	AM29	V_{SS}
AL10	S_AD57	AM4	V_{CC}	AM30	V_{SS}
AL11	V_{CC}	AM5	S_AD38	AM31	V_{SS}
AL12	S_C/BE4#	AM6	S_AD42	AM32	V_{SS}