

119-, 165- & 209-Pin BGA 1M x 18, 512K x 36, 256K x 72 250 MHz–133MHz
Commercial Temp 2.5 V or 3.3 V V_{DD}
Industrial Temp 18Mb S/DCD Sync Burst SRAMs 2.5 V or 3.3 V I/O

Features

- FT pin for user-configurable flow through or pipeline operation
- Single/Dual Cycle Deselect selectable
- IEEE 1149.1 JTAG-compatible Boundary Scan
- ZQ mode pin for user-selectable high/low output drive
- 2.5 V or 3.3 V +10%/–10% core power supply
- LBO pin for Linear or Interleaved Burst mode
- Internal input resistors on mode pins allow floating mode pins
- Default to SCD x18/x36 Interleaved Pipeline mode
- Byte Write (BW) and/or Global Write (GW) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 119-, 165-, and 209-bump BGA package

		-250	-225	-200	-166	-150	-133	Unit
Pipeline 3-1-1-1	t _{KQ}	2.5	2.7	3.0	3.4	3.8	4.0	ns
	t _{Cycle}	4.0	4.4	5.0	6.0	6.7	7.5	ns
3.3 V	Curr (x18)	280	255	230	200	185	165	mA
	Curr (x36)	330	300	270	230	215	190	mA
	Curr (x72)	430	395	350	300	270	245	mA
2.5 V	Curr (x18)	275	250	230	195	180	165	mA
	Curr (x36)	320	295	265	225	210	185	mA
	Curr (x72)	410	380	335	290	260	235	mA
Flow Through 2-1-1-1	t _{KQ}	5.5	6.0	6.5	7.0	7.5	8.5	ns
	t _{Cycle}	5.5	6.0	6.5	7.0	7.5	8.5	ns
3.3 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x36)	200	190	180	170	165	150	mA
	Curr (x72)	255	240	225	115	210	185	mA
2.5 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x36)	200	190	180	170	165	150	mA
	Curr (x72)	255	240	225	115	210	185	mA

Functional Description

Applications

The GS816218(B/D)/GS816236(B/D)/GS816272(C) is an 18,874,368-bit high performance synchronous SRAM with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enable ($\overline{E1}$), address burst control inputs (ADSP, ADSC, ADV), and write control inputs (Bx, BW, GW) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (G) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either ADSP or ADSC inputs. In Burst mode, subsequent

burst addresses are generated internally and are controlled by ADV. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order (LBO) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the FT mode. Holding the FT mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding FT high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

SCD and DCD Pipelined Reads

The GS816218(B/D)/GS816236(B/D)/GS816272(C) is a SCD (Single Cycle Deselect) and DCD (Dual Cycle Deselect) pipelined synchronous SRAM. DCD SRAMs pipeline disable commands to the same degree as read commands. SCD SRAMs pipeline deselect commands one stage less than read commands. SCD RAMs begin turning off their outputs immediately after the deselect command has been captured in the input registers. DCD RAMs hold the deselect command for one full cycle and then begin turning off their outputs just after the second rising edge of clock. The user may configure this SRAM for either mode of operation using the SCD mode input.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (BW) input combined with one or more individual byte write signals (Bx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

FLXDrive™

The ZQ pin allows selection between high drive strength (ZQ low) for multi-drop bus applications and normal drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS816218(B/D)/GS816236(B/D)/GS816272(C) operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

GS816272 Pad Out

209 Bump BGA—Top View Package C

	1	2	3	4	5	6	7	8	9	10	11
A	DQG5	DQG1	A15	E2	ADSP	ADSC	ADV	E3	A17	DQB1	DQB5
B	DQG6	DQG2	BC	BG	NC	BW	A16	BB	BF	DQB2	DQB6
C	DQG7	DQG3	BH	BD	NC	E1	NC	BE	BA	DQB3	DQB7
D	DQG8	DQG4	VSS	NC	NC	G	GW	NC	VSS	DQB4	DQB8
E	DQG9	DQC9	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQF9	DQB9
F	DQC4	DQC8	VSS	VSS	VSS	ZQ	VSS	VSS	VSS	DQF8	DQF4
G	DQC3	DQC7	VDDQ	VDDQ	VDD	MCH	VDD	VDDQ	VDDQ	DQF7	DQF3
H	DQC2	DQC6	VSS	VSS	VSS	MCL	VSS	VSS	VSS	DQF6	DQF2
J	DQC1	DQC5	VDDQ	VDDQ	VDD	MCL	VDD	VDDQ	VDDQ	DQF5	DQF1
K	NC	NC	CK	NC	VSS	MCL	VSS	NC	NC	NC	NC
L	DQH1	DQH5	VDDQ	VDDQ	VDD	FT	VDD	VDDQ	VDDQ	DQA5	DQA1
M	DQH2	DQH6	VSS	VSS	VSS	MCL	VSS	VSS	VSS	DQA6	DQA2
N	DQH3	DQH7	VDDQ	VDDQ	VDD	SCD	VDD	VDDQ	VDDQ	DQA7	DQA3
P	DQH4	DQH8	VSS	VSS	VSS	ZZ	VSS	VSS	VSS	DQA8	DQA4
R	DQD9	DQH9	VDDQ	VDDQ	VDD	VDD	VDD	VDDQ	VDDQ	DQA9	DQE9
T	DQD8	DQD4	VSS	NC	NC	LBO	PE	NC	VSS	DQE4	DQE8
U	DQD7	DQD3	NC	A14	A13	A12	A11	A10	NC	DQE3	DQE7
V	DQD6	DQD2	A9	A8	A7	A1	A6	A5	A4	DQE2	DQE6
W	DQD5	DQD1	TMS	TDI	A3	A0	A2	TDO	TCK	DQE1	DQE5

Rev 10

11 x 19 Bump BGA—14 x 22 mm² Body—1 mm Bump Pitch

GS816272 BGA Pin Description

Pin Location	Symbol	Type	Description
W6, V6	A ₀ , A ₁	I	Address field LSBs and Address Counter Preset Inputs.
W7, W5, V9, V8, V7, V5, V4, V3, U8, U7, U6, U5, U4, A3, B7, A9	A _n	I	Address Inputs
L11, M11, N11, P11, L10, M10, N10, P10, R10 A10, B10, C10, D10, A11, B11, C11, D11, E11 J1, H1, G1, F1, J2, H2, G2, F2, E2 W2, V2, U2, T2, W1, V1, U1, T1, R1 W10, V10, U10, T10, W11, V11, U11, T11, R11 J11, H11, G11, F11, J10, H10, G10, F10, E10 A2, B2, C2, D2, A1, B1, C1, D1, E1 L1, M1, N1, P1, L2, M2, N2, P2, R2	DQ _{A1} –DQ _{A9} DQ _{B1} –DQ _{B9} DQ _{C1} –DQ _{C9} DQ _{D1} –DQ _{D9} DQ _{E1} –DQ _{E9} DQ _{F1} –DQ _{F9} DQ _{G1} –DQ _{G9} DQ _{H1} –DQ _{H9}	I/O	Data Input and Output pins (x36 Version)
C9, B8, B3, C4, C8, B9, B4, C3	$\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$, $\overline{B_E}$, $\overline{B_F}$, $\overline{B_G}$, $\overline{B_H}$	I	Byte Write Enable for DQ _A , DQ _B , DQ _C , DQ _D , DQ _E , DQ _F , DQ _G , DQ _H I/Os; active low
B5, C5, C7, D4, D5, D8, K1, K2, K4, K8, K9, K10, K11, T4, T5, T8, U3, U9	NC	—	No Connect
K3	CK	I	Clock Input Signal; active high
D7	$\overline{GW}$	I	Global Write Enable—Writes all bytes; active low
C6, A8	$\overline{E_1}$, $\overline{E_3}$	I	Chip Enable; active low
A4	E ₂	I	Chip Enable; active high
D6	$\overline{G}$	I	Output Enable; active low
A7	$\overline{ADV}$	I	Burst address counter advance enable; active low
A5, A6	$\overline{ADSP}$, $\overline{ADSC}$	I	Address Strobe (Processor, Cache Controller); active low
P6	ZZ	I	Sleep Mode control; active high
L6	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
T6	$\overline{LBO}$	I	Linear Burst Order mode; active low
N6	SCD	I	Single Cycle Deselect/Dual Cycle Deselect Mode Control
G6	MCH	I	Must Connect High
H6, J6, K6, M6	MCL		Must Connect Low

GS816272 BGA Pin Description

Pin Location	Symbol	Type	Description
T7	$\overline{\text{PE}}$	I	Parity Bit Enable; active low (High = x16/32 Mode, Low = x18/36 Mode)
B6	$\overline{\text{BW}}$	I	Byte Enable; active low
F6	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
W3	TMS	I	Scan Test Mode Select
W4	TDI	I	Scan Test Data In
W8	TDO	O	Scan Test Data Out
W9	TCK	I	Scan Test Clock
E5, E6, E7, G5, G7, J5, J7, L5, L7, N5, N7, R5, R6, R7	V_{DD}	I	Core power supply
D3, D9, F3, F4, F5, F7, F8, F9, H3, H4, H5, H7, H8, H9, K5, K7, M3, M4, M5, M7, M8, M9, P3, P4, P5, P7, P8, P9, T3, T9	V_{SS}	I	I/O and Core Ground
E3, E4, E8, E9, G3, G4, G8, G9, J3, J4, J8, J9, L3, L4, L8, L9, N3, N4, N8, N9, R3, R4, R8, R9	V_{DDQ}	I	Output driver power supply

165 Bump BGA—x18 Commom I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	E1	BB	NC	E3	BW	ADSC	ADV	A	A19	A
B	NC	A	E2	NC	BA	CK	GW	G	ADSP	A	NC	B
C	NC	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQPA	C
D	NC	DQB	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQA	D
E	NC	DQB	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQA	E
F	NC	DQB	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQA	F
G	NC	DQB	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	NC	DQA	G
H	FT	MCL	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	ZQ	ZZ	H
J	DQB	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	NC	J
K	DQB	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	NC	K
L	DQB	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	NC	L
M	DQB	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	NC	M
N	DQPB	SCD	V _{DDQ}	V _{SS}	NC	A18	NC	V _{SS}	V _{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A17	P
R	LBO	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13mm x 15 mm Body—1.0 mm Bump Pitch

165 Bump BGA—x36 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	E1	BC	BB	E3	BW	ADSC	ADV	A	NC	A
B	NC	A	E2	BD	BA	CK	GW	G	ADSP	A	NC	B
C	DQPC	NC	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	DQPB	C
D	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	D
E	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	E
F	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	F
G	DQC	DQC	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQB	DQB	G
H	FT	MCL	NC	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	NC	ZQ	ZZ	H
J	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	J
K	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	K
L	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	L
M	DQD	DQD	V _{DDQ}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DDQ}	DQA	DQA	M
N	DQPD	SCD	V _{DDQ}	V _{SS}	NC	A18	NC	V _{SS}	V _{DDQ}	NC	DQPA	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	A17	P
R	LBO	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13mm x 15 mm Body—1.0 mm Bump Pitch

GS816218/36 165-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
R6, P6	A0, A1	I	Address field LSBs and Address Counter Preset Inputs
A2, A10, B2, B10, P3, P4, P8, P9, P10, R3, R4, R8, R9, R10, R11	An	I	Address Inputs
P11, N6	A17, A18		Address Input
A11	A19	I	Address Input (x18 Version)
J10, K10, L10, M10, J11, K11, L11, M11, N11 G10, F10, E10, D10, G11, F11, E11, D11, C11 G2, F2, E2, D2, G1, F1, E1, D1, C1 J2, K2, L2, M2, J1, K1, L1, M1, N1	DQA1–DQA9 DQB1–DQB9 DQC1–DQC9 DQD1–DQD9	I/O	Data Input and Output pins. (x36 Version)
B5, A5, A4, B4	BA, BB, BC, BD	I	Byte Write Enable for DQA, DQB, DQC, DQD I/Os; active low (x36 Version)
M10, L10, K10, J10, G11, F11, E11, D11, C11 D2, E2, F2, G2, J1, K1, L1, M1, N1	DQA1–DQA9 DQC1–DQC9	I/O	Data Input and Output pins (x18 Version)
B5, A4	BA, BC	I	Byte Write Enable for DQA, DQB I/Os; active low (x18 Version)
A1, B1, B11, C2, C10, H3, H9, N5, N7, N10, P1, P2, R2	NC	—	No Connect
A5, B4, C1, D1, D10, E1, E10, F1, F10, G1, G10, J2, J11, K2, K11, L2, L11, M2, M11, N11	NC	—	No Connect (x18 Version)
A11	NC	—	No Connect (x36 Version)
B6	CK	I	Clock Input Signal; active high
A7	BW	I	Byte Write—Writes all enabled bytes; active low
B7	GW	I	Global Write Enable—Writes all bytes; active low
A3	E1	I	Chip Enable; active low
A6	E3	I	Chip Enable; active low (x36 version)
B3	E2	I	Chip Enable; active high (x36 version)
B8	G	I	Output Enable; active low
A9	ADV	I	Burst address counter advance enable; active low
A8, B9	ADSC, ADSP	I	Address Strobe (Processor, Cache Controller); active low
H11	ZZ	I	Sleep mode control; active high
H1	FT	I	Flow Through or Pipeline mode; active low
R1	LBO	I	Linear Burst Order mode; active low
H10	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
R5	TMS	I	Scan Test Mode Select
P5	TDI	I	Scan Test Data In

GS816218/36 165-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
P7	TDO	O	Scan Test Data Out
R7	TCK	I	Scan Test Clock
H2	MCL	—	Must Connect Low
N2	SCD	—	Single Cycle Deselect/Dual Cycle Deselect Mode Control
D4, D8, E4, E8, F4, F8, G4, G8, H4, H8, J4, J8, K4, K8, L4, L8, M4, M8	V _{DD}	I	Core power supply
C4, C5, C6, C7, C8, D5, D6, D7, E5, E6, E7, F5, F6, F7, G5, G6, G7, H5, H6, H7, J5, J6, J7, K5, K6, K7, L5, L6, L7, M5, M6, M7, N4, N8	V _{SS}	I	I/O and Core Ground
C3, C9, D3, D9, E3, E9, F3, F9, G3, G9, J3, J9, K3, K9, L3, L9, M3, M9, N3, N9	V _{DDQ}	I	Output driver power supply

GS816236 Pad Out

**119-Bump BGA—Top View
Package B**

	1	2	3	4	5	6	7
A	V _{DDQ}	A6	A7	$\overline{\text{ADSP}}$	A8	A9	V _{DDQ}
B	NC	A18	A4	$\overline{\text{ADSC}}$	A15	A17	NC
C	NC	A5	A3	V _{DD}	A14	A16	NC
D	DQC4	DQC9	V _{SS}	ZQ	V _{SS}	DQB9	DQB4
E	DQC3	DQC8	V _{SS}	$\overline{\text{E1}}$	V _{SS}	DQB8	DQB3
F	V _{DDQ}	DQC7	V _{SS}	$\overline{\text{G}}$	V _{SS}	DQB7	V _{DDQ}
G	DQC2	DQC6	$\overline{\text{Bc}}$	$\overline{\text{ADV}}$	$\overline{\text{Bb}}$	DQB6	DQB2
H	DQC1	DQC5	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQB5	DQB1
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQD1	DQD5	V _{SS}	CK	V _{SS}	DQA5	DQA1
L	DQD2	DQD6	$\overline{\text{Bd}}$	SCD	$\overline{\text{Ba}}$	DQA6	DQA2
M	V _{DDQ}	DQD7	V _{SS}	$\overline{\text{BW}}$	V _{SS}	DQA7	V _{DDQ}
N	DQD3	DQD8	V _{SS}	A1	V _{SS}	DQA8	DQA3
P	DQD4	DQD9	V _{SS}	A0	V _{SS}	DQA9	DQA4
R	NC	A2	$\overline{\text{LBO}}$	V _{DD}	$\overline{\text{FT}}$	A13	$\overline{\text{PE}}$
T	NC	NC	A10	A11	A12	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

GS816218 Pad Out

119-Bump BGA—Top View Package B

	1	2	3	4	5	6	7
A	V _{DDQ}	A6	A7	$\overline{\text{ADSP}}$	A8	A9	V _{DDQ}
B	NC	A18	A4	$\overline{\text{ADSC}}$	A15	A17	NC
C	NC	A5	A3	V _{DD}	A14	A16	NC
D	DQB1	NC	V _{SS}	ZQ	V _{SS}	DQA9	NC
E	NC	DQB2	V _{SS}	$\overline{\text{E1}}$	V _{SS}	NC	DQA8
F	V _{DDQ}	NC	V _{SS}	$\overline{\text{G}}$	V _{SS}	DQA7	V _{DDQ}
G	NC	DQB3	$\overline{\text{BB}}$	$\overline{\text{ADV}}$	NC	NC	DQA6
H	DQB4	NC	V _{SS}	$\overline{\text{GW}}$	V _{SS}	DQA5	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQB5	V _{SS}	CK	V _{SS}	NC	DQA4
L	DQB6	NC	NC	SCD	$\overline{\text{BA}}$	DQA3	NC
M	V _{DDQ}	DQB7	V _{SS}	$\overline{\text{BW}}$	V _{SS}	NC	V _{DDQ}
N	DQB8	NC	V _{SS}	A1	V _{SS}	DQA2	NC
P	NC	DQB9	V _{SS}	A0	V _{SS}	NC	DQA1
R	NC	A2	$\overline{\text{LBO}}$	V _{DD}	$\overline{\text{FT}}$	A13	$\overline{\text{PE}}$
T	NC	A10	A11	NC	A12	A19	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

BPR1999.05.18

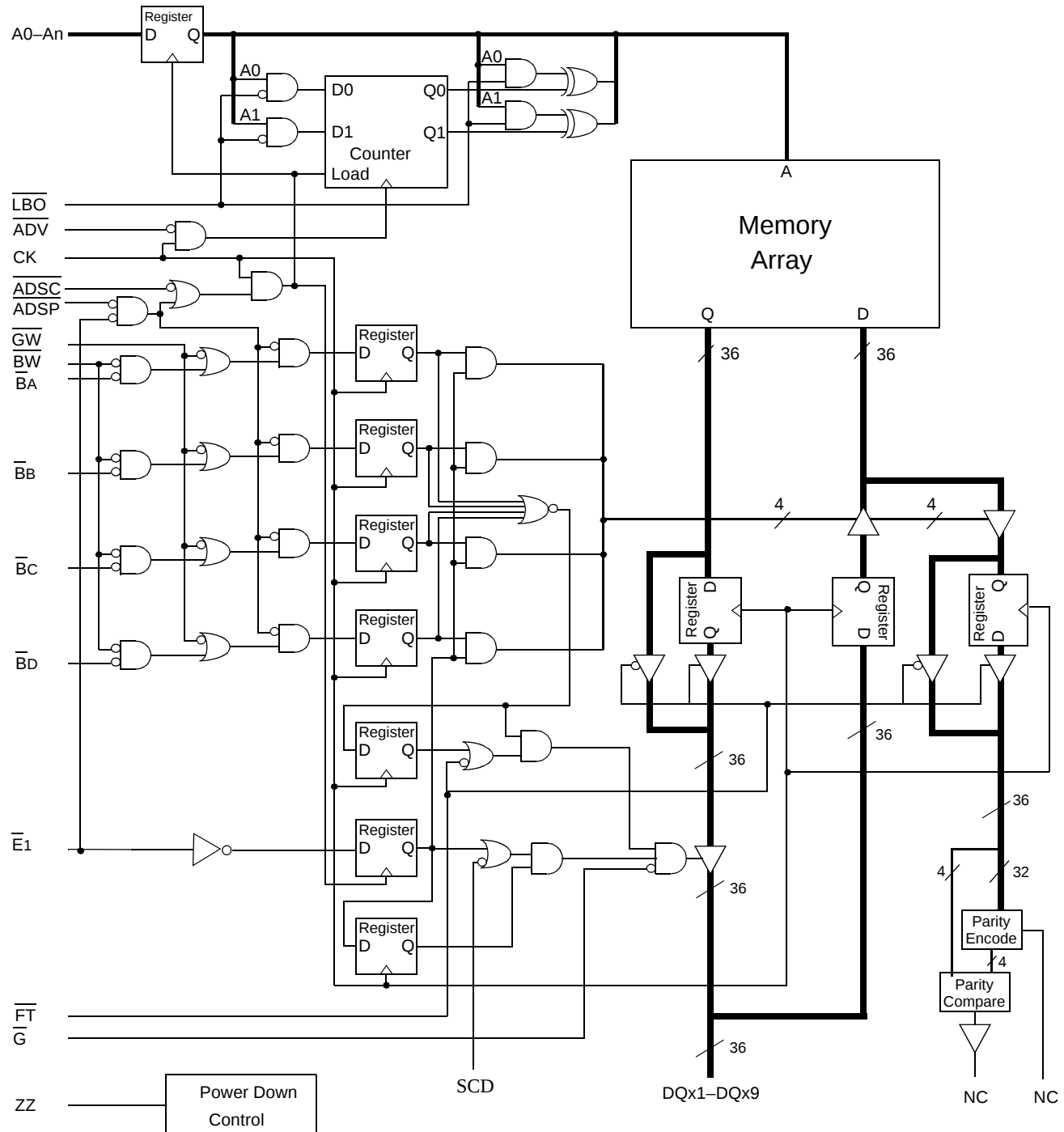
GS816218/36 BGA Pin Description

Pin Location	Symbol	Type	Description
P4, N4	A0, A1	I	Address field LSBs and Address Counter Preset Inputs
R2, C3, B3, C2, A2, A3, A5, A6, T3, T5, R6, C5, B5, C6, B6, B2	An	I	Address Inputs
T4	An		Address Input (x36 Version)
T2, T6	NC	—	No Connect (x36 Version)
T2, T6	An	I	Address Input (x18 Version)
K7, L7, N7, P7, K6, L6, M6, N6 H7, G7, E7, D7, H6, G6, F6, E6 H1, G1, E1, D1, H2, G2, F2, E2 K1, L1, N1, P1, K2, L2, M2, N2	DQA1–DQA8 DQB1–DQB8 DQC1–DQC8 DQD1–DQD8	I/O	Data Input and Output pins. (x36 Version)
P6, D6, D2, P2	DQA9, DQB9, DQC9, DQD9	I/O	Data Input and Output pins. (x36 Version)
L5, G5, G3, L3	BA, BB, BC, BD	I	Byte Write Enable for DQA, DQB, DQC, DQD I/Os; active low (x36 Version)
P7, N6, L6, K7, H6, G7, F6, E7, D6 D1, E2, G2, H1, K2, L1, M2, N1, P2	DQA1–DQA9 DQB1–DQB9	I/O	Data Input and Output pins (x18 Version)
L5, G3	BA, BB	I	Byte Write Enable for DQA, DQB I/Os; active low (x18 Version)
B1, C1, R1, T1, U6, B7, C7, R7, J5	NC	—	No Connect
P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3, T4, J3	NC	—	No Connect (x18 Version)
K4	CK	I	Clock Input Signal; active high
M4	BW	I	Byte Write—Writes all enabled bytes; active low
H4	GW	I	Global Write Enable—Writes all bytes; active low
E4	E ₁	I	Chip Enable; active low
F4	G	I	Output Enable; active low
G4	ADV	I	Burst address counter advance enable; active low
A4, B4	ADSP, ADSC	I	Address Strobe (Processor, Cache Controller); active low
T7	ZZ	I	Sleep mode control; active high
R5	FT	I	Flow Through or Pipeline mode; active low
R3	LBO	I	Linear Burst Order mode; active low
D4	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
L4	SCD	I	Single Cycle Deselect/Dual Cycle Deselect Mode Control
U2	TMS	I	Scan Test Mode Select

GS816218/36 BGA Pin Description

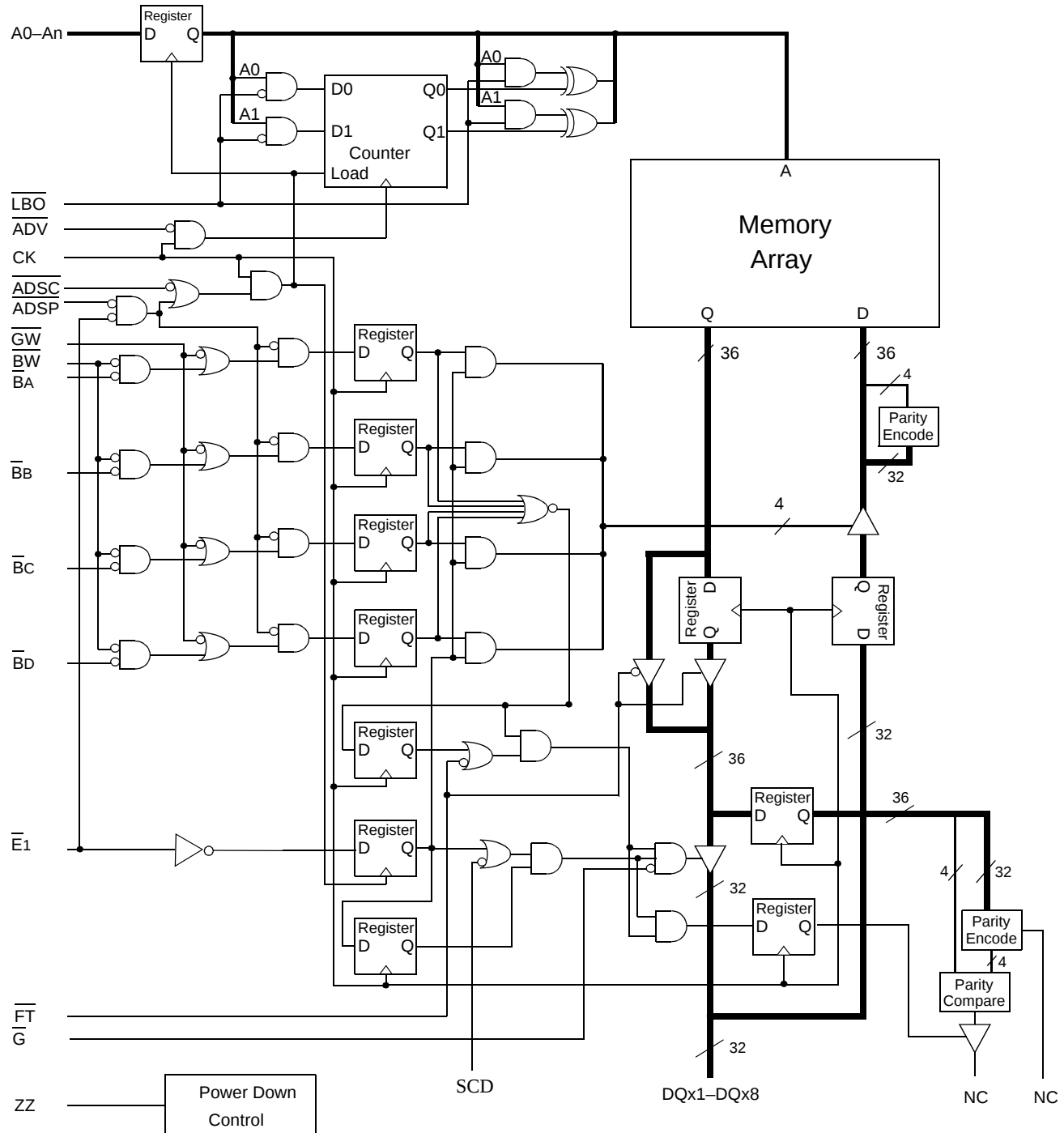
Pin Location	Symbol	Type	Description
U3	TDI	I	Scan Test Data In
U5	TDO	O	Scan Test Data Out
U4	TCK	I	Scan Test Clock
R7	PE	I	Parity Bit Enable; active low
J2, C4, J4, R4, J6	V _{DD}	I	Core power supply
D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5	V _{SS}	I	I/O and Core Ground
A1, F1, J1, M1, U1, A7, F7, J7, M7, U7	V _{DDQ}	I	Output driver power supply

GS816218/36 ($\overline{\text{PE}} = 0$) Block Diagram



Note: Only x36 version shown for simplicity.

GS816218/36 ($\overline{PE} = 1$) x32 Mode Block Diagram



Note: Only x36 version shown for simplicity.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{\text{LBO}}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{\text{FT}}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Single/Dual Cycle Deselect Control	SCD	L	Dual Cycle Deselect
		H or NC	Single Cycle Deselect
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H or NC	Low Drive (High Impedance)

Note:

There are pull-up devices on the ZQ, SCD, and $\overline{\text{FT}}$ pins and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Enable / Disable Parity I/O Pins

This SRAM allows the user to configure the device to operate in Parity I/O active (x18, x36, or x72) or in Parity I/O inactive (x16, x32, or x64) mode. Holding the $\overline{\text{PE}}$ bump low or letting it float will activate the 9th I/O on each byte of the RAM. Grounding PE deactivates the 9th I/O of each byte.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{BA}$	$\overline{BB}$	$\overline{BC}$	$\overline{BD}$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:

1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{BA}$, $\overline{BB}$, $\overline{BC}$, and/or $\overline{BD}$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x36 version.

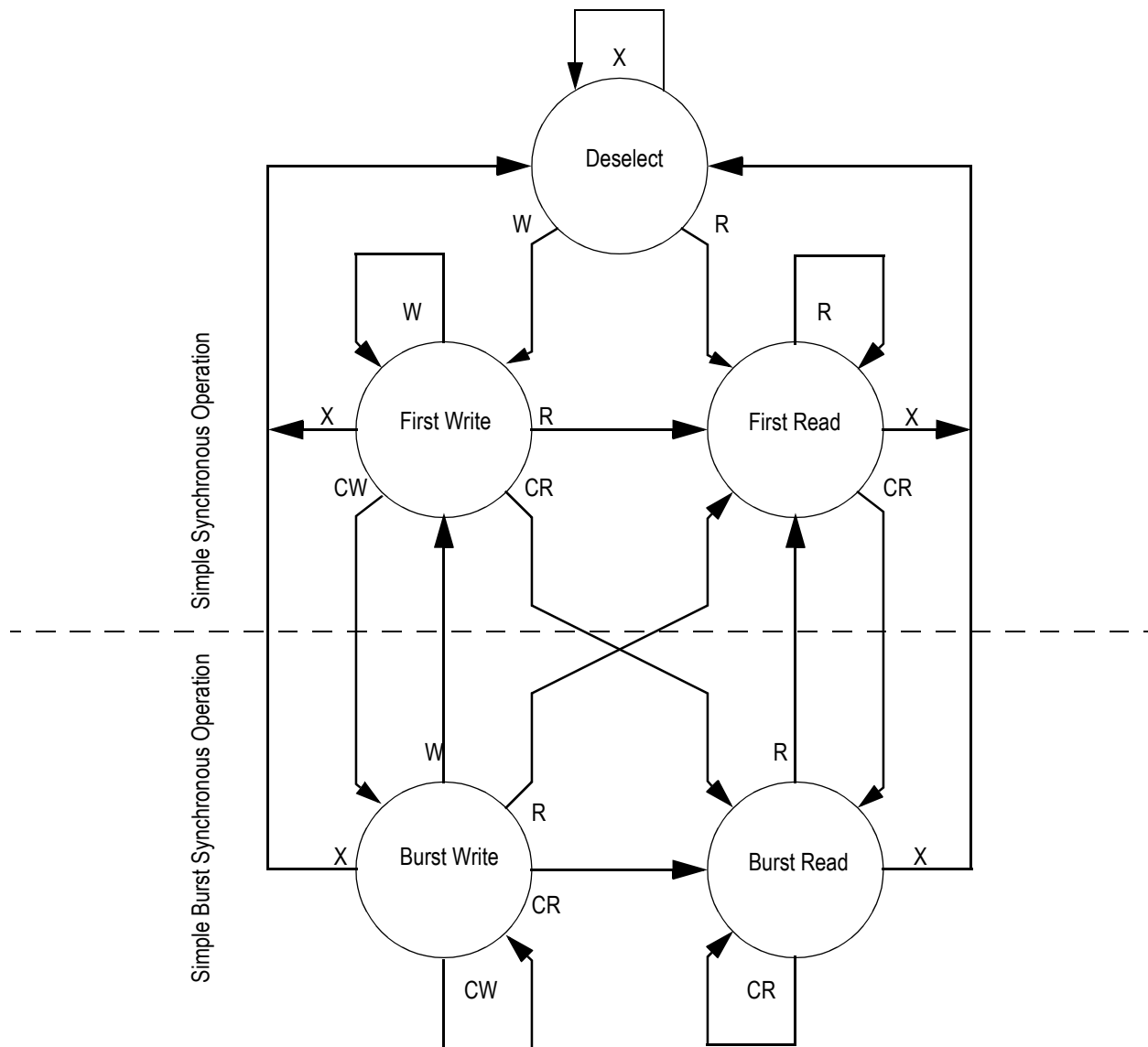
Synchronous Truth Table

Operation	Address Used	State Diagram Key ⁵	$\bar{E}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\bar{W}^3$	DQ ⁴
Deselect Cycle, Power Down	None	X	H	X	L	X	X	High-Z
Read Cycle, Begin Burst	External	R	L	L	X	X	X	Q
Read Cycle, Begin Burst	External	R	L	H	L	X	F	Q
Write Cycle, Begin Burst	External	W	L	H	L	X	T	D
<i>Read Cycle, Continue Burst</i>	<i>Next</i>	<i>CR</i>	X	H	H	L	F	Q
Read Cycle, Continue Burst	Next	CR	H	X	H	L	F	Q
<i>Write Cycle, Continue Burst</i>	<i>Next</i>	<i>CW</i>	X	H	H	L	T	D
Write Cycle, Continue Burst	Next	CW	H	X	H	L	T	D
Read Cycle, Suspend Burst	Current		X	H	H	H	F	Q
Read Cycle, Suspend Burst	Current		H	X	H	H	F	Q
Write Cycle, Suspend Burst	Current		X	H	H	H	T	D
Write Cycle, Suspend Burst	Current		H	X	H	H	T	D

Notes:

1. X = Don't Care, H = High, L = Low
2. $\bar{W}$ = T (True) and F (False) is defined in the Byte Write Truth Table preceding
3. $\bar{G}$ is an asynchronous input. $\bar{G}$ can be driven high at any time to disable active output drivers. $\bar{G}$ low can only enable active drivers (shown as "Q" in the Truth Table above).
4. All input combinations shown above are tested and supported. Input combinations shown in gray boxes need not be used to accomplish basic synchronous or synchronous burst operations and may be avoided for simplicity.
5. Tying $\overline{ADSP}$ high and $\overline{ADSC}$ low allows simple non-burst synchronous operations. See **BOLD** items above.
6. Tying $\overline{ADSP}$ high and $\overline{ADV}$ low while using $\overline{ADSC}$ to load new addresses allows simple burst operations. See *ITALIC* items above.

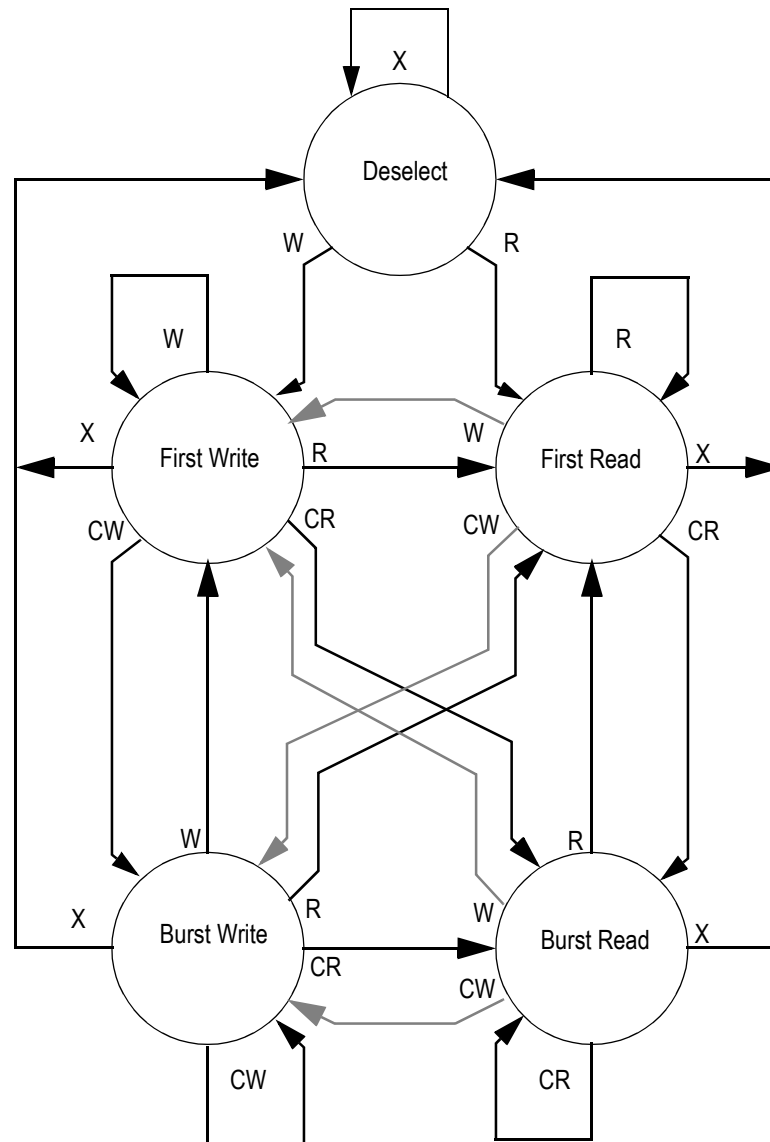
Simplified State Diagram



Notes:

1. The diagram shows only supported (tested) synchronous state transitions. The diagram presumes $\overline{G}$ is tied low.
2. The upper portion of the diagram assumes active use of only the Enable (E1) and Write (BA, BB, BC, BD, BW, and GW) control inputs, and that ADSP is tied high and ADSC is tied low.
3. The upper and lower portions of the diagram together assume active use of only the Enable, Write, and $\overline{ADSC}$ control inputs and assumes ADSP is tied high and ADV is tied low.

Simplified State Diagram with $\overline{G}$



Notes:

1. The diagram shows supported (tested) synchronous state transitions plus supported transitions that depend upon the use of $\overline{G}$.
2. Use of "Dummy Reads" (Read Cycles with $\overline{G}$ High) may be used to make the transition from read cycles to write cycles without passing through a Deselect cycle. Dummy Read cycles increment the address counter just like normal read cycles.
3. Transitions shown in grey tone assume $\overline{G}$ has been pulsed high long enough to turn the RAM's drivers off and for incoming data to meet Data Input Set Up Time.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	−0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	−0.5 to 4.6	V
V_{CK}	Voltage on Clock Input Pin	−0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	−0.5 to $V_{DDQ} + 0.5$ (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	−0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/−20	mA
I_{OUT}	Output Current on Any I/O Pin	+/−20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	−55 to 125	°C
T_{BIAS}	Temperature Under Bias	−55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	2.0	—	$V_{DD} + 0.3$	V	1
V_{DD} Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	2.0	—	$V_{DDQ} + 0.3$	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	-0.3	—	0.8	V	1,3

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
- V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	$0.6 \cdot V_{DD}$	—	$V_{DD} + 0.3$	V	1
V_{DD} Input Low Voltage	V_{IL}	-0.3	—	$0.3 \cdot V_{DD}$	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	$0.6 \cdot V_{DD}$	—	$V_{DDQ} + 0.3$	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	-0.3	—	$0.3 \cdot V_{DD}$	V	1,3

Notes:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
- V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

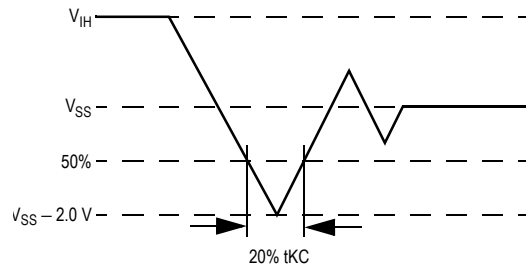
Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	-40	25	85	°C	2

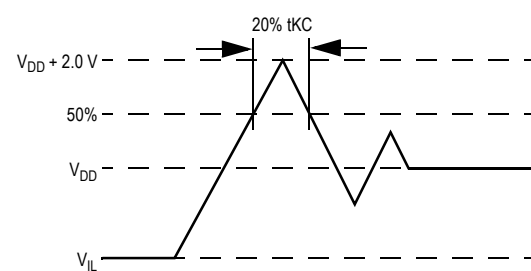
Note:

- The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
- Input Under/overshoot voltage must be $-2\text{ V} > V_i < V_{DDn} + 2\text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 2.5\text{ V}$)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0\text{ V}$	4	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{OUT} = 0\text{ V}$	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

Notes:

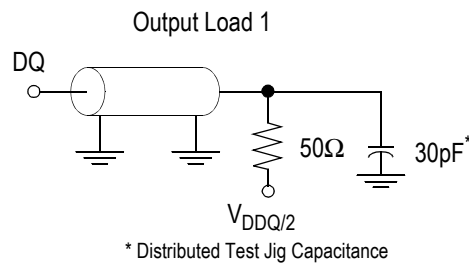
- Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
- SCMI G-38-87
- Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	$V_{DD} - 0.2\text{ V}$
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	Fig. 1

Notes:

1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	$V_{IN} = 0\text{ to }V_{DD}$	$-1\text{ }\mu\text{A}$	$1\text{ }\mu\text{A}$
ZZ and $\overline{\text{PE}}$ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ $0\text{ V} \leq V_{IN} \leq V_{IH}$	$-1\text{ }\mu\text{A}$ $-1\text{ }\mu\text{A}$	$1\text{ }\mu\text{A}$ $100\text{ }\mu\text{A}$
$\overline{\text{FT}}$, SCD, ZQ Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ $0\text{ V} \leq V_{IN} \leq V_{IL}$	$-100\text{ }\mu\text{A}$ $-1\text{ }\mu\text{A}$	$1\text{ }\mu\text{A}$ $1\text{ }\mu\text{A}$
Output Leakage Current	I_{OL}	Output Disable, $V_{OUT} = 0\text{ to }V_{DD}$	$-1\text{ }\mu\text{A}$	$1\text{ }\mu\text{A}$
Output High Voltage	V_{OH2}	$I_{OH} = -8\text{ mA}$, $V_{DDQ} = 2.375\text{ V}$	1.7 V	—
Output High Voltage	V_{OH3}	$I_{OH} = -8\text{ mA}$, $V_{DDQ} = 3.135\text{ V}$	2.4 V	—
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{ mA}$	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode	Symbol	-250		-225		-200		-166		-150		-133		Unit
				0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	0 to 70°C	-40 to 85°C	
Operating Current 3.3 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x72) Pipeline	I_{DD}	355	365	325	335	290	300	250	260	225	235	205	215	mA
			I_{DDQ}	75	75	70	70	60	60	50	50	45	45	40	40	
		Flow Through	I_{DD}	220	230	205	215	195	205	185	195	180	190	165	175	mA
			I_{DDQ}	35	35	35	35	30	30	30	30	30	30	20	20	
		(x36) Pipeline	I_{DD}	290	300	265	275	240	250	205	215	190	200	170	180	mA
			I_{DDQ}	40	40	35	35	30	30	25	25	25	25	20	20	
		Flow Through	I_{DD}	180	190	170	180	165	175	155	165	150	160	140	150	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
Operating Current 2.5 V	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x18) Pipeline	I_{DD}	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
		Flow Through	I_{DD}	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I_{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
		(x72) Pipeline	I_{DD}	355	365	325	335	290	300	250	260	225	235	205	215	mA
			I_{DDQ}	55	55	55	55	45	45	40	40	35	35	30	30	
		Flow Through	I_{DD}	220	230	205	215	195	205	185	195	180	190	165	175	mA
			I_{DDQ}	35	35	35	35	30	30	30	30	30	30	20	20	
Standby Current	ZZ $\geq V_{DD} - 0.2$ V	(x36) Pipeline	I_{DD}	290	300	265	275	240	250	205	215	190	200	170	180	mA
			I_{DDQ}	30	30	30	30	25	25	20	20	20	20	15	15	
		Flow Through	I_{DD}	180	190	170	180	165	175	155	165	150	160	140	150	mA
			I_{DDQ}	20	20	20	20	15	15	15	15	15	15	10	10	
		(x18) Pipeline	I_{DD}	260	270	235	245	215	225	185	195	170	180	155	165	mA
			I_{DDQ}	15	15	15	15	15	15	10	10	10	10	10	10	
		Flow Through	I_{DD}	165	175	155	165	150	160	140	150	135	145	125	135	mA
			I_{DDQ}	10	10	10	10	10	10	10	10	10	10	10	10	
Deselect Current	—	Pipeline	I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	mA
		Flow Through	I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	
	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	Pipeline	I_{DD}	85	90	80	85	75	80	64	70	60	65	50	55	mA
		Flow Through	I_{DD}	60	65	60	65	50	55	50	55	50	55	45	50	

Notes:

- I_{DD} and I_{DDQ} apply to any combination of V_{DD3} , V_{DD2} , V_{DDQ3} , and V_{DDQ2} operation.
- All parameters listed are worst case scenario.

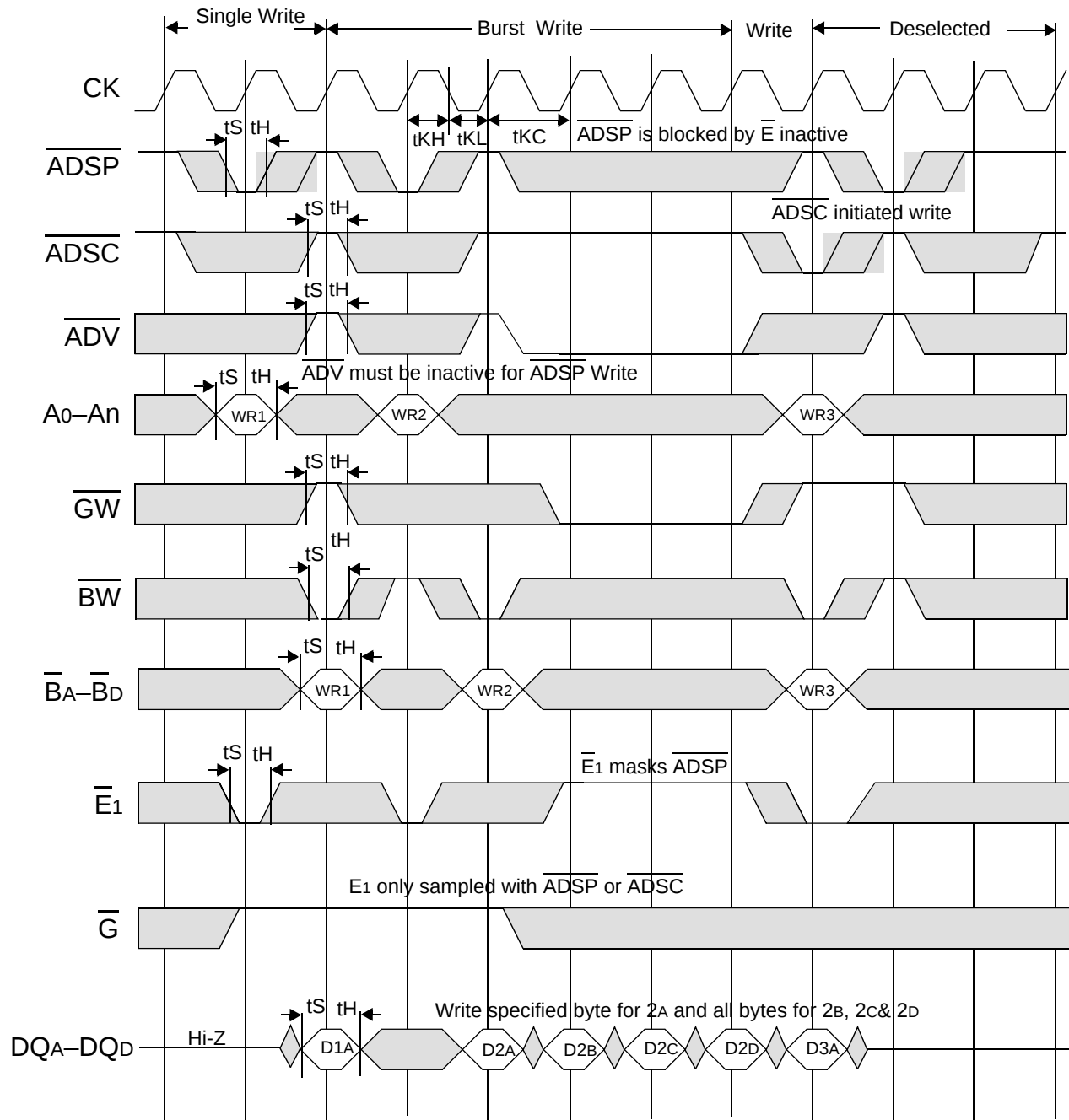
AC Electrical Characteristics

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	t _{KC}	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	t _{KQ}	—	2.5	—	2.7	—	3.0	—	3.4	—	3.8	—	4.0	ns
	Clock to Output Invalid	t _{KQX}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	t _S	1.2	—	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.2	—	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	t _{KC}	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	—	ns
	Clock to Output Valid	t _{KQ}	—	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	ns
	Clock to Output Invalid	t _{KQX}	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	t _{LZ} ¹	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	t _S	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	t _H	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	t _{KH}	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	t _{KL}	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	t _{HZ} ¹	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\bar{G}$ to Output Valid	t _{OE}	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\bar{G}$ to output in Low-Z	t _{OLZ} ¹	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\bar{G}$ to output in High-Z	t _{OHZ} ¹	—	2.3	—	2.5	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	t _{ZZS} ²	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	t _{ZZH} ²	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	t _{ZZR}	20	—	20	—	20	—	20	—	20	—	20	—	ns

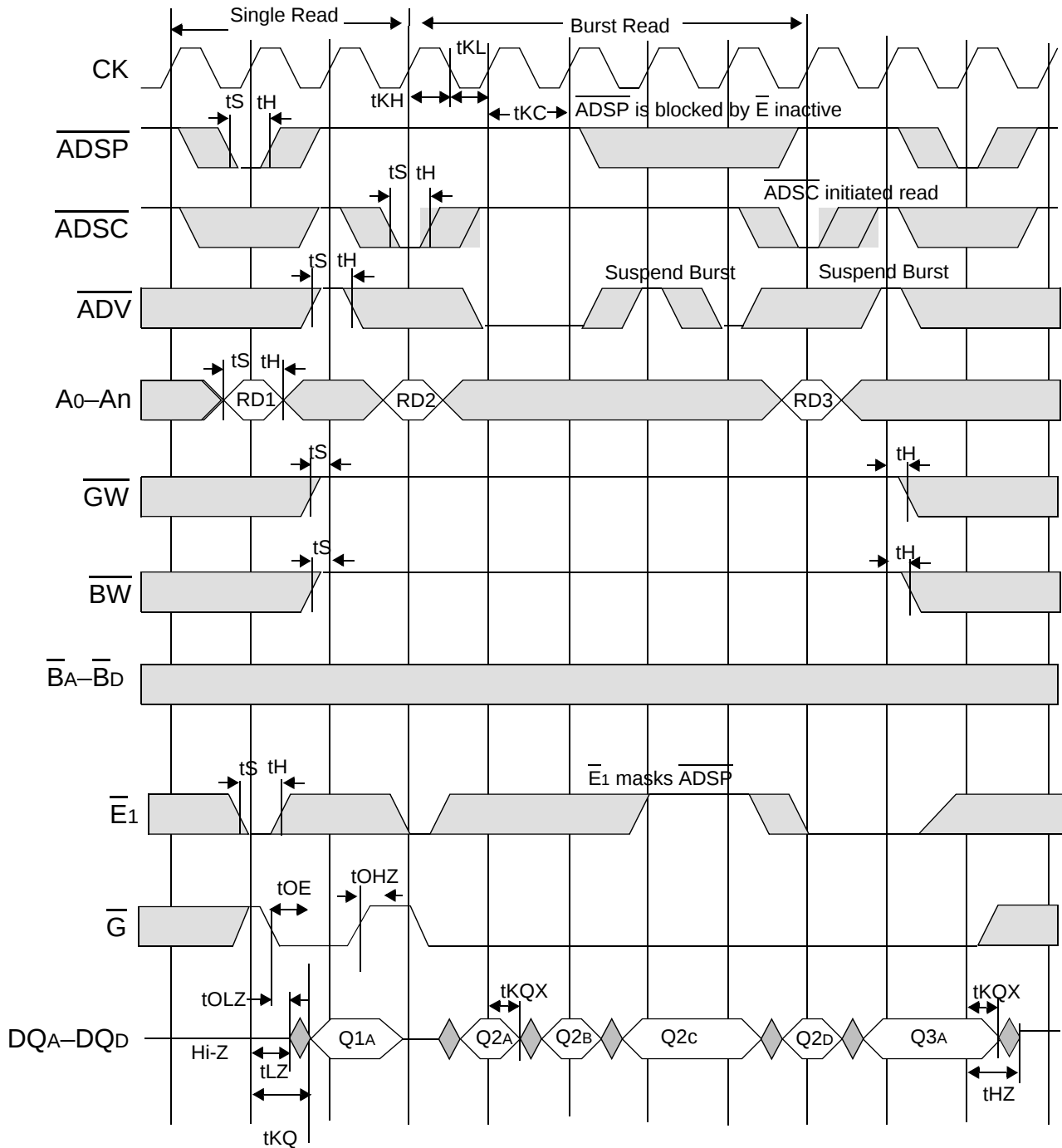
Notes:

- These parameters are sampled and are not 100% tested.
- ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

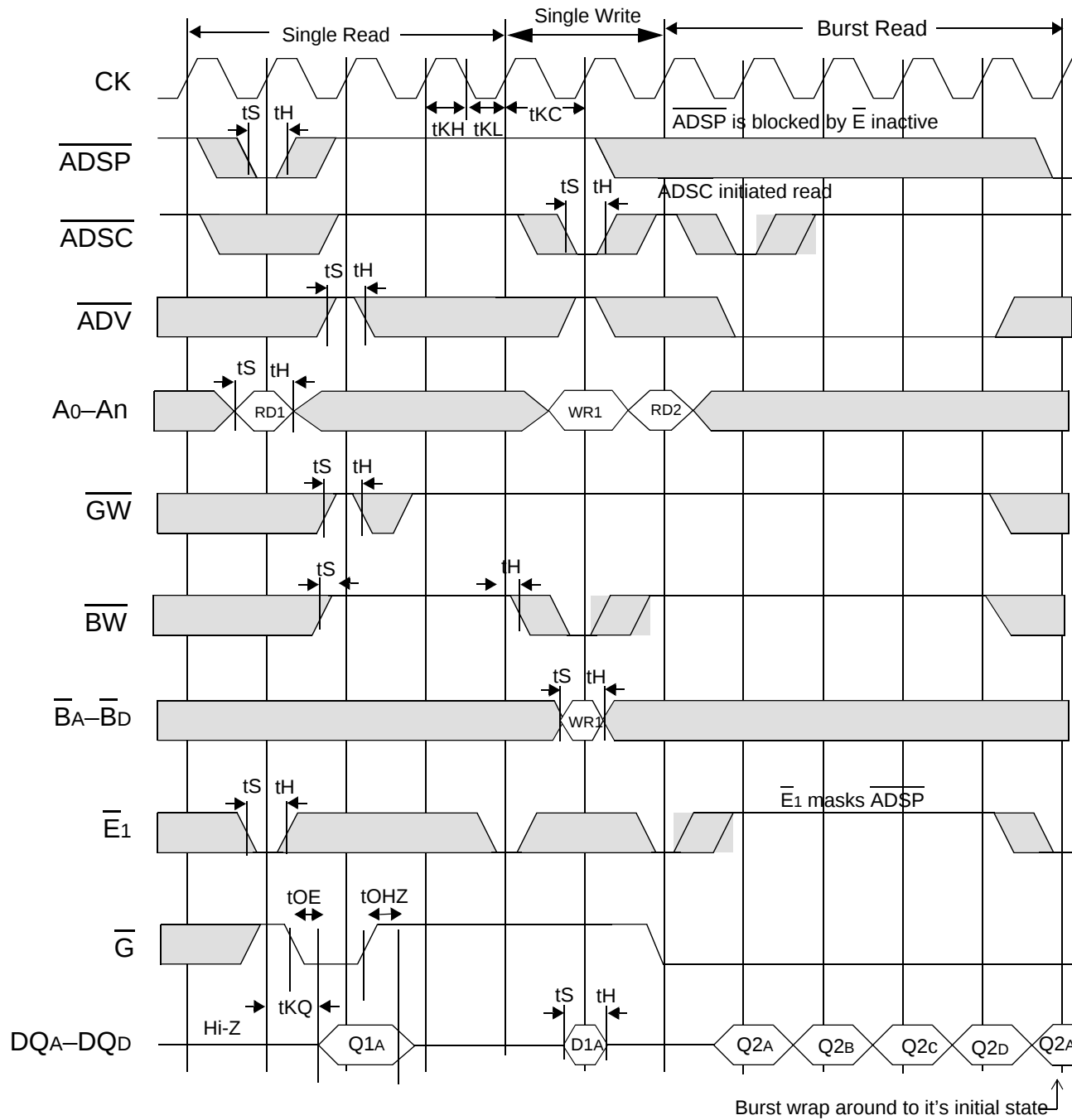
Write Cycle Timing



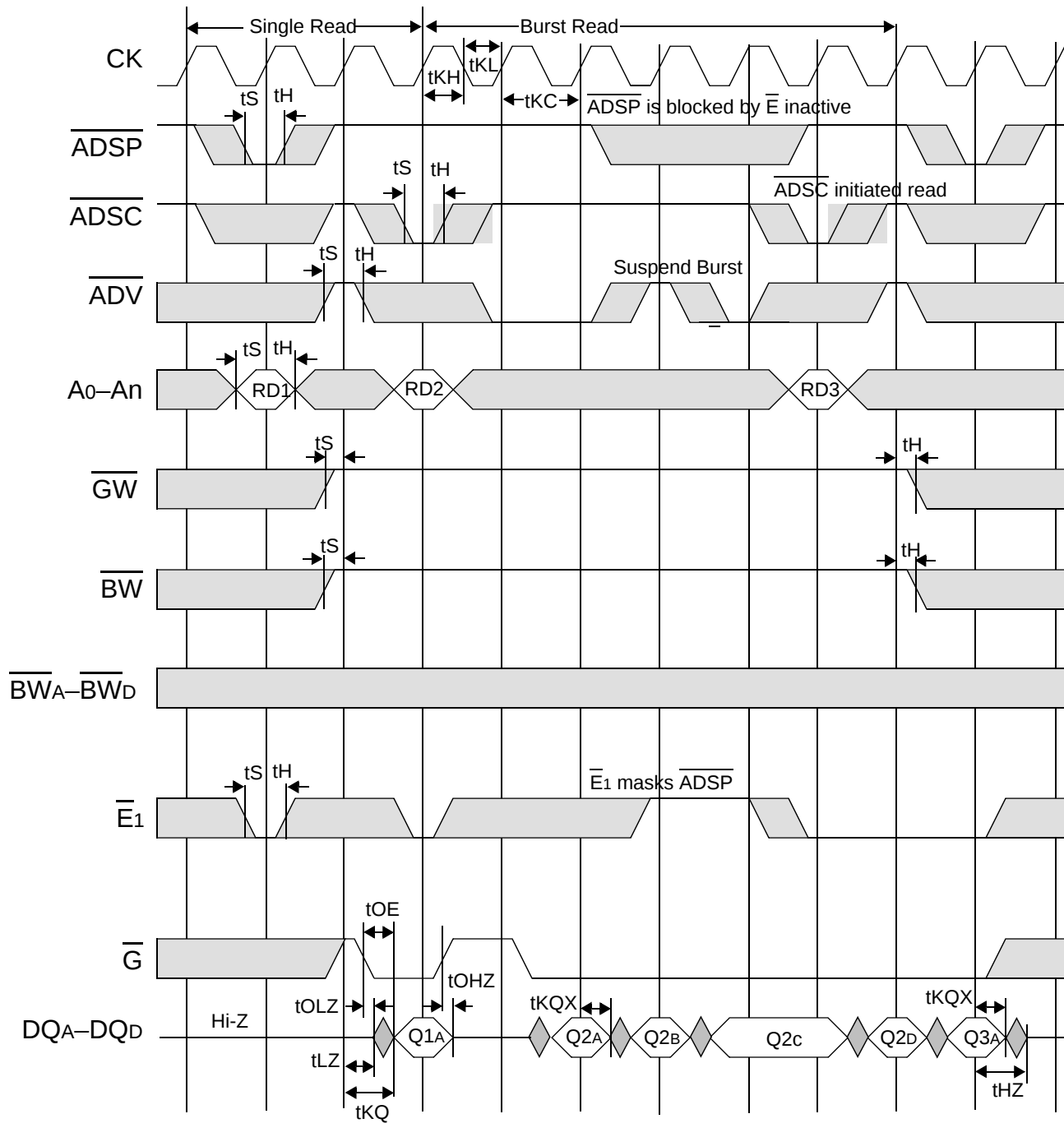
Flow Through Read Cycle Timing



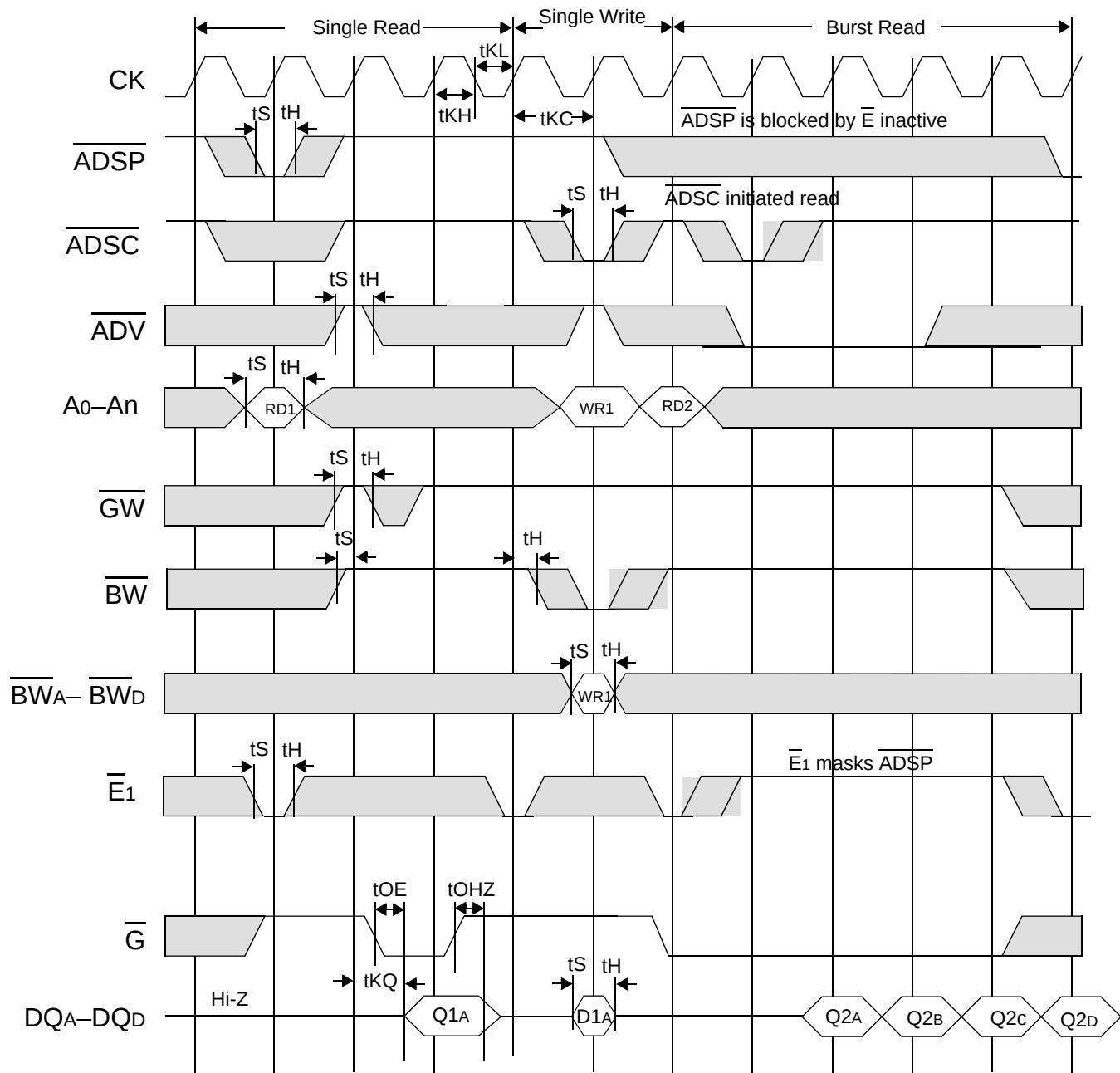
Flow Through Read-Write Cycle Timing



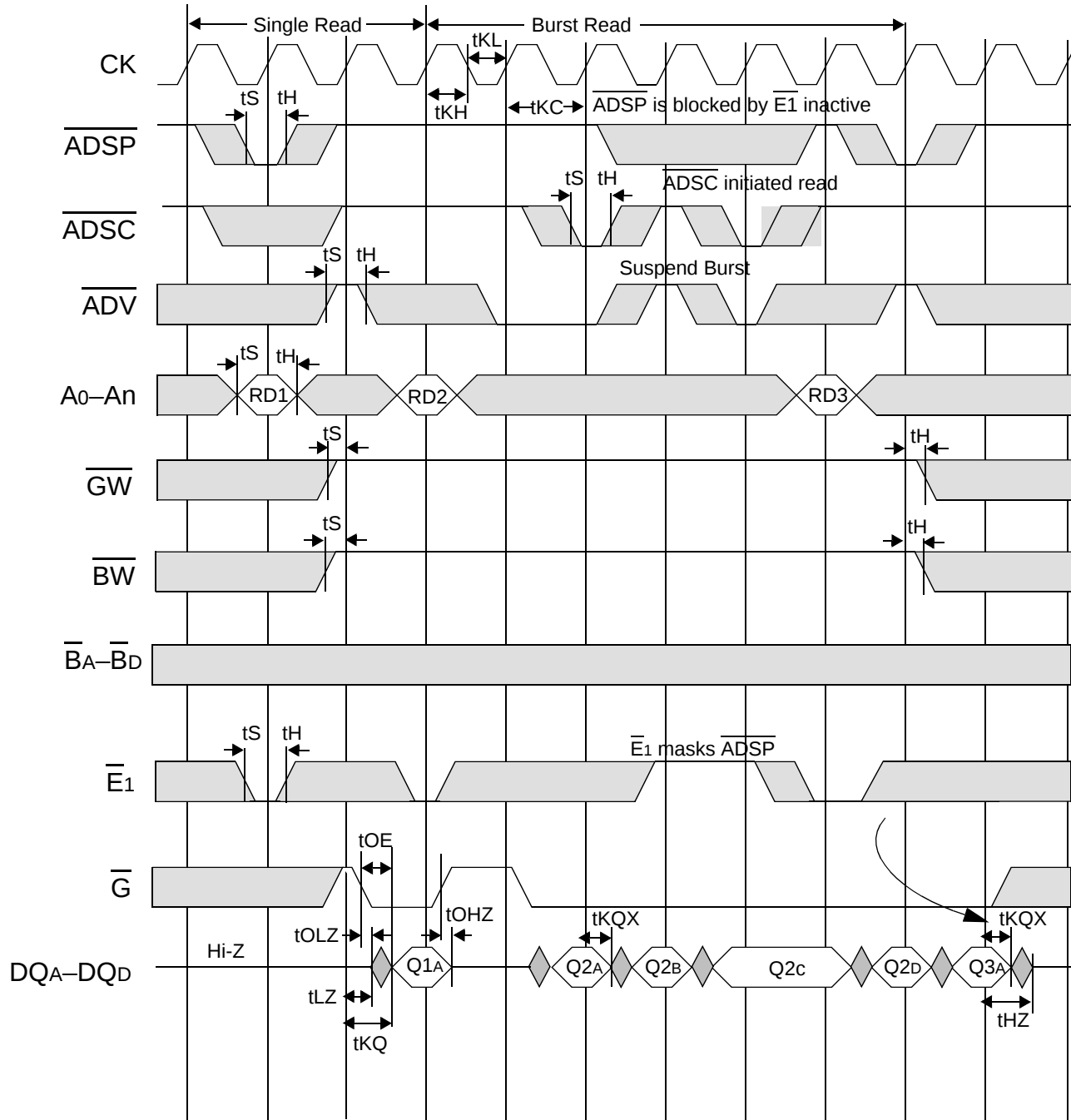
Pipelined SCD Read Cycle Timing



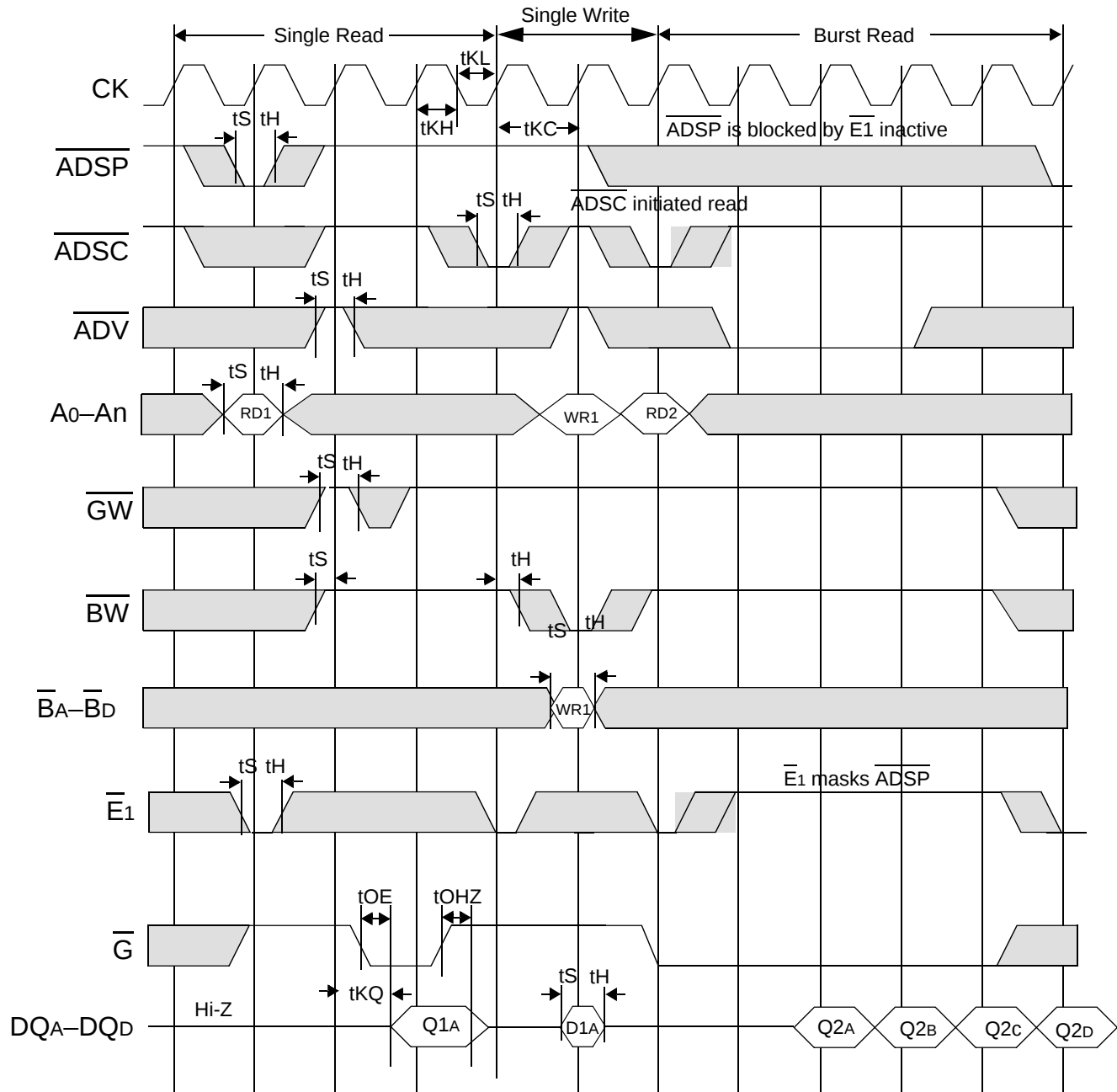
Pipelined SCD Read-Write Cycle Timing



Pipelined DCD Read Cycle Timing



Pipelined DCD Read-Write Cycle Timing

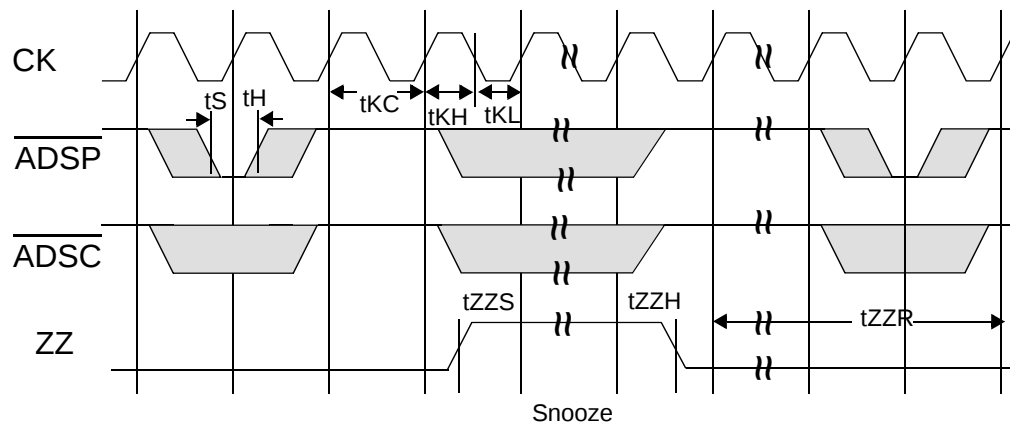


Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z. The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, I_{SB2} is guaranteed after the time t_{ZZI} is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during t_{ZZR} , only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Application Tips

Single and Dual Cycle Deselect

SCD devices (like this one) force the use of “dummy read cycles” (read cycles that are launched normally, but that are ended with the output drivers inactive) in a fully synchronous environment. Dummy read cycles waste performance, but their use usually assures there will be no bus contention in transitions from reads to writes or between banks of RAMs. DCD SRAMs do not waste bandwidth on dummy cycles and are logically simpler to manage in a multiple bank application (wait states need not be inserted at bank address boundary crossings), but greater care must be exercised to avoid excessive bus contention.

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD} . The JTAG output drivers are powered by V_{DDQ} .

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless

clocked. TCK, TDI, and TMS are designed with internal pull-up circuits. To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS} . TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:

This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automatically at power-up.

JTAG Port Registers

Overview

The various JTAG registers, referred to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

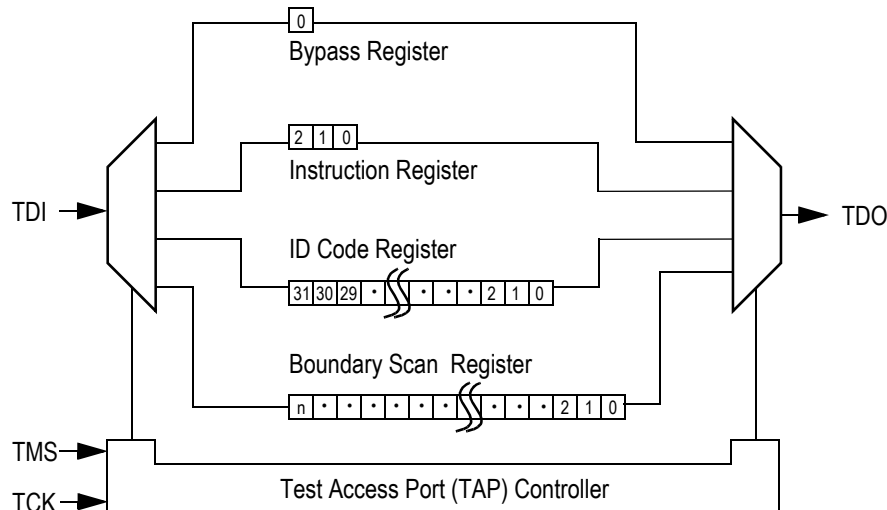
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code												Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
x72	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1	
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1	
x32	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1	0	0	1	1	
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1	
x16	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	1	0	0	1	1	

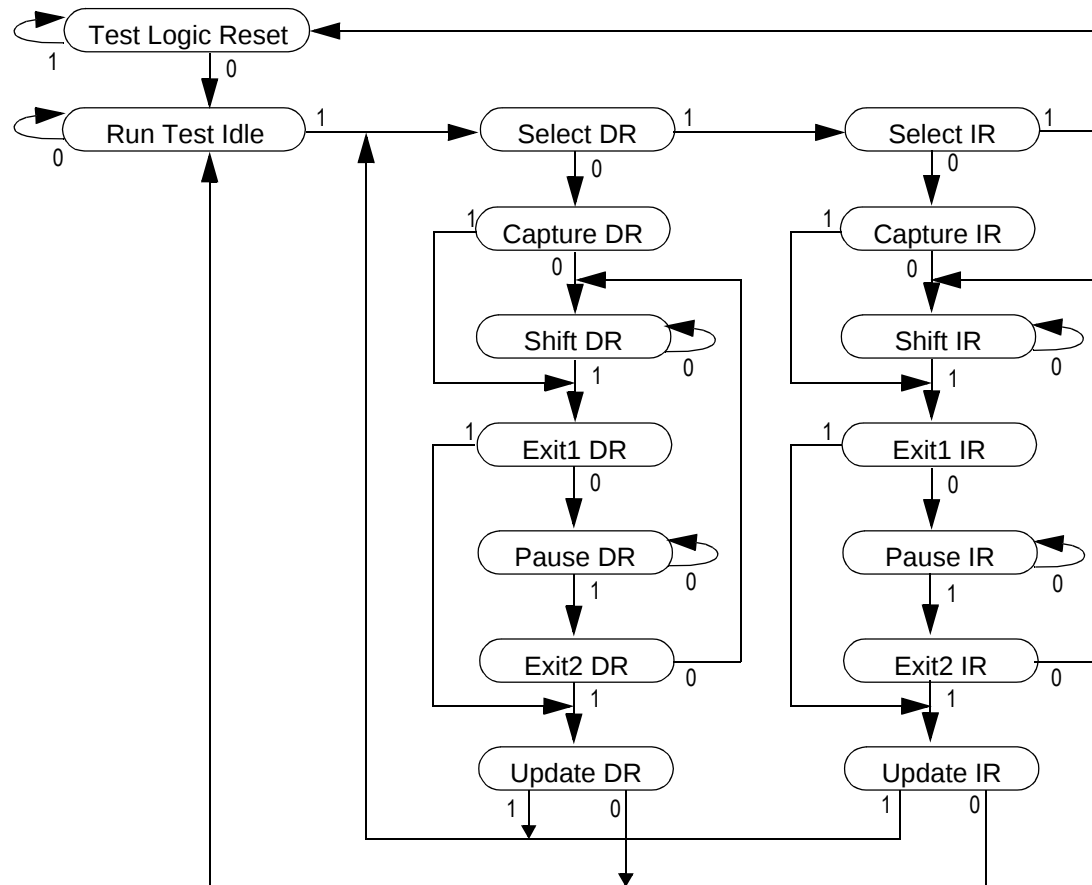
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although

allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (t_{TS} plus t_{TH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the state of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:

1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	$V_{DD3} + 0.3$	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	-0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	$0.6 * V_{DD2}$	$V_{DD2} + 0.3$	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	-0.3	$0.3 * V_{DD2}$	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	-300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	-1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	-1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	$V_{DDQ} - 100 \text{ mV}$	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:

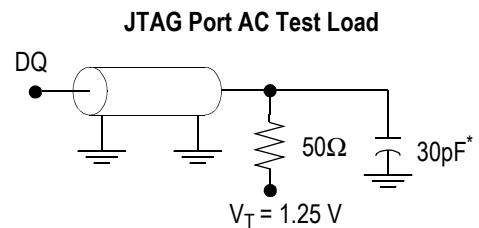
- Input Under/overshoot voltage must be $-2 \text{ V} > V_i < V_{DDn} + 2 \text{ V}$ not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
- $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
- $0 \text{ V} \leq V_{IN} \leq V_{ILJn}$
- Output Disable, $V_{OUT} = 0$ to V_{DDn}
- The TDO output driver is served by the V_{DDQ} supply.
- $I_{OHJ} = -4 \text{ mA}$
- $I_{OLJ} = +4 \text{ mA}$
- $I_{OHJC} = -100 \text{ uA}$
- $I_{OHJC} = +100 \text{ uA}$

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V

Notes:

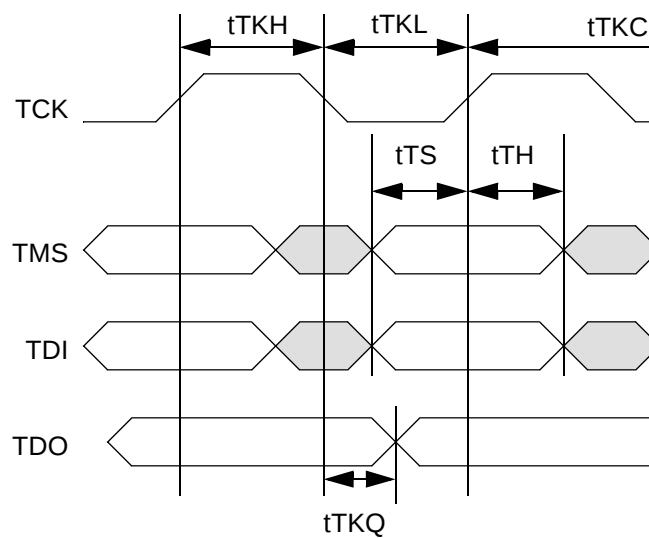
- Include scope and jig capacitance.
- Test conditions as as shown unless otherwise noted.



* Distributed Test Jig Capacitance

JTAG Port Timing Diagram

JTAG Port AC Electrical Characteristics



Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	t_{TKC}	50	—	ns
TCK Low to TDO Valid	t_{TKQ}	—	20	ns
TCK High Pulse Width	t_{TKH}	20	—	ns
TCK Low Pulse Width	t_{TKL}	20	—	ns
TDI & TMS Set Up Time	t_{TS}	10	—	ns
TDI & TMS Hold Time	t_{TH}	10	—	ns

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
1	PE			T7	R7	
2	A13	X		U5	n/a	
3	A11	X		U7	n/a	
4	A3	A10		W5	T3	
5	A12	A11		U6	T4	
6	A6	A12		V7	T5	
7	A2	A13		W7	R6	
8	A10	A14		U8	C5	
9	A5	A15		V8	B5	
10	A4	A16		V9	C6	
11	QE9	QA9	NC = 1	R11	P6	n/a
12	DE9	DA9	PH = 0	R11	P6	n/a
13	QA9	NC = 1		R10	n/a	
14	DA9	PH = 0		R10	n/a	
15	QE5	QA4	NC = 1	W11	P7	n/a
16	DE5	DA4	PH = 0	W11	P7	n/a
17	QA4	NC = 1		P11	n/a	
18	DA4	PH = 0		P11	n/a	
19	QE1	QA3	NC = 1	W10	N7	n/a
20	DE1	DA3	PH = 0	W10	N7	n/a
21	QA8	NC = 1		P10	n/a	
22	DA8	PH = 0		P10	n/a	
23	QE4	QA8	NC = 1	T10	N6	n/a
24	DE4	DA8	PH = 0	T10	N6	n/a
25	QA7	NC = 1		N10	n/a	
26	DA7	PH = 0		N10	n/a	
27	QE8	QA7	NC = 1	T11	M6	n/a
28	DE8	DA7	PH = 0	T11	M6	n/a
29	QA3	NC = 1		N11	n/a	

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
30	DA3	PH = 0		N11	n/a	
31	QE3	QA2	QA1	U10	L7	P7
32	DE3	DA2	DA1	U10	L7	P7
33	QA6	NC = 1		M10	n/a	
34	DA6	PH = 0		M10	n/a	
35	QE7	QA6	QA2	U11	L6	N6
36	DE7	DA6	DA2	U11	L6	N6
37	QA2	NC = 1		M11	n/a	
38	DA2	PH = 0		M11	n/a	
39	QE6	QA1	QA3	V11	K7	L6
40	DE6	DA1	DA3	V11	K7	L6
41	QA1	NC = 1		L11	n/a	
42	DA1	PH = 0		L11	n/a	
43	QE2	QA5	QA4	V10	K6	K7
44	DE2	DA5	DA4	V10	K6	K7
45	QA5	NC = 1		L10	n/a	
46	DA5	PH = 0		L10	n/a	
47	ZZ			P6	T7	
48	PH = 0			n/a		
49	DNU (Do Not Use)			n/a		
50	QB1		QA5	A10	H7	H6
51	DB1		DA5	A10	H7	H6
52	QF1	NC = 1		J11	n/a	
53	DF1	PH = 0		J11	n/a	
54	QB5		QA6	A11	H6	G7
55	DB5		DA6	A11	H6	G7
56	QF5	NC = 1		J10	n/a	
57	DF5	PH = 0		J10	n/a	
58	QB2		QA7	B10	G7	F6

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
59	DB2		DA7	B10	G7	F6
60	QF2	NC = 1		H11	n/a	
61	DF2	PH = 0		H11	n/a	
62	QB3	QB6	QA8	C10	G6	E7
63	DB3	DB6	DA8	C10	G6	E7
64	QF6	NC = 1		H10	n/a	
65	DF6	PH = 0		H10	n/a	
66	QB6	QB7	QA9	B11	F6	D6
67	DB6	DB7	DA9	B11	F6	D6
68	QF7	NC = 1		G10	n/a	
69	DF7	PH = 0		G10	n/a	
70	QB4	QB3	NC = 1	D10	E7	n/a
71	DB4	DB3	PH = 0	D10	E7	n/a
72	QF3	NC = 1		G11	n/a	
73	DF3	PH = 0		G11	n/a	
74	QB7	QB8	NC = 1	C11	E6	n/a
75	DB7	DB8	PH = 0	C11	E6	n/a
76	QF8	NC = 1		F10	n/a	
77	DF8	PH = 0		F10	n/a	
78	QB8	QB4	NC = 1	D11	D7	n/a
79	DB8	DB4	PH = 0	D11	D7	n/a
80	QF4	NC = 1		F11	n/a	
81	DF4	PH = 0		F11	n/a	
82	QB9		NC = 1	E11	D6	n/a
83	DB9		PH = 0	E11	D6	n/a
84	QF9	NC = 1		E10	n/a	
85	DF9	PH = 0		E10	n/a	
86	NC = 1		A19	n/a		T6
87	NC = 1	A9		n/a	A6	

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
88	A17	A8		A9	A5	
89	$\overline{ADV}$			A7	G4	
90	$\overline{ADSP}$			A5	A4	
91	$\overline{ADSC}$			A6	B4	
92	$\overline{G}$			D6	F4	
93	$\overline{BW}$			B6	M4	
94	$\overline{GW}$			D7	H4	
95	$\overline{B_H}$	NC = 1		C3	n/a	
96	$\overline{B_F}$	NC = 1		B3	n/a	
97	$\overline{B_D}$	NC = 1		B9	n/a	
98	$\overline{B_B}$	NC = 1		C9	n/a	
99	CK			K3	K4	
100	NC = 1	PH = 0		n/a		
101	PH = 0			n/a		
102	$\overline{E_3}$	A17		A8	B6	
103	$\overline{B_A}$			C8	L5	
104	$\overline{B_C}$	$\overline{B_B}$	NC = 1	B8	G5	n/a
105	$\overline{B_E}$	$\overline{B_C}$	$\overline{B_B}$	B4	G3	
106	$\overline{B_G}$	$\overline{B_D}$	NC = 1	C4	L3	n/a
107	E2	A18		A4	B2	
108	$\overline{E_1}$			C6	E4	
109	A16	A7		B7	A3	
110	A15	A6		A3	A2	
111	QG9	QC9	NC = 1	E1	D2	n/a
112	DG9	Dc9	PH = 0	E1	D2	n/a
113	QC9	NC = 1		E2	n/a	
114	Dc9	PH = 0		E2	n/a	
115	QG4	QC4	NC = 1	D2	D1	n/a
116	DG4	Dc4	PH = 0	D2	D1	n/a

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
117	QC8	NC = 1		F2	n/a	
118	Dc8	PH = 0		F2	n/a	
119	QG8	QC3	NC = 1	D1	E1	n/a
120	DG8	Dc3	PH = 0	D1	E1	n/a
121	QC4	NC = 1		F1	n/a	
122	Dc4	PH = 0		F1	n/a	
123	QG7	QC8	NC = 1	C1	E2	n/a
124	DG7	Dc8	PH = 0	C1	E2	n/a
125	QC7	NC = 1		G2	n/a	
126	Dc7	PH = 0		G2	n/a	
127	QG3	QC7	NC = 1	C2	F2	n/a
128	DG3	Dc7	PH = 0	C2	F2	n/a
129	QC3	NC = 1		G1	n/a	
130	Dc3	PH = 0		G1	n/a	
131	QG6	QC2	QB1	B1	G1	D1
132	DG6	Dc2	DB1	B1	G1	D1
133	QC6	NC = 1		H2	n/a	
134	Dc6	PH = 0		H2	n/a	
135	QG5	QC6	QB2	A1	G2	E2
136	DG5	Dc6	DB2	A1	G2	E2
137	QC2	NC = 1		H1	n/a	
138	Dc2	PH = 0		H1	n/a	
139	QG2	QC1	QB3	B2	H1	G2
140	DG2	Dc1	DB3	B2	H1	G2
141	QC1	NC = 1		J1	n/a	
142	Dc1	PH = 0		J1	n/a	
143	QG1	QC5	QB4	A2	H2	H1
144	DG1	Dc5	DB4	A2	H2	H1
145	QC5	NC = 1		J2	n/a	

GS816218/36/72 Boundary Scan Chain Order

Order	x72	x36	x18	Bump		
				x72	x36	x18
146	DC5	PH = 0		J2	n/a	
147	FT			L6	R5	
148	DNU (Do Not Use)			n/a		
149	SCD			N6	L4	
150	QD2	QD1	QB5	V2	K1	K2
151	DD2	DD1	DB5	V2	K1	K2
152	QH1	NC = 1		L1	n/a	
153	DH1	PH = 0		L1	n/a	
154	QD1	QD5	QB6	W2	K2	L1
155	DD1	DD5	DB6	W2	K2	L1
156	QH5	NC = 1		L2	n/a	
157	DH5	PH = 0		L2	n/a	
158	QD5	QD2	QB7	W1	L1	M2
159	DD5	DD2	DB7	W1	L1	M2
160	QH2	NC = 1		M1	n/a	
161	DH2	PH = 0		M1	n/a	
162	QD6		QB8	V1	L2	N1
163	DD6		DB8	V1	L2	N1
164	QH6	NC = 1		M2	n/a	
165	DH6	PH = 0		M2	n/a	
166	QD7		QB9	U1	M2	P2
167	DD7		DB9	U1	M2	P2
168	QH4	NC = 1		P1	n/a	
169	DH4	PH = 0		P1	n/a	
170	QD3		NC = 1	U2	N1	n/a
171	DD3		PH = 0	U2	N1	n/a
172	QH7	NC = 1		N2	n/a	
173	DH7	PH = 0		N2	n/a	
174	QD4	QD8	NC = 1	T2	N2	n/a

GS816218/36/72 Boundary Scan Chain Order

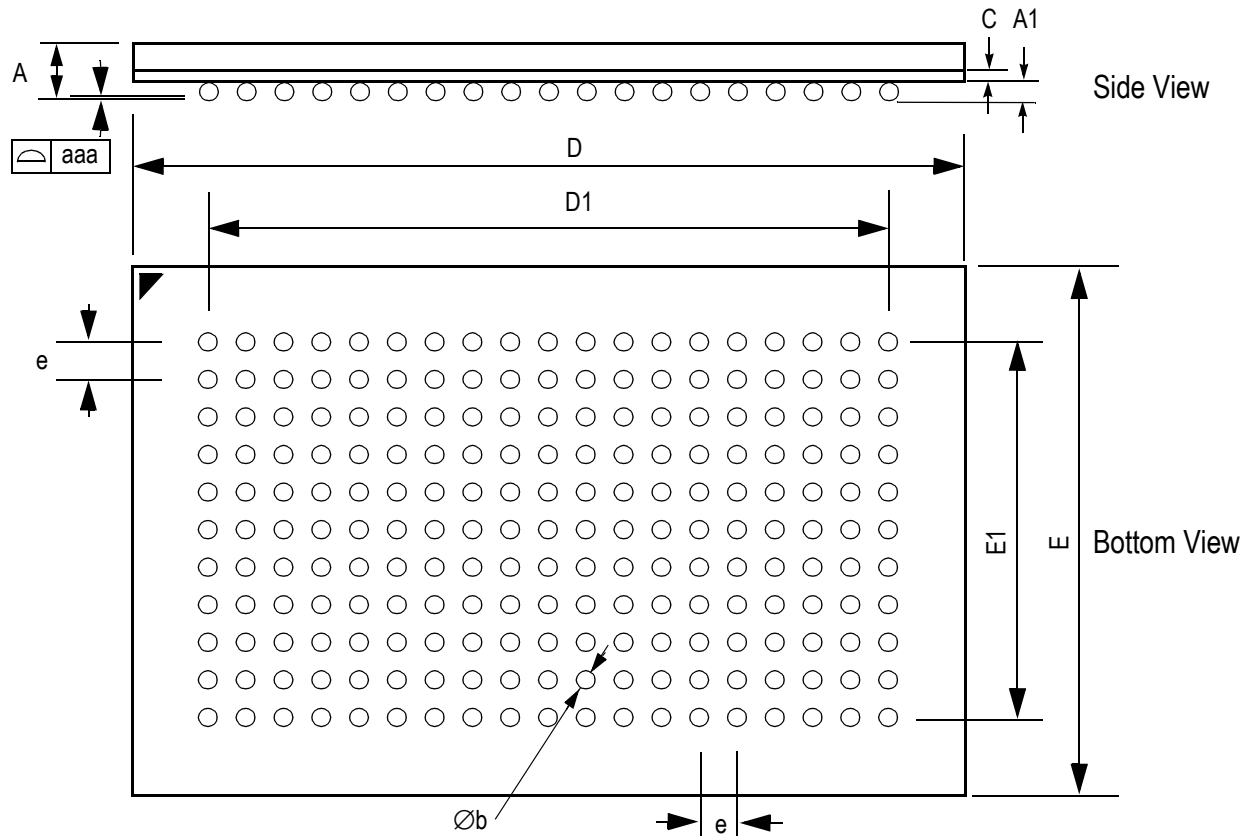
Order	x72	x36	x18	Bump		
				x72	x36	x18
175	DD4	DD8	PH = 0	T2	N2	n/a
176	QH3	NC = 1		N1	n/a	
177	DH3	PH = 0		N1	n/a	
178	QD8	QD4	NC = 1	T1	P1	n/a
179	DD8	DD4	PH = 0	T1	P1	n/a
180	QH8	NC = 1		P2	n/a	
181	DH8	PH = 0		P2	n/a	
182	QD9		NC = 1	R1	P2	n/a
183	DD9		PH = 0	R1	P2	n/a
184	QH9	NC = 1		R2	n/a	
185	DH9	PH = 0		R2	n/a	
186	$\overline{\text{LBO}}$			T6	R3	
187	A9	A5		V3	C2	
188	A14	A4		U4	B3	
189	A8	A3		V4	C3	
190	A7	A2		V5	R2	
191	A1			V6	N4	
192	A0			W6	P4	
193	ZQ			F6	D4	
194	$\overline{\text{G}}$			D6	F4	

Notes:

- Depending on the package, some input pads of the scan chain may not be connected to any external pin. In such case: $\overline{LBO} = 1$, $ZQ = 1$, $\overline{PE} = 0$, $SD = 0$, $ZZ = 0$, $\overline{FT} = 1$, $DP = 1$, and $SCD = 1$.
- Every DQ pad consists of two scan registers—D is for input capture, and Q is for output capture.
- A single register (#194) for controlling tristate of all the DQ pins is at the end of the scan chain (i.e., the last bit shifted in this tristate control is effective after JTAG EXTEST instruction is executed.
- 1 = no connect, internally set to logic value 1
- 0 = no connect, internally set to logic value 0
- X = no connect, value is undefined

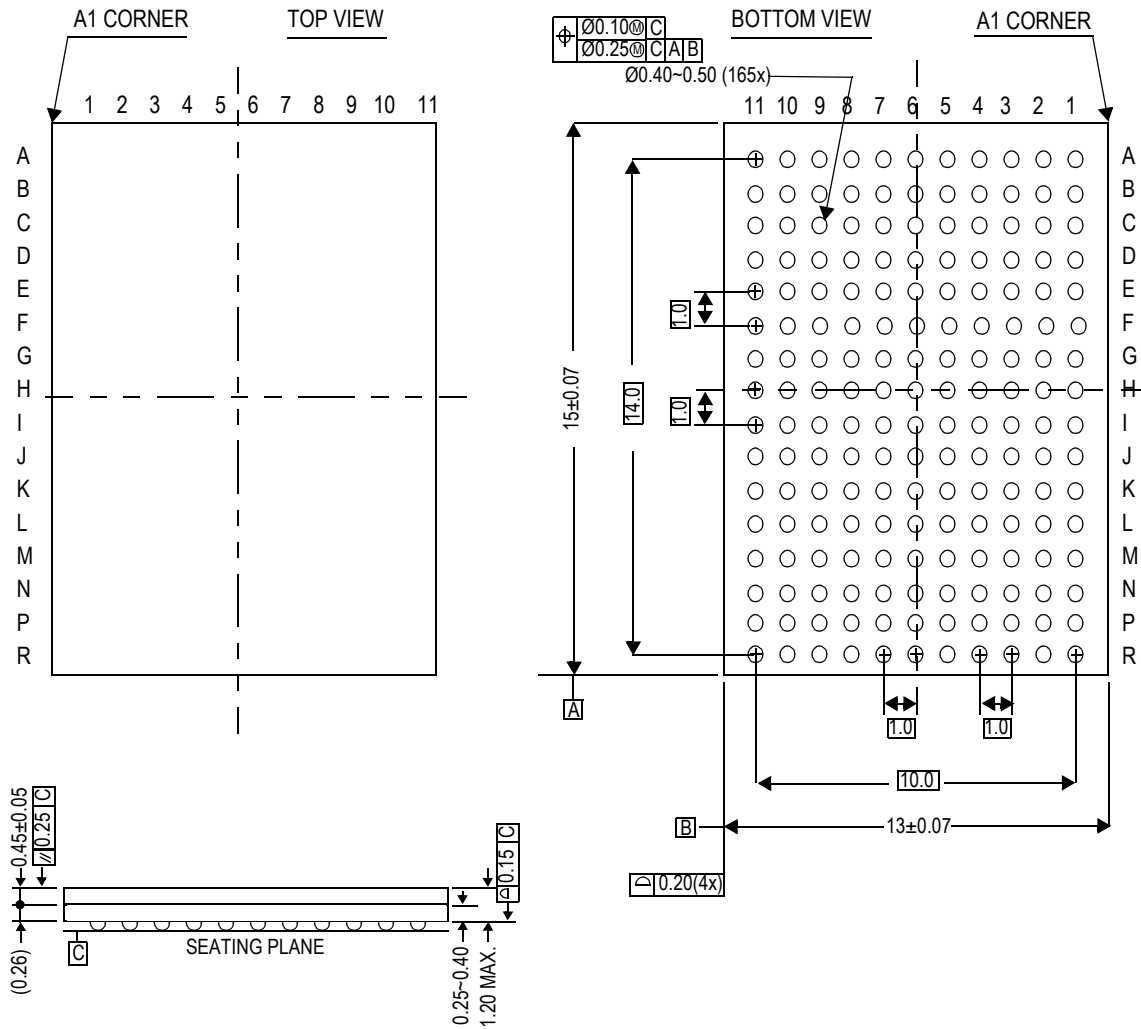
209 BGA Package Drawing (Package B)

14 mm x 22 mm Body, 1.0 mm Bump Pitch, 11 x 19 Bump Array

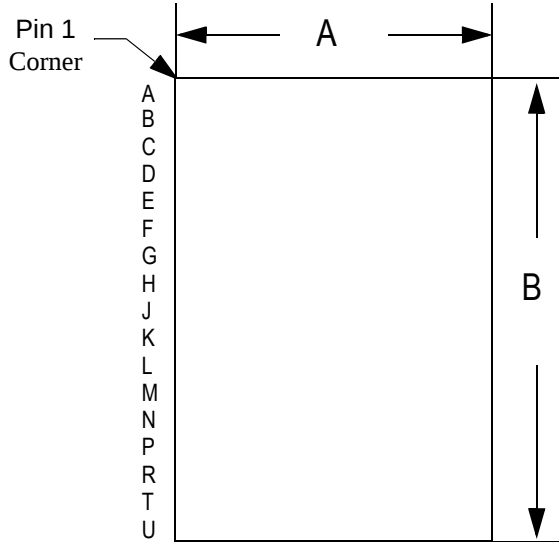


Symbol	Min	Typ	Max	Units
A			1.70	mm
A1	0.40	0.50	0.60	mm
Øb	0.50	0.60	0.70	mm
c	0.31	0.36	0.38	mm
D	21.9	22.0	22.1	mm
D1		18.0 (BSC)		mm
E	13.9	14.0	14.1	mm
E1		10.0 (BSC)		mm
e		1.00 (BSC)		mm
aaa		0.15		mm
Rev 1.0				

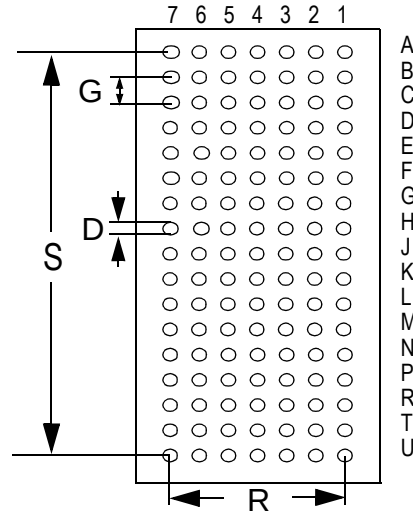
Package Dimensions—165-Bump FPBGA (Package D)



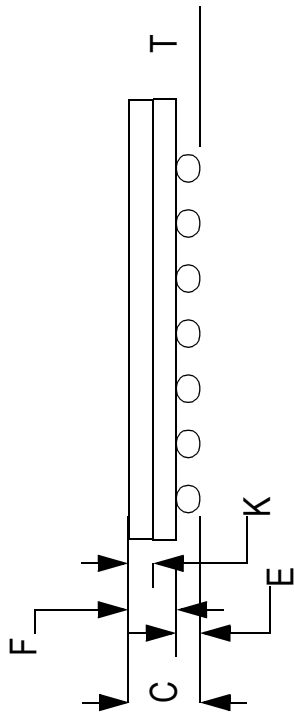
119-Bump BGA Package (Package B)



Top View



Bottom View



Side View

Package Dimensions—119-Pin PBGA

Symbol	Description	Min.	Nom.	Max
A	Width	13.9	14.0	14.1
B	Length	21.9	22.0	22.1
C	Package Height (including ball)	1.73	1.86	1.99
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)	1.16	1.26	1.36
G	Width between Balls		1.27	
K	Package Height above board	0.65	0.70	0.75
R	Width of package between balls		7.62	
S	Length of package between balls		20.32	
T	Variance of Ball Height		0.15	

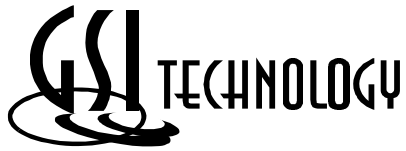
Unit: mm

Ordering Information for GSI Synchronous Burst RAMs

Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS816218B-250	NBT Pipeline/Flow Through	119 BGA	250/5.5	C	
1M x 18	GS816218B-225	NBT Pipeline/Flow Through	119 BGA	225/6	C	
1M x 18	GS816218B-200	NBT Pipeline/Flow Through	119 BGA	200/6.5	C	
1M x 18	GS816218B-166	NBT Pipeline/Flow Through	119 BGA	166/7	C	
1M x 18	GS816218B-150	NBT Pipeline/Flow Through	119 BGA	150/7.5	C	
1M x 18	GS816218B-133	NBT Pipeline/Flow Through	119 BGA	133/8.5	C	
512K x 36	GS816236B-250	NBT Pipeline/Flow Through	119 BGA	250/5.5	C	
512K x 36	GS816236B-225	NBT Pipeline/Flow Through	119 BGA	225/6	C	
512K x 36	GS816236B-200	NBT Pipeline/Flow Through	119 BGA	200/6.5	C	
512K x 36	GS816236B-166	NBT Pipeline/Flow Through	119 BGA	166/7	C	
512K x 36	GS816236B-150	NBT Pipeline/Flow Through	119 BGA	150/7.5	C	
512K x 36	GS816236B-133	NBT Pipeline/Flow Through	119 BGA	133/8.5	C	
1M x 18	GS816218D-250	NBT Pipeline/Flow Through	165 BGA	250/5.5	C	
1M x 18	GS816218D-225	NBT Pipeline/Flow Through	165 BGA	225/6	C	
1M x 18	GS816218D-200	NBT Pipeline/Flow Through	165 BGA	200/6.5	C	
1M x 18	GS816218D-166	NBT Pipeline/Flow Through	165 BGA	166/7	C	
1M x 18	GS816218D-150	NBT Pipeline/Flow Through	165 BGA	150/7.5	C	
1M x 18	GS816218D-133	NBT Pipeline/Flow Through	165 BGA	133/8.5	C	
512K x 36	GS816236D-250	NBT Pipeline/Flow Through	165 BGA	250/5.5	C	
512K x 36	GS816236D-225	NBT Pipeline/Flow Through	165 BGA	225/6	C	
512K x 36	GS816236D-200	NBT Pipeline/Flow Through	165 BGA	200/6.5	C	
512K x 36	GS816236D-166	NBT Pipeline/Flow Through	165 BGA	166/7	C	
512K x 36	GS816236D-150	NBT Pipeline/Flow Through	165 BGA	150/7.5	C	
512K x 36	GS816236D-133	NBT Pipeline/Flow Through	165 BGA	133/8.5	C	
256K x 72	GS816272C-250	NBT Pipeline/Flow Through	209 BGA	250/5.5	C	
256K x 72	GS816272C-225	NBT Pipeline/Flow Through	209 BGA	225/6	C	
256K x 72	GS816272C-200	NBT Pipeline/Flow Through	209 BGA	200/6.5	C	
256K x 72	GS816272C-166	NBT Pipeline/Flow Through	209 BGA	166/7	C	
256K x 72	GS816272C-150	NBT Pipeline/Flow Through	209 BGA	150/7.5	C	
256K x 72	GS816272C-133	NBT Pipeline/Flow Through	209 BGA	133/8.5	C	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS816236-200IT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
- GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsistechnology.com) for a complete listing of current offerings



Org	Part Number ¹	Type	Package	Speed ² (MHz/ns)	T _A ³	Status
1M x 18	GS816218B-250I	NBT Pipeline/Flow Through	119 BGA	250/5.5	I	Not Available
1M x 18	GS816218B-225I	NBT Pipeline/Flow Through	119 BGA	225/6	I	
1M x 18	GS816218B-200I	NBT Pipeline/Flow Through	119 BGA	200/6.5	I	
1M x 18	GS816218B-166I	NBT Pipeline/Flow Through	119 BGA	166/7	I	
1M x 18	GS816218B-150I	NBT Pipeline/Flow Through	119 BGA	150/7.5	I	
1M x 18	GS816218B-133I	NBT Pipeline/Flow Through	119 BGA	133/8.5	I	
512K x 36	GS816236B-250I	NBT Pipeline/Flow Through	119 BGA	250/5.5	I	Not Available
512K x 36	GS816236B-225I	NBT Pipeline/Flow Through	119 BGA	225/6	I	
512K x 36	GS816236B-200I	NBT Pipeline/Flow Through	119 BGA	200/6.5	I	
512K x 36	GS816236B-166I	NBT Pipeline/Flow Through	119 BGA	166/7	I	
512K x 36	GS816236B-150I	NBT Pipeline/Flow Through	119 BGA	150/7.5	I	
512K x 36	GS816236B-133I	NBT Pipeline/Flow Through	119 BGA	133/8.5	I	
1M x 18	GS816218D-250I	NBT Pipeline/Flow Through	165 BGA	250/5.5	I	Not Available
1M x 18	GS816218D-225I	NBT Pipeline/Flow Through	165 BGA	225/6	I	
1M x 18	GS816218D-200I	NBT Pipeline/Flow Through	165 BGA	200/6.5	I	
1M x 18	GS816218D-166I	NBT Pipeline/Flow Through	165 BGA	166/7	I	
1M x 18	GS816218D-150I	NBT Pipeline/Flow Through	165 BGA	150/7.5	I	
1M x 18	GS816218D-133I	NBT Pipeline/Flow Through	165 BGA	133/8.5	I	
512K x 36	GS816236D-250I	NBT Pipeline/Flow Through	165 BGA	250/5.5	I	
512K x 36	GS816236D-225I	NBT Pipeline/Flow Through	165 BGA	225/6	I	
512K x 36	GS816236D-200I	NBT Pipeline/Flow Through	165 BGA	200/6.5	I	
512K x 36	GS816236D-166I	NBT Pipeline/Flow Through	165 BGA	166/7	I	
512K x 36	GS816236D-150I	NBT Pipeline/Flow Through	165 BGA	150/7.5	I	
512K x 36	GS816236D-133I	NBT Pipeline/Flow Through	165 BGA	133/8.5	I	
256K x 72	GS816272C-250I	NBT Pipeline/Flow Through	209 BGA	250/5.5	I	Not Available
256K x 72	GS816272C-225I	NBT Pipeline/Flow Through	209 BGA	225/6	I	
256K x 72	GS816272C-200I	NBT Pipeline/Flow Through	209 BGA	200/6.5	I	
256K x 72	GS816272C-166I	NBT Pipeline/Flow Through	209 BGA	166/7	I	
256K x 72	GS816272C-150I	NBT Pipeline/Flow Through	209 BGA	150/7.5	I	
256K x 72	GS816272C-133I	NBT Pipeline/Flow Through	209 BGA	133/8.5	I	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS816236-200IT.
- The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
- T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
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18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
GS816218B-150IB 1.00 9/ 1999A;GS816218B-150IB 2.00 1/1999B	Content	• Converted from 0.25u 3.3V process to 0.18u 2.5V process. Master File Rev B • Added x72 Pinout. • Added GSI Logo.
GS816218B 2.01 1/ 2000C;GS816218 B 2.02 1/ 2000D		• Changed BGA package drawing for 209 pin package.
GS18/362.0 1/2000DGS18/ 362.03 2/2000E		• Front page; Features - changed 2.5V I/O supply to 2.5V or 3.3V I/O supply; Core and Interface voltages - Changed paragraph to include information for 3.3V; Completeness • Absolute Maximum Ratings; Changed VDDQ - Value: From: -.05 to VDD : to : -.05 to 3.6; Completeness. • Recommended Operating Conditions; Changed: I/O Supply Voltage- Max. from VDD to 3.6; Input High Voltage- Max. from VDD +0.3 to 3.6; Same page - took out Note 1; Completeness • Electrical Characteristics - Added second Output High Voltage line to table; completeness. • Note: There was not a Rev 2.02 for the 8160Z or the 8161Z.
GS18/362.03 2/2000E; 816218_r2_04	Content	• Updated pad out and pin description table (7D changed from NC to GW)
816218_r2_04; 816218_r2_05	Content	• Updated BGA pin description table to comply with JEDEC standards
816218_r2_05; 816218_r2_06	Content	• Changed the value of ZZ recovery in the AC Electrical Characteristics table on page 19 from 20 ns to 100 ns
816218_r2_06; 816218_r2_07	Content/Format	• Added 225 MHz speed bin • Updated numbers in page 1 table, AC Characteristics table, and Operating Currents table • Updated format to comply with Technical Publications standards
816218_r2_07; 816218_r2_08	Content	• Changed V_{SSQ} references to V_{SS} • Changed K4 and K8 in 209-bump BGA to NC • Updated Capacitance table—removed Input row and changed Output row to I/O
816218_r2_08; 816218_r2_09	Content	• Updated numbers for Clock to Output Valid (PL) and Clock to Output Valid (FT) for 166 MHz and 133 MHz on AC Electrical Characteristics table
816218_r2_09; 816218_r2_10	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions table on page 9

18Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
816218_r2_10; 816218_r2_11	Content	• Added 3.3 V references to entire document • Updated Operating Conditions table • Updated JTAG section • Updated Boundary Scan Chain table • Updated Operating Currents table and added note • Updated Application Tips paragraph • Update table on page 1; added power numbers
816218_r2_11; 816218_r2_12	Content	• Updated JTAG ID Register table • Updated Synchronous Truth table • Updated Operating Currents table • Updated table on page 1; updated power numbers • Updated Recommended Operating Conditions table (added V_{DDQ} references)
816218_r2_12; 816218_r2_13	Content	• Updated table on page 1 • Added 119-Bump BGA Pin Description table • Created recommended operating conditions tables on pages 16 and 17 • Updated AC Electrical Characteristics table • Added Sleep mode description on page 29 • Updated Ordering Information for 225 MHz part (changed from 7ns to 6.5 ns) • Updated BSR table (2 and 3 changed to X (value undefined)) • Added 250 MHz speed bin • Deleted 180 MHz speed bin
816218_r2_13; 816218_r2_14	Content	• Updated AC Characteristics table • Updated package designator for 209 BGA from B to C • Updated VIH from 1.7 to 2.0 • Updated FT power numbers • Updated Mb references from 16Mb to 18Mb • Removed ByteSafe references • Changed DP and QE pins to NC • Updated ZZ recovery time diagram • Add 165-bump FPBGA package • Updated AC Test Conditions table and removed Output Load 2 diagram