100-Pin TQFP
Commercial Temp
Industrial Temp

18Mb Pipelined and Flow Through Synchronous NBT SRAM

250 MHz–133 MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- User-configurable Pipeline and Flow Through mode
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization
- Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- IEEE 1149.1 JTAG-compatible Boundary Scan
- On-chip write parity checking; even or odd selectable
- 2.5 V or 3.3 V +10%/–10% core power supply
- LBO pin for Linear or Interleave Burst mode
- Pin-compatible with 2M, 4M, and 8M devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ pin for automatic power-down
- JEDEC-standard 100-lead TQFP package

		-250	-225	-200	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.5	2.7	3.0	3.4	3.8	4.0	ns
	tCycle	4.0	4.4	5.0	6.0	6.7	7.5	ns
3.3 V	Curr (x18)	280	255	230	200	185	165	mA
	Curr (x36)	330	300	270	230	215	190	mA
2.5 V	Curr (x18)	275	250	230	195	180	165	mA
	Curr (x36)	320	295	265	225	210	185	mA
Flow Through 2-1-1-1	t_{KQ}	5.5	6.0	6.5	7.0	7.5	8.5	ns
	tCycle	5.5	6.0	6.5	7.0	7.5	8.5	ns
3.3 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x36)	200	190	180	170	165	150	mA
2.5 V	Curr (x18)	175	165	160	150	145	135	mA
	Curr (x36)	200	190	180	170	165	150	mA

Functional Description

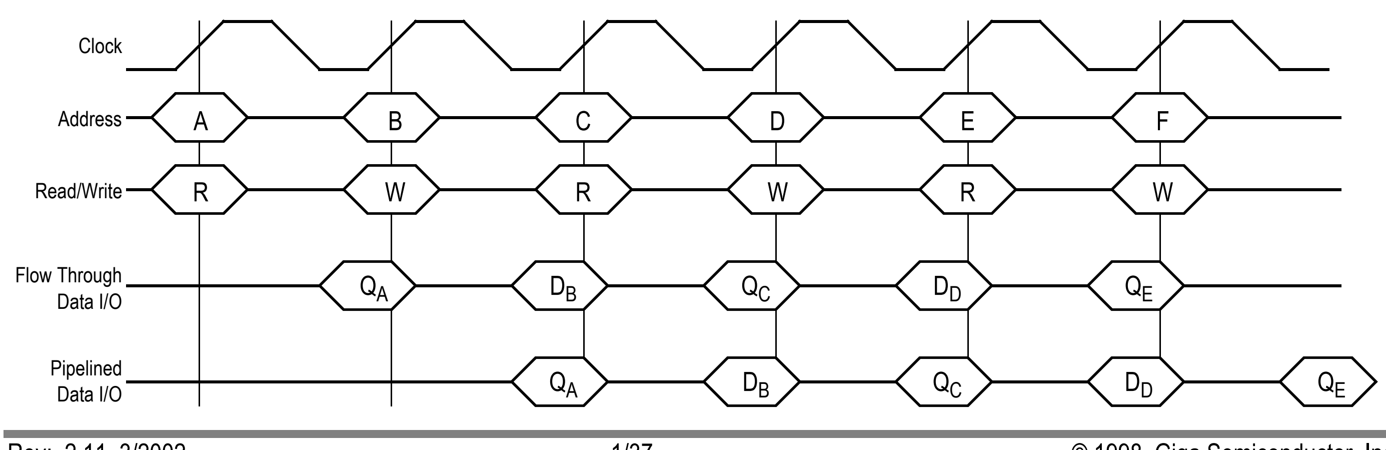
The GS8161Z18/36T is an 18Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control (LBO) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable, ZZ and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

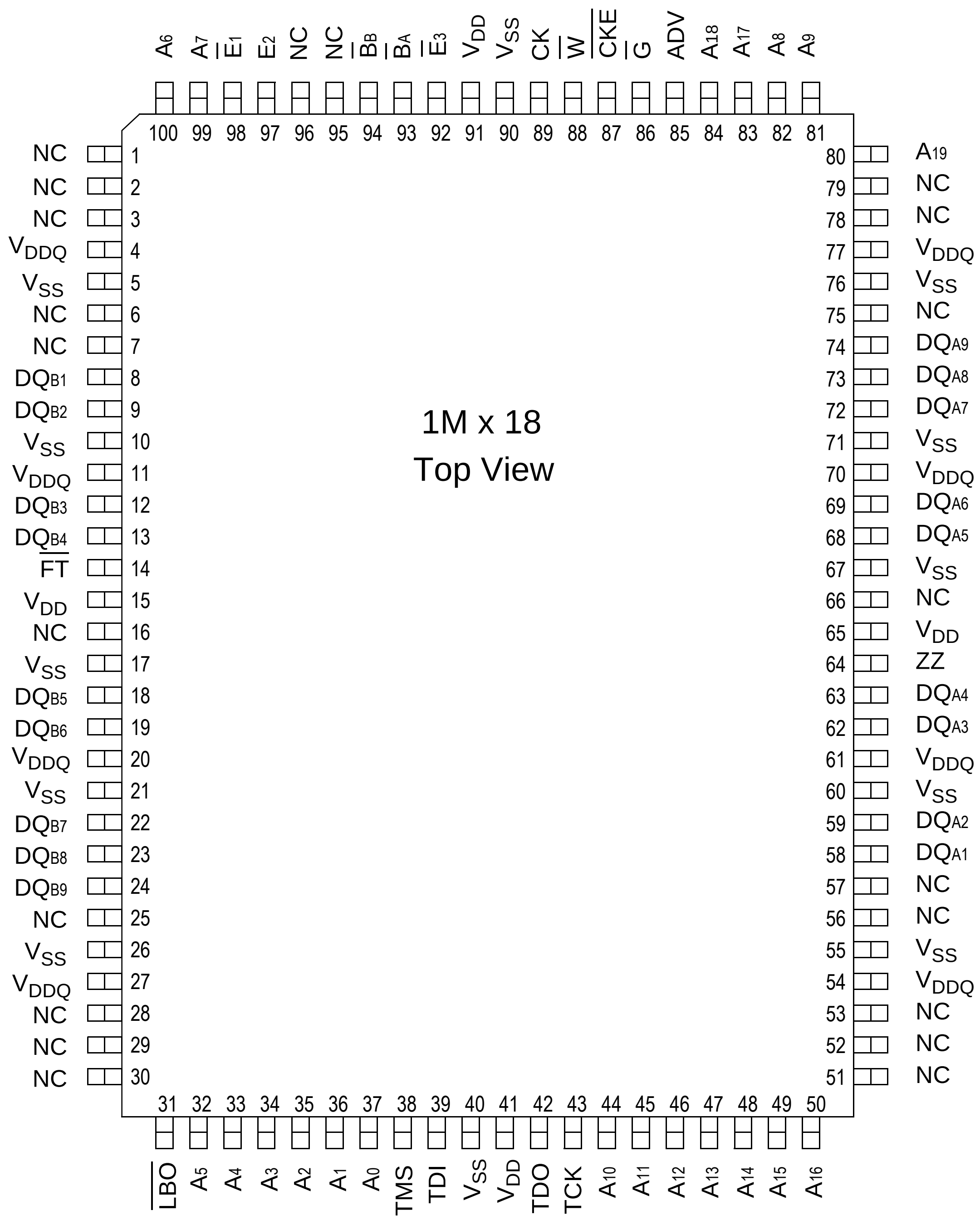
The GS8161Z18/36T may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, in addition to the rising-edge-triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS8161Z18/36T is implemented with GSI's high performance CMOS technology and is available in a JEDEC-standard 100-pin TQFP package.

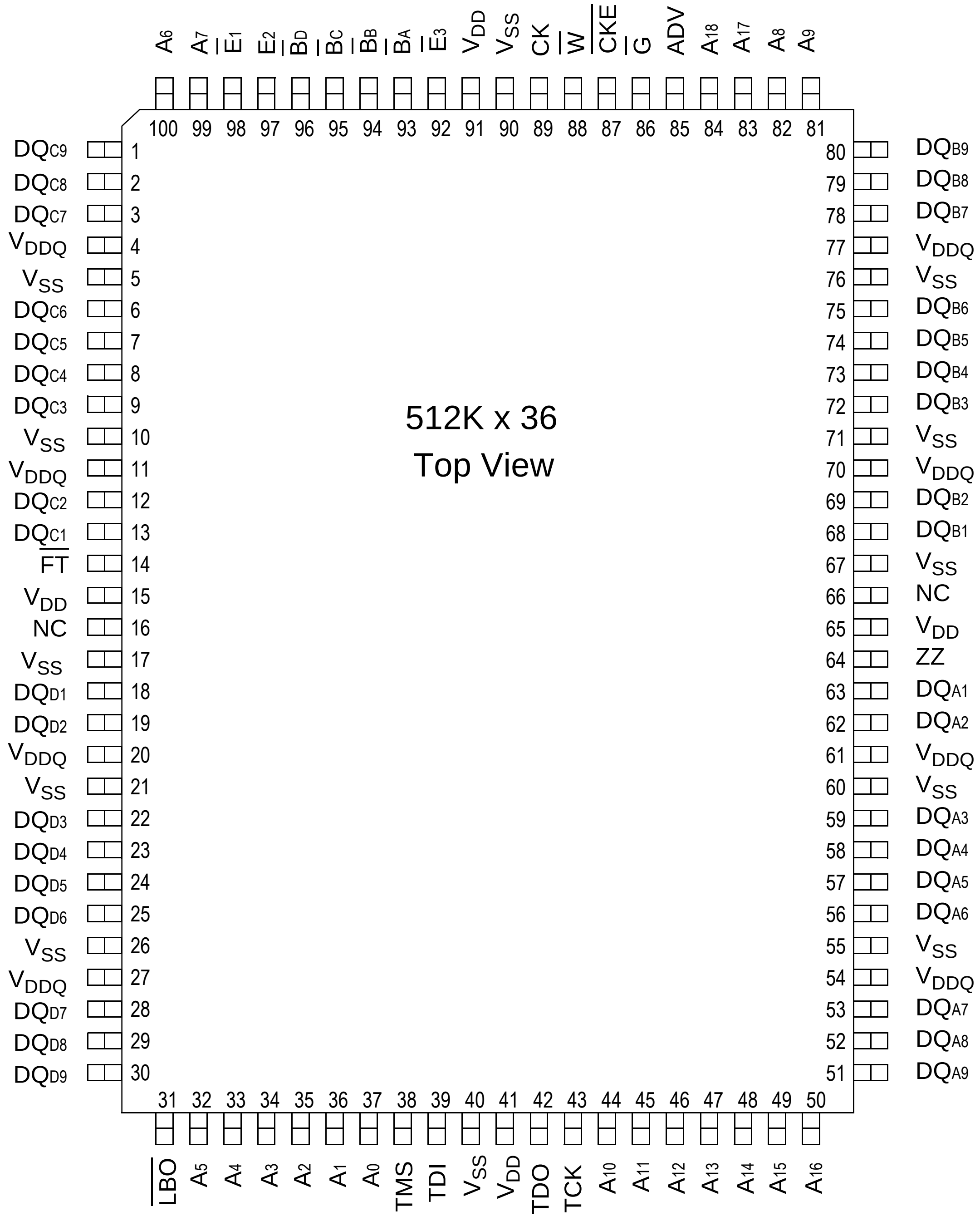
Flow Through and Pipelined NBT SRAM Back-to-Back Read/Write Cycles



GS8161Z18T Pinout



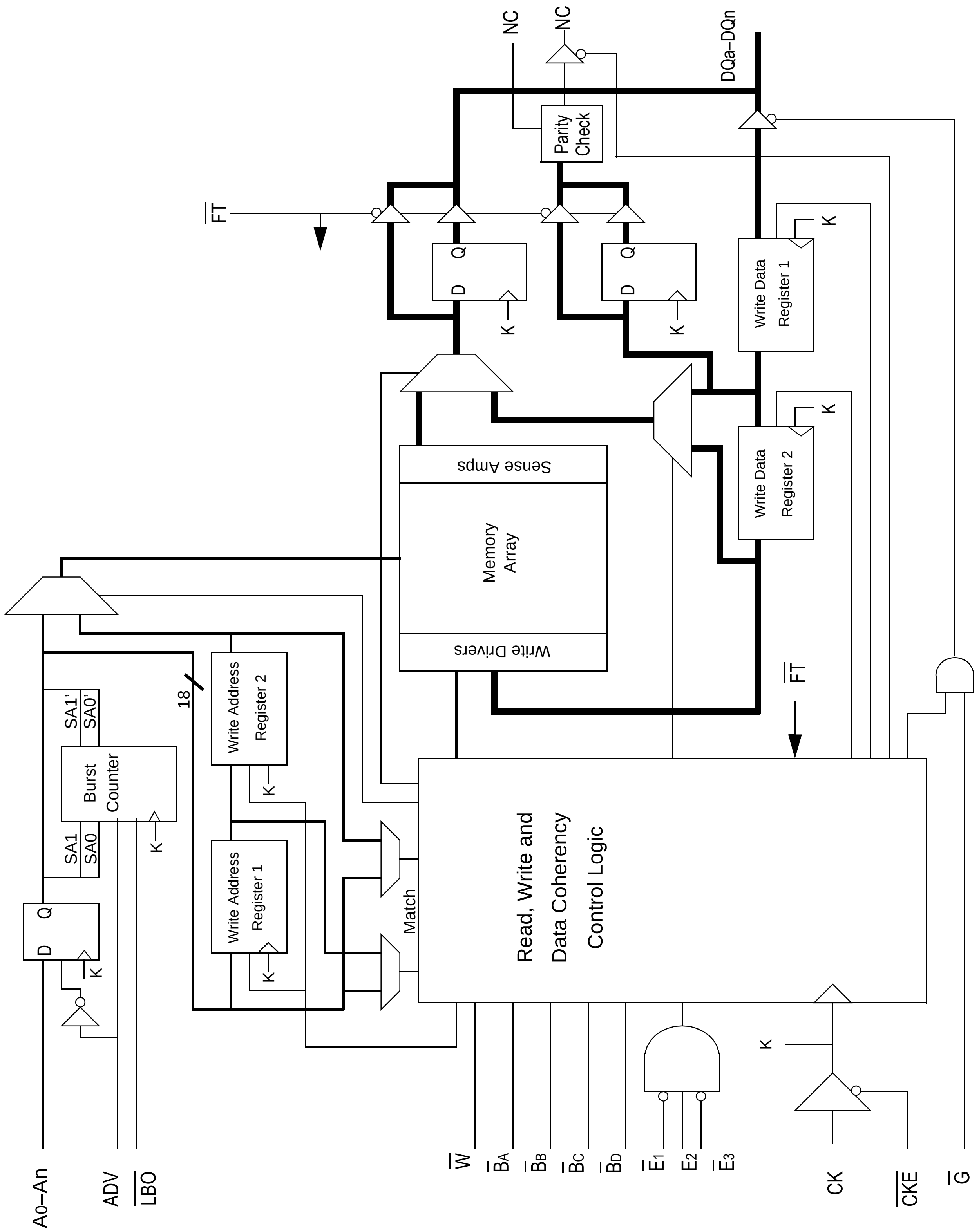
GS8161Z36T Pinout



100-Pin TQFP Pin Descriptions

Pin Location	Symbol	Type	Description
37, 36	A_0, A_1	In	Burst Address Inputs; Preload the burst counter
35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46,47, 48, 49, 50, 83, 84	A_2–A_{18}	In	Address Inputs
80	A_{19}	In	Address Input (x18 Version Only)
89	CK	In	Clock Input Signal
93	$\overline{B}_A$	In	Byte Write signal for data inputs DQ_{A1}–DQ_{A9}; active low
94	$\overline{B}_B$	In	Byte Write signal for data inputs DQ_{B1}–DQ_{B9}; active low
95	$\overline{B}_C$	In	Byte Write signal for data inputs DQ_{C1}–DQ_{C9}; active low (x36 Version Only)
96	$\overline{B}_D$	In	Byte Write signal for data inputs DQ_{D1}–DQ_{D9}; active low (x36 Version Only)
88	$\overline{W}$	In	Write Enable; active low
98	$\overline{E}_1$	In	Chip Enable; active low
97	E_2	In	Chip Enable—Active High. For self decoded depth expansion
92	$\overline{E}_3$	In	Chip Enable—Active Low. For self decoded depth expansion
86	$\overline{G}$	In	Output Enable; active low
85	ADV	In	Advance/$\overline{\text{Load}}$; Burst address counter control pin
87	$\overline{\text{CKE}}$	In	Clock Input Buffer Enable; active low
58, 59, 62,63, 68, 69, 72, 73, 74	DQ_{A1}–DQ_{A9}	I/O	Byte A Data Input and Output pins (x18 Version Only)
8, 9, 12, 13, 18, 19, 22, 23, 24	DQ_{B1}–DQ_{B9}	I/O	Byte B Data Input and Output pins (x18 Version Only)
16, 66	NC	—	No Connect
51, 52, 53, 56, 57, 75, 78, 79, 95, 96, 1, 2, 3, 6, 7, 25, 28, 29, 30	NC	—	No Connect (x18 Version Only)
63, 62, 59, 58, 57, 56, 53, 52, 51	DQ_{A1}–DQ_{A9}	I/O	Byte A Data Input and Output pins (x36 Version Only)
68, 69, 72, 73, 74, 75, 78, 79, 80	DQ_{B1}–DQ_{B9}	I/O	Byte B Data Input and Output pins (x36 Version Only)
13, 12, 9, 8, 7, 6, 3, 2, 1	DQ_{C1}–DQ_{C9}	I/O	Byte C Data Input and Output pins (x36 Version Only)
18, 19, 22, 23, 24, 25, 28, 29, 30	DQ_{D1}–DQ_{D9}	I/O	Byte D Data Input and Output pins (x36 Version Only)
64	ZZ	In	Power down control; active high
14	$\overline{\text{FT}}$	In	Pipeline/Flow Through Mode Control; active low
31	$\overline{\text{LBO}}$	In	Linear Burst Order; active low.
15, 41, 65, 91	V_{DD}	In	Core power supply
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V_{SS}	In	Ground
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	In	Output driver power supply

GS8161Z18/36 NBT SRAM Functional Block Diagram



Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{CKE}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst $\overline{Order}$ and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/$\overline{Load}$ pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2 and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte "a"	L	L	H	H	H
Write Byte "b"	L	H	L	H	H
Write Byte "c"	L	H	H	L	H
Write Byte "d"	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{CKE}$ is asserted low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active and the write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ & $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a read cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

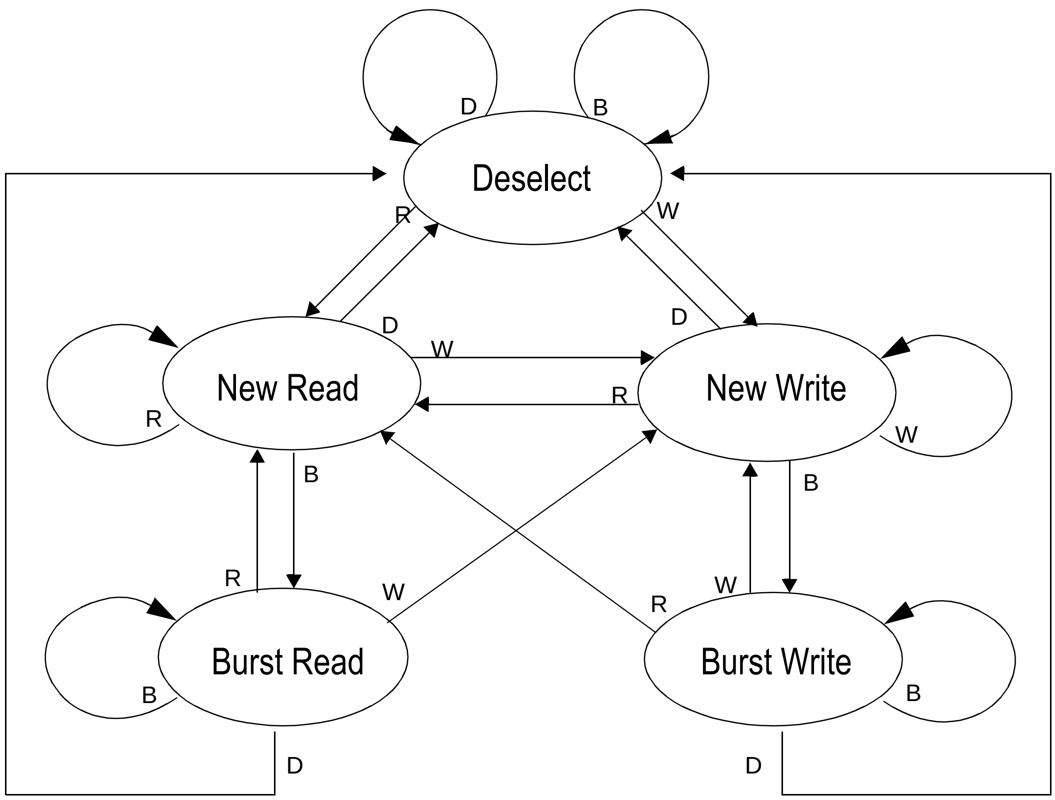
Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

Synchronous Truth Table

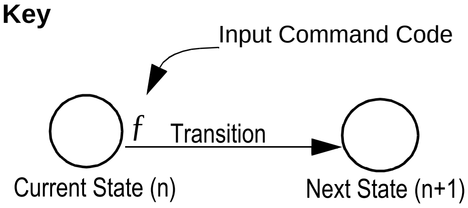
Operation	Type	Address	$\overline{E_1}$	E_2	$\overline{E_3}$	ZZ	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{G}$	$\overline{CKE}$	CK	DQ	Notes
Deselect Cycle, Power Down	D	None	H	X	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	X	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	D	None	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
Read Cycle, Begin Burst	R	External	L	H	L	L	L	H	X	L	L	L-H	Q	
Read Cycle, Continue Burst	B	Next	X	X	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/Read, Begin Burst	R	External	L	H	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy Read, Continue Burst	B	Next	X	X	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L	H	L	L	L	L	L	X	L	L-H	D	3
Write Cycle, Continue Burst	B	Next	X	X	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/Write Abort, Begin Burst	W	None	L	H	L	L	L	L	H	X	L	L-H	High-Z	2,3
Write Abort, Continue Burst	B	Next	X	X	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ignore, Stall		Current	X	X	X	L	X	X	X	X	H	L-H	-	4
Sleep Mode		None	X	X	X	H	X	X	X	X	X	X	High-Z	

Notes:
1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOP's because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active so no Write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during Write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined Read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a Write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

Pipelined and Flow Through Read Write Control State Diagram

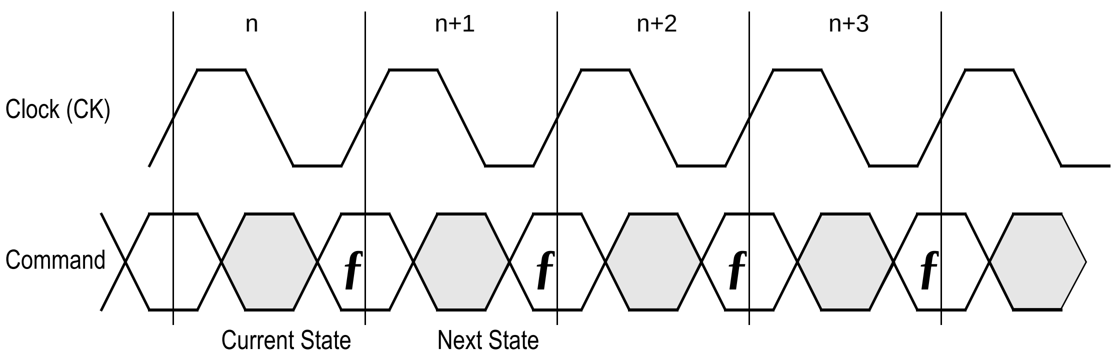


Key



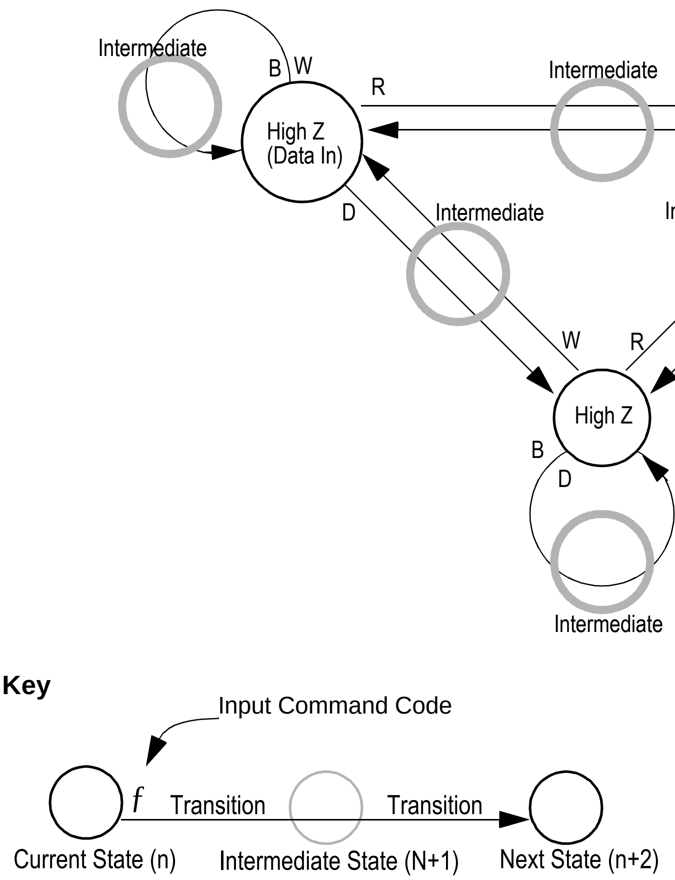
Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Synchronous Truth Table.



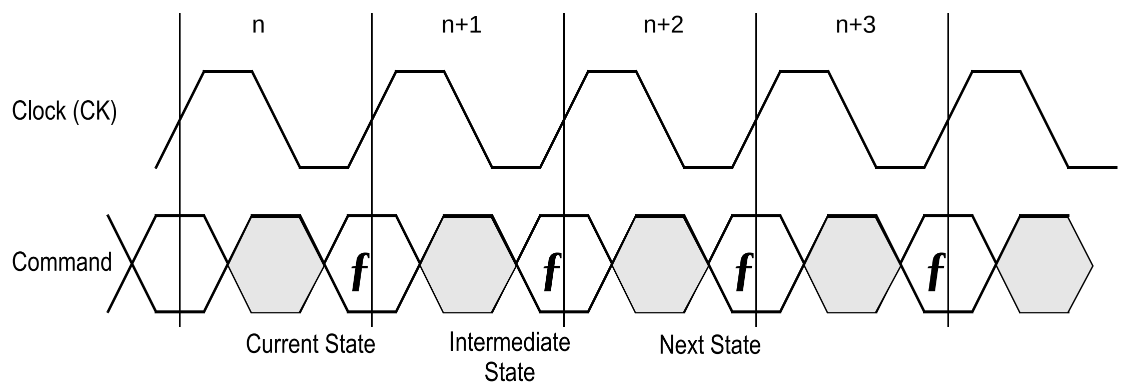
Current State and Next State Definition for Pipelined and Flow Through Read/Write Control State Diagram

Pipeline Mode Data I/O State Diagram



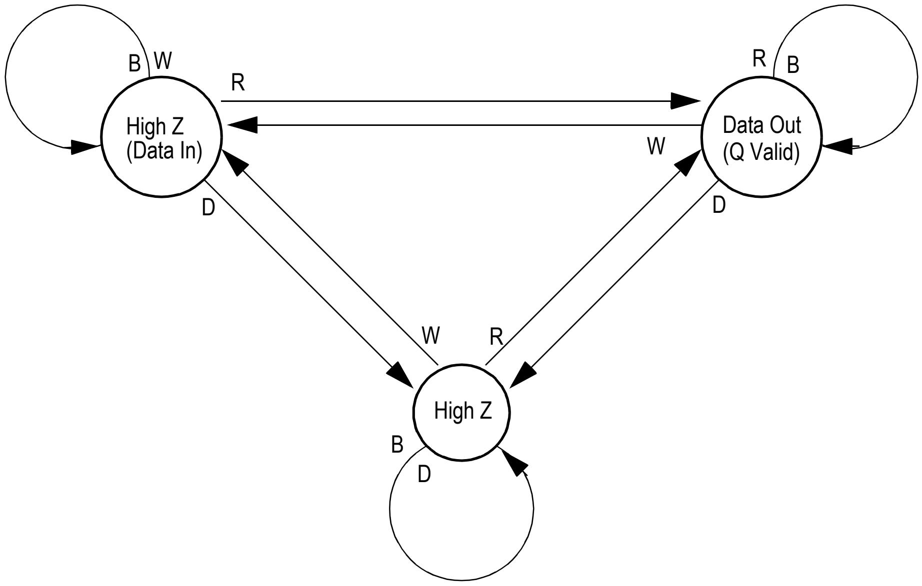
Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

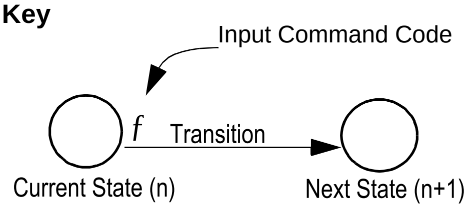


Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

Flow Through Mode Data I/O State Diagram



Key



Notes:

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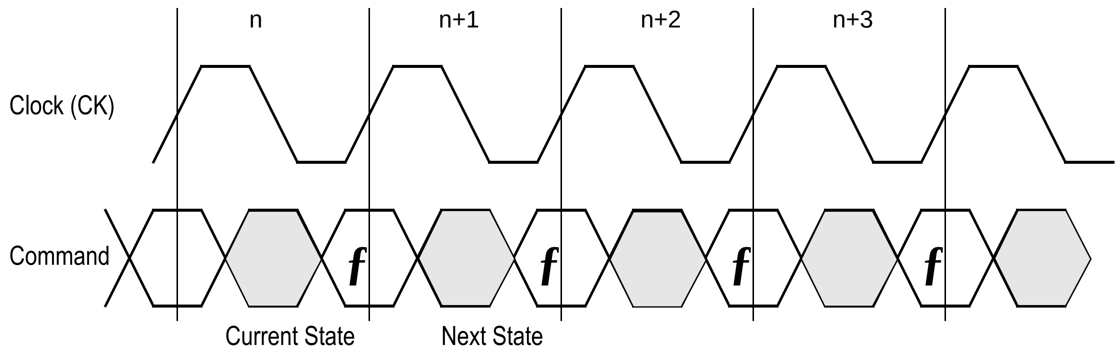
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow through Read Write Control State Diagram

Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{LBO}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There are pull-up devices on the $\overline{FT}$ pin and a pull-down device on the ZZ pin, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

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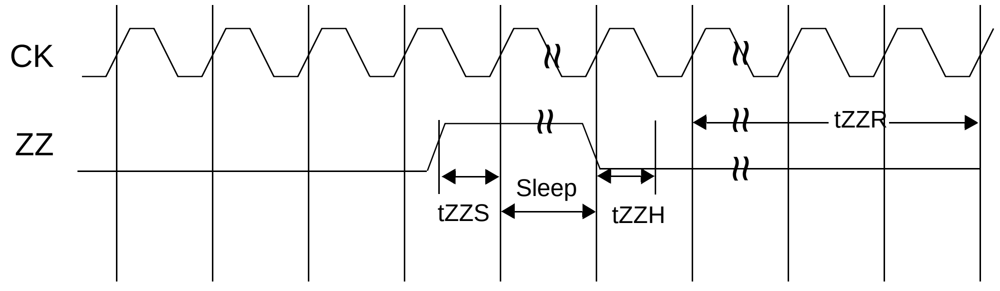
Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipelinemode via the $\overline{FT}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	2.7	V	

Notes:
1. The part numbers of Industrial Temperature Range versions end the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	2.0	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.8	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	2.0	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.8	V	1,3

Notes:
1. The part numbers of Industrial Temperature Range versions end the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	0.6*V_{DD}	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.3*V_{DD}	V	1,3

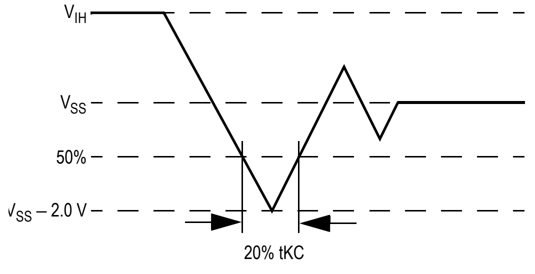
Notes:
1. The part numbers of Industrial Temperature Range versions end the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

Recommended Operating Temperatures

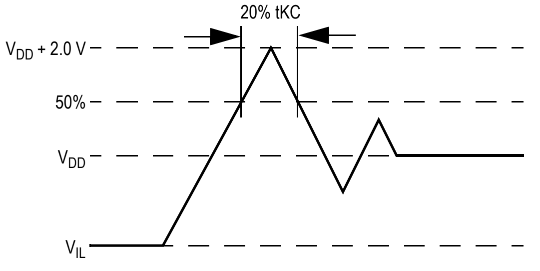
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Note:
1. The part numbers of Industrial Temperature Range versions end the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

($T_A = 25^oC$, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

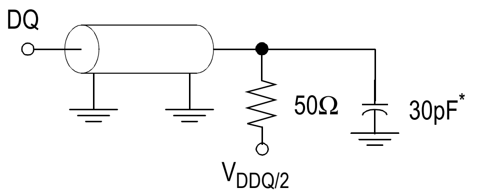
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DDQ}/2$
Output load	**Fig. 1**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Output Load 1



* Distributed Test Jig Capacitance

DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
ZZ Input Current	I_{IN1}	$V_{DD} \ge V_{IN} \ge V_{IH}$ $0\ V \le V_{IN} \le V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$ Input Current	I_{IN2}	$V_{DD} \ge V_{IN} \ge V_{IL}$ $0\ V \le V_{IN} \le V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

Operating Currents

Parameter	Test Conditions	Mode		Symbol	-250		-225		-200		-166		-150		-133		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current **3.3 V**	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x36)**	Pipeline	I_{DD} I_{DDQ}	290 40	300 40	265 35	275 35	240 30	250 30	205 25	215 25	190 25	200 25	170 20	180 20	mA
		(x36)	Flow Through	I_{DD} I_{DDQ}	180 20	190 20	170 20	180 20	165 15	175 15	155 15	165 15	150 15	160 15	140 10	150 10	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	260 20	270 20	235 20	245 20	215 15	225 15	185 15	195 15	170 15	180 15	155 10	165 10	mA
		(x18)	Flow Through	I_{DD} I_{DDQ}	165 10	175 10	155 10	165 10	150 10	160 10	140 10	150 10	135 10	145 10	125 10	135 10	mA
Operating Current **2.5 V**	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	**(x36)**	Pipeline	I_{DD} I_{DDQ}	290 30	300 30	265 30	275 30	240 25	250 25	205 20	215 20	190 20	200 20	170 15	180 15	mA
		(x36)	Flow Through	I_{DD} I_{DDQ}	180 20	190 20	170 20	180 20	165 15	175 15	155 15	165 15	150 15	160 15	140 10	150 10	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	260 15	270 15	235 15	245 15	215 15	225 15	185 10	195 10	170 10	180 10	155 10	165 10	mA
		(x18)	Flow Through	I_{DD} I_{DDQ}	165 10	175 10	155 10	165 10	150 10	160 10	140 10	150 10	135 10	145 10	125 10	135 10	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	mA
		—	Flow Through	I_{SB}	20	30	20	30	20	30	20	30	20	30	20	30	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	85	90	80	85	75	80	64	70	60	65	50	55	mA
		—	Flow Through	I_{DD}	60	65	60	65	50	55	50	55	50	55	45	50	mA

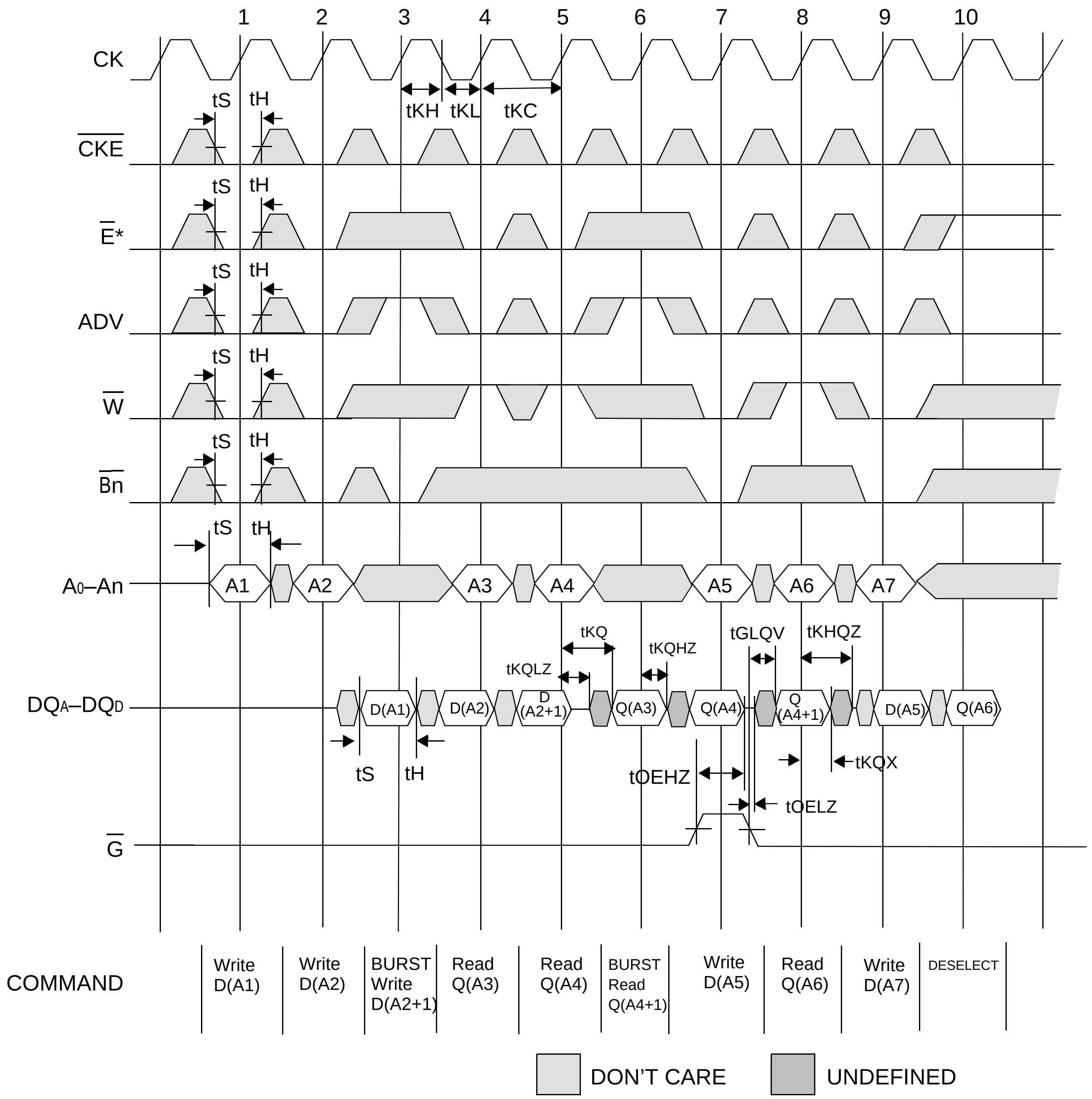
Notes:
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

AC Electrical Characteristics

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	2.5	—	2.7	—	3.0	—	3.4	—	3.8	—	4.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	1.2	—	1.3	—	1.4	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.2	—	0.3	—	0.4	—	0.5	—	0.5	—	0.5	—	ns
Flow Through	Clock Cycle Time	tKC	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	—	ns
	Clock to Output Valid	tKQ	—	5.5	—	6.0	—	6.5	—	7.0	—	7.5	—	8.5	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.3	—	2.5	—	3.0	—	3.0	—	3.0	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	20	—	20	—	20	—	ns

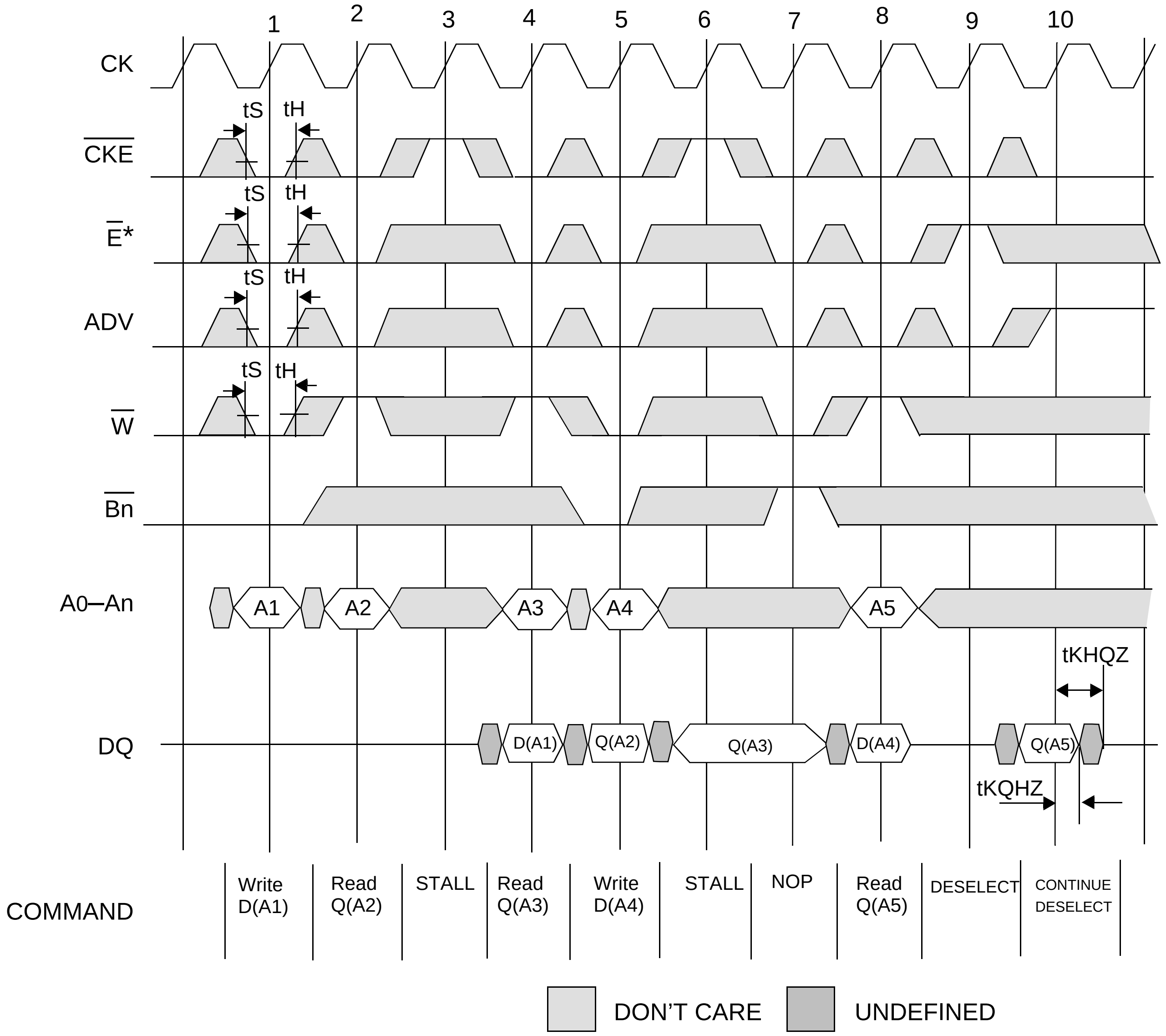
Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

Pipeline Mode Read/Write Cycle Timing



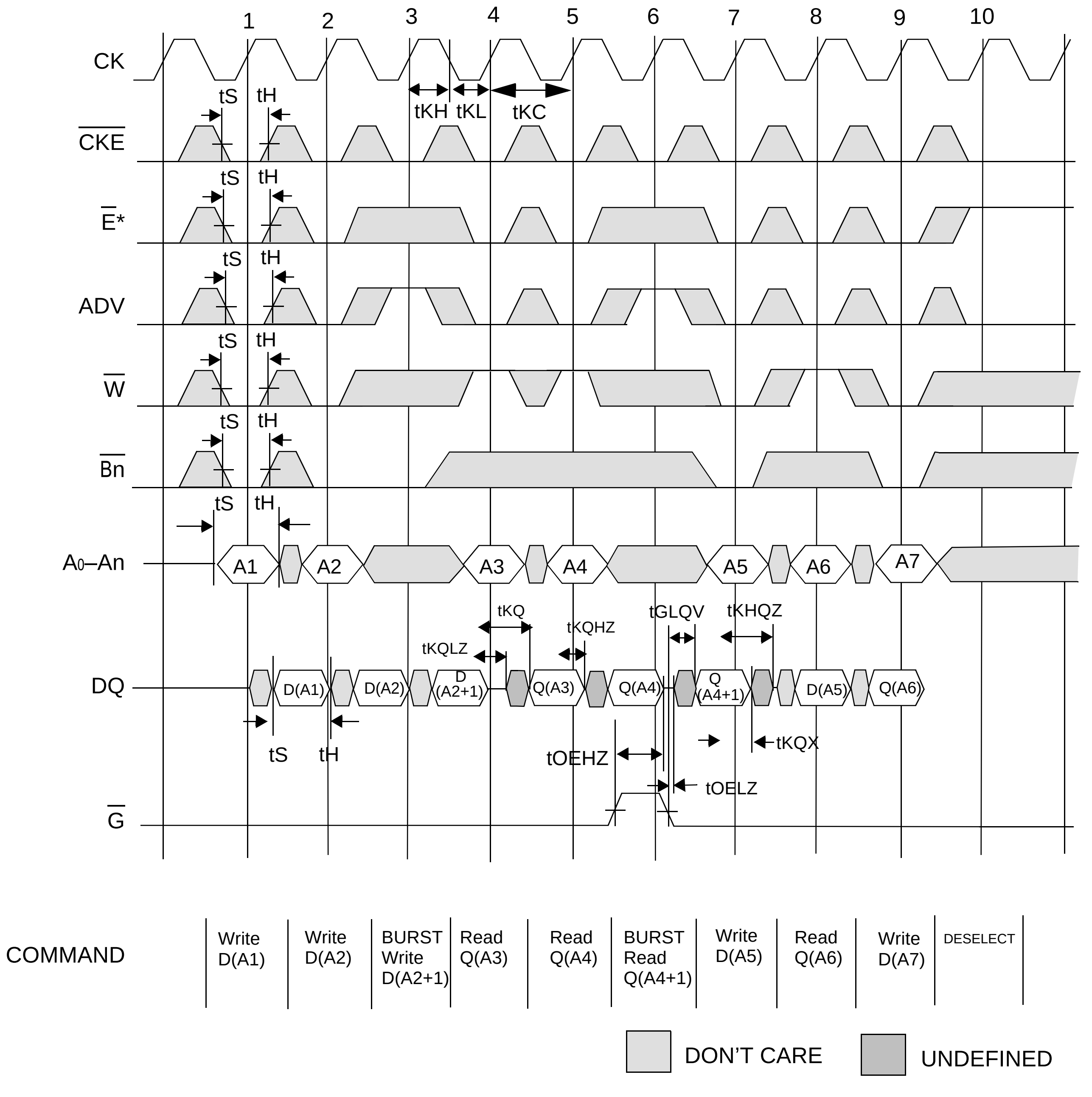
*Note: $\overline{E}$ = High (False) if $\overline{E}_1 = 1$ or $E_2 = 0$ or $\overline{E}_3 = 1$

Pipeline Mode No-Op, Stall and Deselect Timing



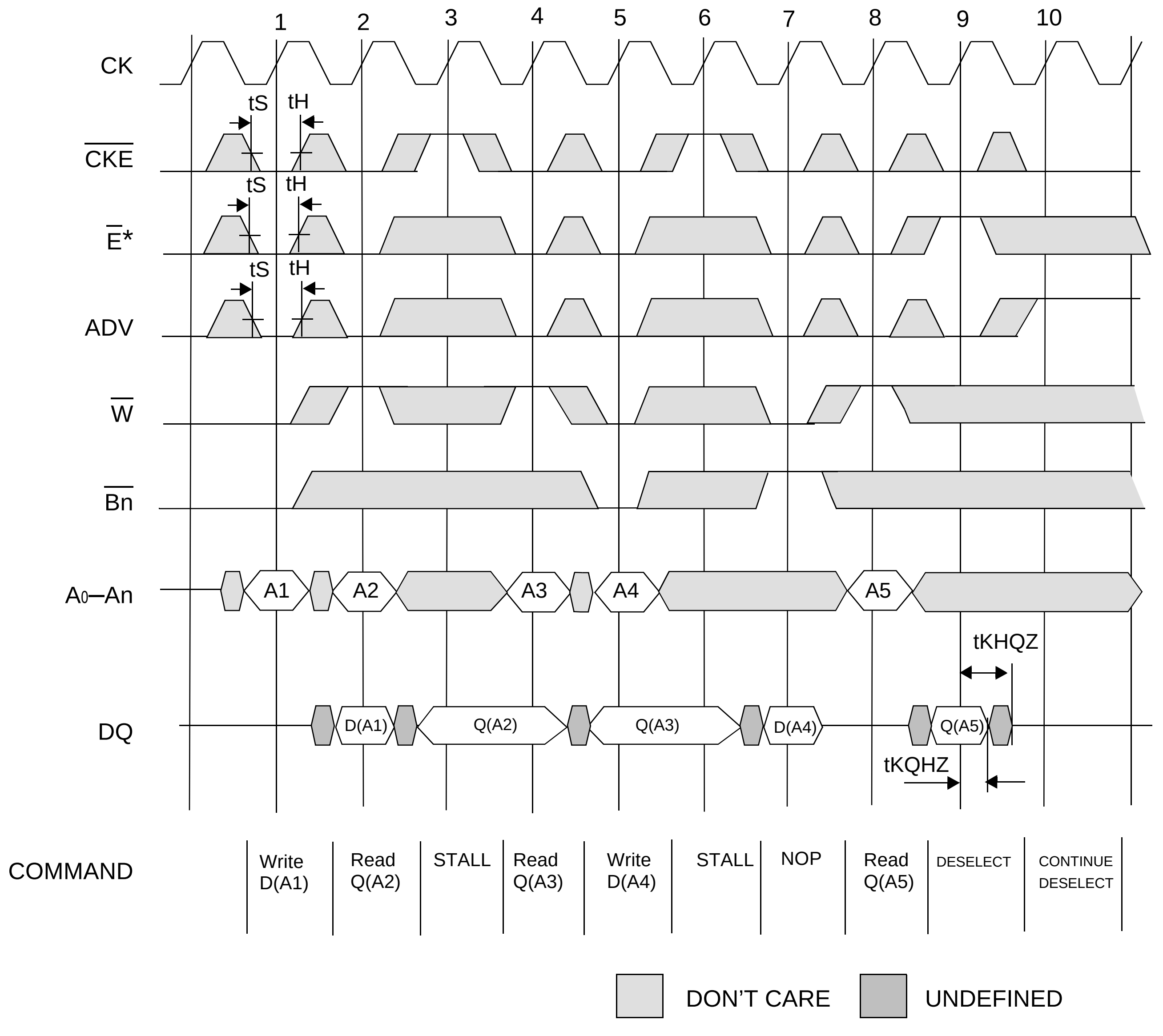
*Note: $\overline{E}$ = High (False) if $\overline{E}_1 = 1$ or $E_2 = 0$ or $\overline{E}_3 = 1$

Flow Through Mode Read/Write Cycle Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1 = 1$ or $E_2 = 0$ or $\overline{E}_3 = 1$

Flow Through Mode No-Op, Stall and Deselect Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1$ = 1 or E_2 = 0 or $\overline{E}_3$ = 1

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

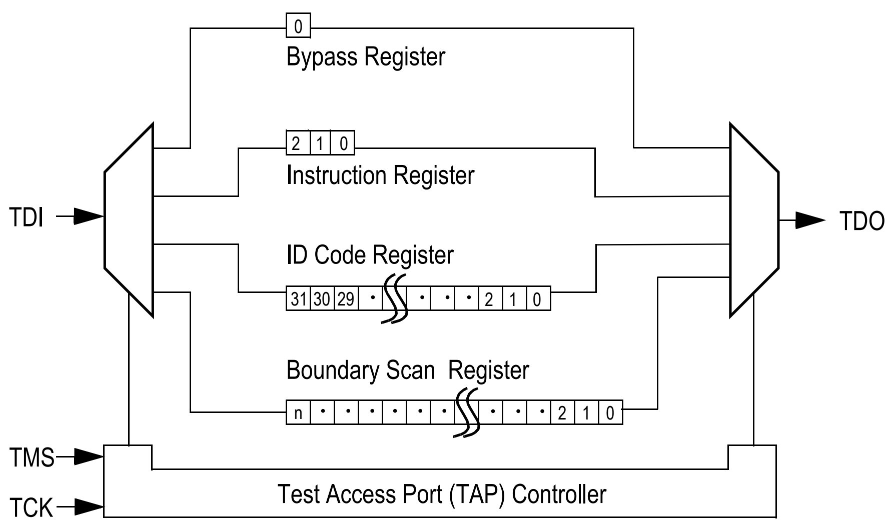
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM’s input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port’s TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1

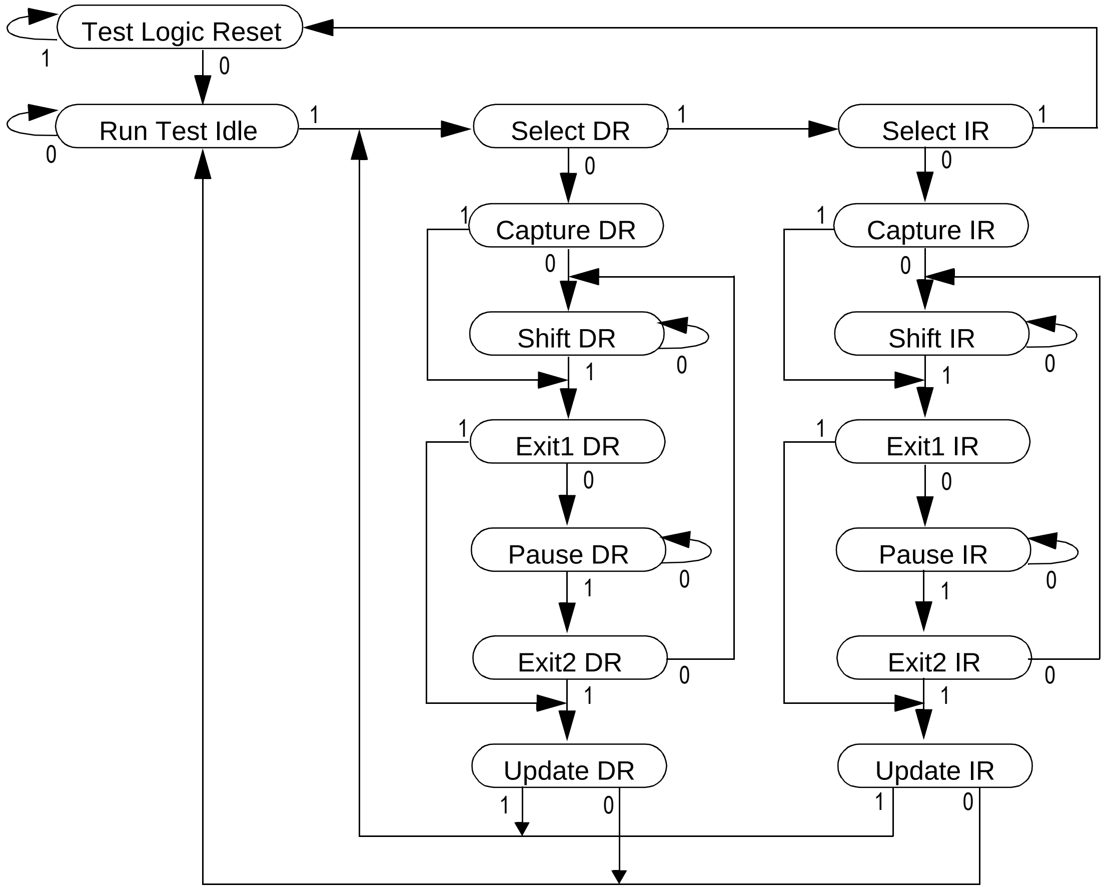
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

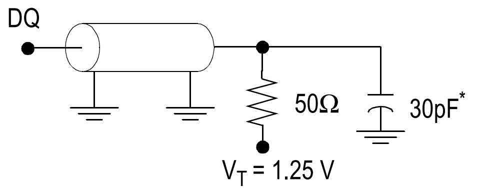
Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	V_{DD3} +0.3	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	–0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	0.6 * V_{DD2}	V_{DD2} +0.3	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	–0.3	0.3 * V_{DD2}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:
1. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn} +2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \le V_{IN} \le V_{DDn}$
3. $0 V \le V_{IN} \le V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OHJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V

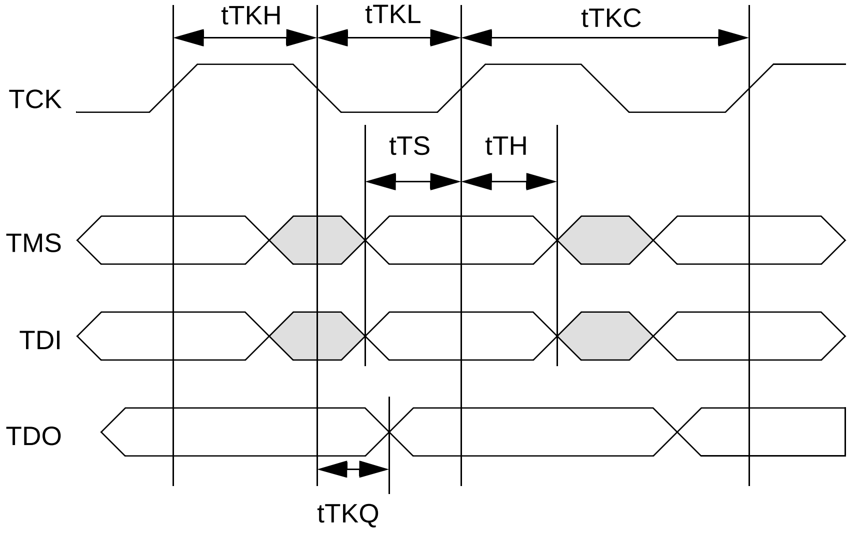
JTAG Port AC Test Load



* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as as shown unless otherwise noted.

JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
1	PH = 0		n/a	
2	X		n/a	
3	X		n/a	
4	A_{10}		44	
5	A_{11}		45	
6	A_{12}		46	
7	A_{13}		47	
8	A_{14}		48	
9	A_{15}		49	
10	A_{16}		50	
11	Q_{A9}	NC = 1	51	n/a
12	D_{A9}	PH = 0	51	n/a
13	NC = 1		n/a	
14	PH = 0		n/a	
15	Q_{A8}	NC = 1	52	n/a
16	D_{A8}	PH = 0	52	n/a
17	PH = 0	NC = 1	n/a	
18	PH = 0		n/a	
19	Q_{A7}	NC = 1	53	n/a
20	D_{A7}	PH = 0	53	n/a
21	NC = 1		n/a	
22	PH = 0		n/a	
23	Q_{A6}	NC = 1	56	n/a
24	D_{A6}	PH = 0	56	n/a
25	NC = 1		n/a	
26	PH = 0		n/a	
27	Q_{A5}	NC = 1	57	n/a
28	D_{A5}	PH = 0	57	n/a
29	NC = 1		n/a	

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
30	PH = 0		n/a	
31	Q_{A4}	Q_{A1}	58	
32	D_{A4}	D_{A1}	58	
33	NC = 1		n/a	
34	PH = 0		n/a	
35	Q_{A3}	Q_{A2}	59	
36	D_{A3}	D_{A2}	59	
37	NC = 1		n/a	
38	PH = 0		n/a	
39	Q_{A2}	Q_{A3}	62	
40	D_{A2}	D_{A3}	62	
41	NC = 1		n/a	
42	PH = 0		n/a	
43	Q_{A1}	Q_{A4}	63	
44	D_{A1}	D_{A4}	63	
45	NC = 1		n/a	
46	PH = 0		n/a	
47	ZZ		64	
48	PH = 0		n/a	
49	$\overline{QE}$		66	
50	Q_{B1}	Q_{A5}	68	
51	D_{B1}	D_{A5}	68	
52	NC = 1		n/a	
53	PH = 0		n/a	
54	Q_{B2}	Q_{A6}	69	
55	D_{B2}	D_{A6}	69	
56	NC = 1		n/a	
57	PH = 0		n/a	
58	Q_{B3}	Q_{A7}	72	

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
59	D_{B3}	D_{A7}	72	
60	NC = 1		n/a	
61	PH = 0		n/a	
62	Q_{B4}	Q_{A8}	73	
63	D_{B4}	D_{A8}	73	
64	NC = 1		n/a	
65	PH = 0		n/a	
66	Q_{B5}	Q_{A9}	74	
67	D_{B5}	D_{A9}	74	
68	NC = 1		n/a	
69	PH = 0		n/a	
70	Q_{B6}	NC = 1	75	n/a
71	D_{B6}	PH = 0	75	n/a
72	NC = 1		n/a	
73	PH = 0		n/a	
74	Q_{B7}	NC = 1	78	n/a
75	D_{B7}	PH = 0	78	n/a
76	NC = 1		n/a	
77	PH = 0		n/a	
78	Q_{B8}	NC = 1	79	n/a
79	D_{B8}	PH = 0	79	n/a
80	NC = 1		n/a	
81	PH = 0		n/a	
82	Q_{B9}	NC = 1	80	n/a
83	D_{B9}	PH = 0	80	n/a
84	NC = 1		n/a	
85	PH = 0		n/a	
86	NC = 1	A_{19}	n/a	80
87	A_9		81	

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
88	A_8		82	
89	A_{17}		83	
90	A_{18}		84	
91	$\overline{ADV}$		85	
92	$\overline{G}$		86	
93	$\overline{CKE}$		87	
94	$\overline{W}$		88	
95	NC = 1		n/a	
96	NC = 1		n/a	
97	NC = 1		n/a	
98	NC = 1		n/a	
99	CK		89	
100	PH = 0		n/a	
101	PH = 0		n/a	
102	$\overline{E}_3$		92	
103	$\overline{B}_A$		93	
104	$\overline{B}_B$	NC = 1	94	n/a
105	$\overline{B}_C$	$\overline{B}_B$	95	
106	$\overline{B}_D$	NC = 1	96	n/a
107	E_2		97	
108	$\overline{E}_1$		98	
109	A_7		99	
110	A_6		100	
111	Q_{C9}	NC = 1	1	n/a
112	D_{C9}	PH = 0	1	n/a
113	NC = 1		n/a	
114	PH = 0		n/a	
115	Q_{C8}	NC = 1	2	n/a
116	D_{C8}	PH = 0	2	n/a

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
117	NC = 1		n/a	
118	PH = 0		n/a	
119	Q_{C7}	NC = 1	3	n/a
120	D_{C7}	PH = 0	3	n/a
121	NC = 1		n/a	
122	PH = 0		n/a	
123	Q_{C6}	NC = 1	6	n/a
124	D_{C6}	PH = 0	6	n/a
125	NC = 1		n/a	
126	PH = 0		n/a	
127	Q_{C5}	NC = 1	7	n/a
128	D_{C5}	PH = 0	7	n/a
129	NC = 1		n/a	
130	PH = 0		n/a	
131	Q_{C4}	Q_{B1}	8	
132	D_{C4}	D_{B1}	8	
133	NC = 1		n/a	
134	PH = 0		n/a	
135	Q_{C3}	Q_{B2}	9	
136	D_{C3}	D_{B2}	9	
137	NC = 1		n/a	
138	PH = 0		n/a	
139	Q_{C2}	Q_{B3}	12	
140	D_{C2}	D_{B3}	12	
141	NC = 1		n/a	
142	PH = 0		n/a	
143	Q_{C1}	Q_{B4}	13	
144	D_{C1}	D_{B4}	13	
145	NC = 1		n/a	

GS8161Z18/36 Boundary Scan Chain Order

Order	x36	x18	Pin	
			x36	x18
146	PH = 0		n/a	
147	$\overline{FT}$		14	
148	DP		16	
149	NC = 1		n/a	
150	Q_{D8}	Q_{B5}	18	
151	D_{D8}	D_{B5}	18	
152	NC = 1		n/a	
153	PH = 0		n/a	
154	Q_{D7}	Q_{B6}	19	
155	D_{D7}	D_{B6}	19	
156	NC = 1		n/a	
157	PH = 0		n/a	
158	Q_{D6}	Q_{B7}	22	
159	D_{D6}	D_{B7}	22	
160	NC = 1		n/a	
161	PH = 0		n/a	
162	Q_{D5}	Q_{B8}	23	
163	D_{D5}	D_{B8}	23	
164	NC = 1		n/a	
165	PH = 0		n/a	
166	Q_{D4}	Q_{B9}	24	
167	D_{D4}	D_{B9}	24	
168	NC = 1		n/a	
169	PH = 0		n/a	
170	Q_{D3}	NC = 1	25	n/a
171	D_{D3}	PH = 0	25	n/a
172	NC = 1		n/a	
173	PH = 0		n/a	
174	Q_{D2}	NC = 1	28	n/a

GS8161Z18/36 Boundary Scan Chain Order

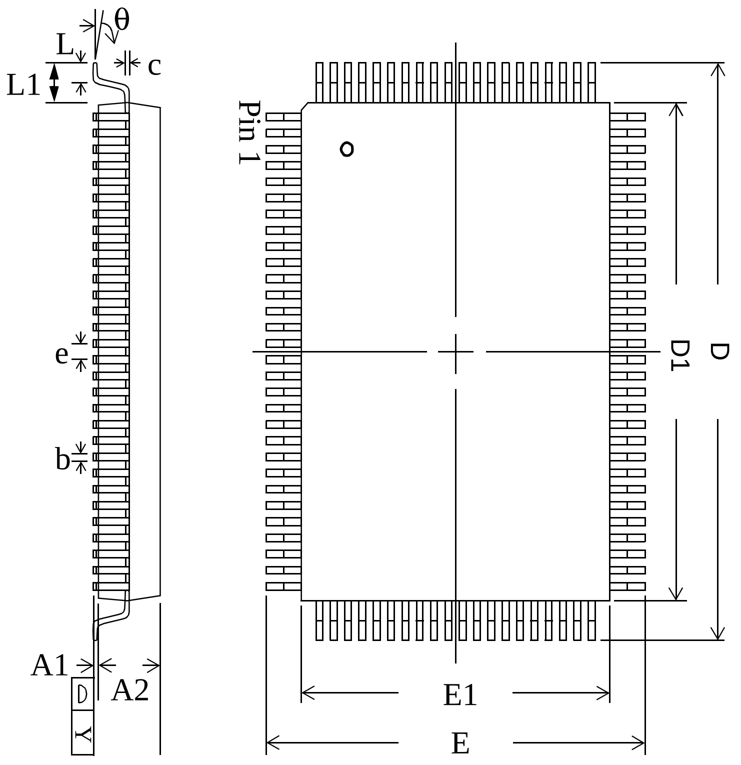
Order	x36	x18	Pin x36	Pin x18
175	D_{D2}	PH = 0	28	n/a
176	NC = 1		n/a	
177	PH = 0		n/a	
178	Q_{D1}	NC = 1	29	n/a
179	D_{D1}	PH = 0	29	n/a
180	NC = 1		n/a	
181	PH = 0		n/a	
182	Q_{D9}	NC = 1	30	n/a
183	D_{D9}	PH = 0	30	n/a
184	NC = 1		n/a	
185	PH = 0		n/a	
186	$\overline{LBO}$		31	
187	A_5		32	
188	A_4		33	
189	A_3		34	
190	A_2		35	
191	A_1		36	
192	A_0		37	
193	PH = 0		n/a	
194	$\overline{G}$		86	

Notes:
1. Depending on the package, some input pads of the scan chain may not be connected to any external pin. In such case: $\overline{LBO}$ = 1, ZQ = 1, $\overline{PE}$ = 0, $\overline{SD}$ = 0, ZZ = 0, $\overline{FT}$ = 1, DP = 1, and SCD = 1.
2. Every DQ pad consists of two scan registers—D is for input capture, and Q is for output capture.
3. A single register (#194) for controlling tristate of all the DQ pins is at the end of the scan chain (i.e., the last bit shifted in this tristate control is effective after JTAG EXTEST instruction is executed.
4. 1 = no connect, internally set to logic value 1
5. 0 = no connect, internally set to logic value 0
6. X = no connect, value is undefined

TQFP Package Drawing

TQFP Package Drawing

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09		0.20
D	Terminal Dimension	21.9	22.0	20.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch		0.65	
L	Foot Length	0.45	0.60	0.75
L1	Lead Length		1.00	
Y	Coplanarity			0.10
θ	Lead Angle	0°		7°



Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

BPR 1999.05.18

Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]	Status
1M x 18	GS8161Z18T-250	NBT Pipeline/Flow Through	TQFP	250/5.5	C	
1M x 18	GS8161Z18T-225	NBT Pipeline/Flow Through	TQFP	225/6	C	
1M x 18	GS8161Z18T-200	NBT Pipeline/Flow Through	TQFP	200/6.5	C	
1M x 18	GS8161Z18T-166	NBT Pipeline/Flow Through	TQFP	166/7	C	
1M x 18	GS8161Z18T-150	NBT Pipeline/Flow Through	TQFP	150/7.5	C	
1M x 18	GS8161Z18T-133	NBT Pipeline/Flow Through	TQFP	133/8.5	C	
512K x 36	GS8161Z36T-250	NBT Pipeline/Flow Through	TQFP	250/5.5	C	
512K x 36	GS8161Z36T-225	NBT Pipeline/Flow Through	TQFP	225/6	C	
512K x 36	GS8161Z36T-200	NBT Pipeline/Flow Through	TQFP	200/6.5	C	
512K x 36	GS8161Z36T-166	NBT Pipeline/Flow Through	TQFP	166/7	C	
512K x 36	GS8161Z36T-150	NBT Pipeline/Flow Through	TQFP	150/7.5	C	
512K x 36	GS8161Z36T-133	NBT Pipeline/Flow Through	TQFP	133/8.5	C	
1M x 18	GS8161Z18T-250I	NBT Pipeline/Flow Through	TQFP	250/5.5	I	Not Available
1M x 18	GS8161Z18T-225I	NBT Pipeline/Flow Through	TQFP	225/6	I	Not Available
1M x 18	GS8161Z18T-200I	NBT Pipeline/Flow Through	TQFP	200/6.5	I	Not Available
1M x 18	GS8161Z18T-166I	NBT Pipeline/Flow Through	TQFP	166/7	I	
1M x 18	GS8161Z18T-150I	NBT Pipeline/Flow Through	TQFP	150/7.5	I	
1M x 18	GS8161Z18T-133I	NBT Pipeline/Flow Through	TQFP	133/8.5	I	
512K x 36	GS8161Z36T-250I	NBT Pipeline/Flow Through	TQFP	250/5.5	I	Not Available
512K x 36	GS8161Z36T-225I	NBT Pipeline/Flow Through	TQFP	225/6	I	Not Available
512K x 36	GS8161Z36T-200I	NBT Pipeline/Flow Through	TQFP	200/6.5	I	Not Available
512K x 36	GS8161Z36T-166I	NBT Pipeline/Flow Through	TQFP	166/7	I	
512K x 36	GS8161Z36T-150I	NBT Pipeline/Flow Through	TQFP	150/7.5	I	
512K x 36	GS8161Z36T-133I	NBT Pipeline/Flow Through	TQFP	133/8.5	I	

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS816Z36-166IT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user .
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

18Mb Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	**Types of Changes Format or Content**	**Page;Revisions;Reason**
GS18/36 1.00 9/ 1999A;GS18/362.0012/ 1999B	Content	• Converted from 0.25u 3.3V process to 0.18u 2.5V process. Master File Rev B • Added x72 Pinout.
GS18/362.00 12/ 1999BGS18/362.01 1/2000C	Format	• Added new GSI Logo
GS18/362.0 1/2000DGS18/ 362.03 2/2000E		• Front page; Features - changed 2.5V I/O supply to 2.5V or3.3V I/O supply; Completeness • Absolute Maximum Ratings; Changed VDDQ - Value: From: -.05 to VDD : to : -.05 to 3.6; Completeness. • Recommended Operating Conditions;Changed: I/O Supply Voltage- Max. from VDD to 3.6; Input High Voltage- Max. from VDD +0.3 to 3.6; Same page - took out Note 1;Completeness • Electrical Characteristics - Added second Output High Voltage line to table; completeness. • Note: There was not a Rev 2.02 for the 8160Z or the 8161Z.
GS18/362.03 2/2000E; 8161Z18_r2_04	Content	• Pin 14 removed from V_{SS} in pin description table. • ADV changed to pin 85 in pin description table.
8161Z18_r2_04; 8161Z18_r2_05	Content	• Changed the value of ZZ recovery in the AC Electrical Characteristics table on page 18 from 20 ns to 100 ns
8161Z18_r2_05; 8161Z18_r2_06	Content/Format	• Added 225 MHz speed bin • Updated page 1 table, AC Characteristics table, and Operating Currents table • Updated format to comply with Technical Publications standards • Updated Capitance table—removed Input row and updated Output row to I/O
8161Z18_r2_06; 8161Z18_r2_07	Content	• Updated Features list on page 1 • Completely reworked table on page 1 • Updated Mode Pin Functions on page 12
8161Z18_r2_07; 8161Z18_r2_08	Content	• Added 3.3 V references to entire document • Updated Operating Conditions table • Updated JTAG Operating Conditions table • Updated Boundary Scan Chain table • Updated Opearting Currents table and added note • Updated table on page 1; added power numbers

18Mb Sync SRAM Data Sheet Revision History

DS/DateRev. Code: Old; New	**Types of Changes Format or Content**	**Page;Revisions;Reason**
8161Z18_r2_08; 8161Z18_r2_09	Content	• Updated Pin Description table • Updated DQ on page 21 • Updated DQ on page 23 • Updated Operating Currrents table • Updated table on page 1; updated power numbers • Updated Recommended Operating Conditions table (added V_{DDQ} references)
8161Z18_r2_09; 8161Z18_r2_10	Content	• Updated table on page 1 • Created recommended operating conditions tables on pages 15 and 16 • Updated AC Electrical Characteristics table • Updated Ordering Information for 225 MHz part (changed from 7ns to 6.5 ns) • Updated BSR table (2 and 3 changed to X (value undefined)) • Added 250 MHz speed bin • Deleted 180 MHz speed bin
8161Z18_r2_10; 8161Z18_r2_11	Content	• Updated AC Characteristics table • Updated FT power numbers • Updated Mb references from 16Mb to 18Mb • Removed ByteSafe references • Changed DP and $\overline{QE}$ pins to NC • Updated ZZ recovery time diagram • Updated AC Test Conditions table and removed Output Load 2 diagram

