Using the GS9001 EDH Coprocessor

APPLICATION NOTE

INTRODUCTION

The GS9001 EDH coprocessor provides access to video timing signals in addition to implementing SMPTE RP165 error detection and handling (EDH). It provides the benefits of an I^2C interface as well as the capability to operate as a stand alone device.

The inclusion of an I^2C interface allows the GS9001 to communicate with other integrated circuits via a simple two wire interface. In this application note, the use of the GS9001 I^2C interface , and an overview of the I^2C bus is described. Some designs will not require the use of the GS9001 I^2C interface. In these systems, the use of the dedicated error flag outputs and video timing signals available from the GS9001 will be sufficient. Some basic applications are described for using the GS9001 in the stand alone mode.

OVERVIEW OF GS9001 FEATURES

A functional pinout of the GS9001 is shown in Figure 1.

Receive/Transmit Mode

The GS9001 can be configured for either RECEIVE or TRANSMIT mode of operation. The mode of operation is set by the logic level on the R/$\overline{T}$ pin of the GS9001.

The TRANSMIT mode inserts a valid CRC checkword into the EDH packet and resets all EDH flags. The TRANSMIT mode is typically used for source equipment, and does not allow any modification of the EDH flags.

In the RECEIVE mode of operation, the calculated CRC is compared to the incoming CRC embedded in the error data packet. The GS9001 will normally set the error flag that corresponds to the type of input error. The receive mode allows any of the fifteen EDH flags to be set/reset through flag masking, or to be left in the transparent mode.

Stand Alone Operation

In the standalone mode, the I^2C interface is not used, however, error flag outputs and all timing information is still available.

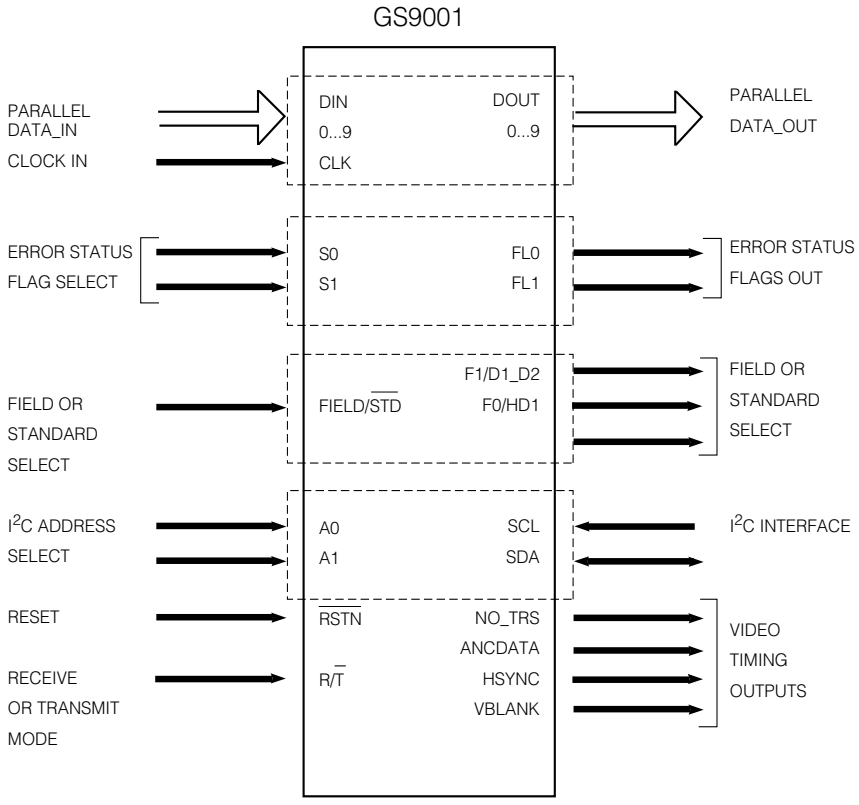

Fig. 1 GS9001 Functional Pinout

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The SCL and SDA pins of the GS9001 must be connected to the most negative supply to enable the stand alone mode. This ensures that noise on the SCL and SDA lines will not be interpreted as I^2C information, and allows the A_0 / A_1 pins to control the function of the ancillary data pin as shown in Table 1.

A_0 (pin 19)	A_1(pin 20)	ANC DATA PIN OUTPUT
0	0	ANC DATA PRESENT
0	1	TRS ID and ANC DATA PRESENT
1	0	ANC DATA PRESENT
1	1	ANC DATA PRESENT

Table 1. Function of ANC Data Pin during Stand Alone Mode

During the stand alone mode of operation, the following conditions apply:

- flag masking is disabled
- video standard override is disabled
- programmable interrupt is disabled

I^2C INTERFACE

The inclusion of an I^2C interface allows the GS9001 to communicate with other integrated circuits by means of a simple two wire interface. This interface provides access to the internal read and write memory maps of the GS9001. A brief summary of I^2C terminology is provided in Table 2.

I^2C TERM	DESCRIPTION
TRANSMITTER	A device which sends data to the bus
RECEIVER	A device which receives data from the bus
MASTER	A device which initiates and terminates a transfer. The master generates the clock
SLAVE	A device accessed by a master
START CONDITION	A high to low transition of the SDA line while SCL is high
STOP CONDITION	A low to high transition of the SDA line while SCL is high
ACKNOWLEDGE	Receiver pulls the SDA line low during the high period of SCL
NOT ACKNOWLEDGE	Receiver leaves the SDA line HIGH during the HIGH period of SCL

Table 2 Summary of I^2C Terminology

The I^2C format for transferring data to and from the GS9001 is shown in Figures 2 and 3 respectively.

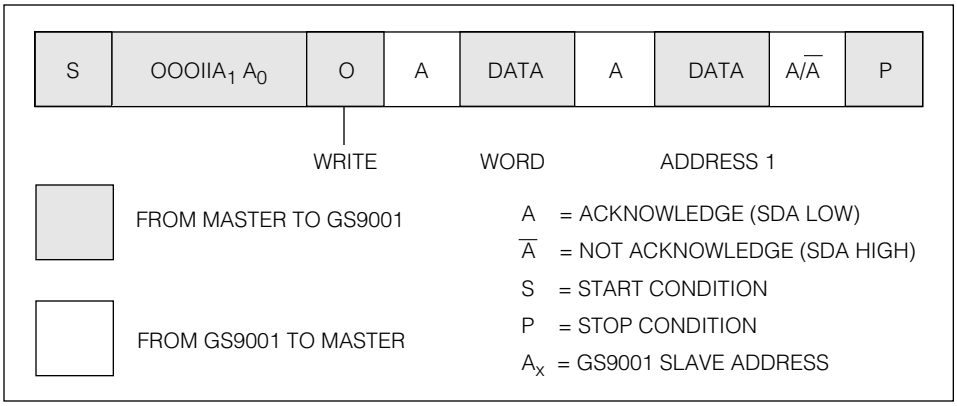


Fig. 2 GS9001 I^2C Write Format

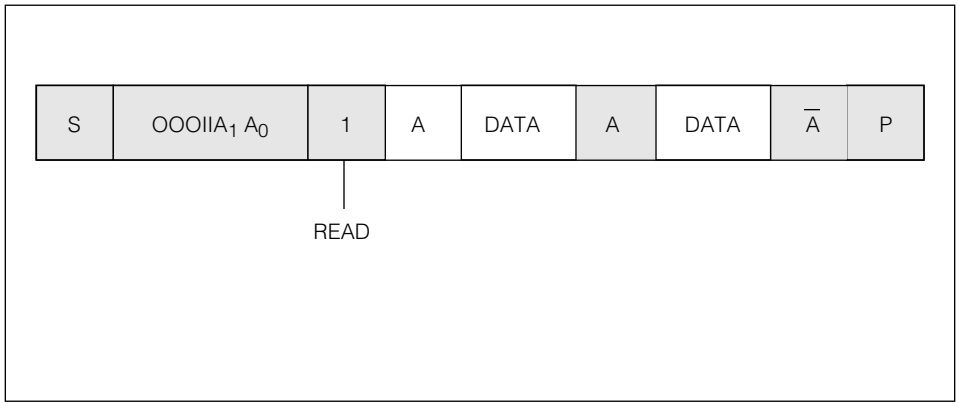


Fig. 3 GS9001 I^2C Read Format

Following a start condition, the GS9001's 7 bit address is transfered. The first five bits of the address is the GS9001 device address, while bits A_1 and A_0 select the slave sub-address. The I^2C slave address is set by the A0 and A1 pins of the GS9001.

Data is transfered over the GS9001 in an autoincrement format. The first data byte transfered always references WORD 1 in the GS9001 memory map. Following an acknowledge, the address is auto incremented and the next word is accessed until all 15 locations have been read. The auto increment counter operates as a circular pointer; an I^2C read/write operation after WORD 15 will return to WORD1.

The GS9001 I^2C interface will support both standard (100kbps) and fast (400kbps) mode access, provided proper bus loading is observed.

Example: Connecting More than Two GS9001's on the I^2C bus

Although the GS9001 has a total of four unique I^2C subaddresses, two subaddresses are dedicated for test and EDH passthrough modes. The test mode should not be used because the output pins are reconfigured when the TEST mode is selected. The EDH passthrough mode is provided to aid in system diagnostics, and does not update the EDH packet.

Because there are only 2 valid I^2C addresses on the GS9001, systems that require multiple devices will have to use selective addressing on the I^2C bus as shown in Figure 4.

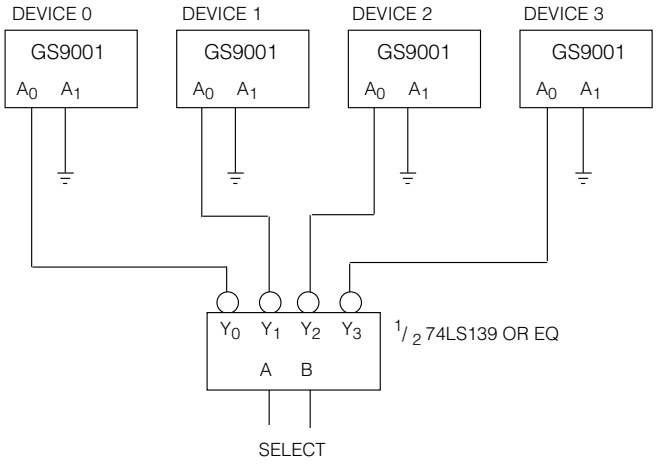


Fig. 4 Addressing Multiple GS9001s

The addressing sequence begins by selecting GS9001 #0 as address 0 and reading/writing to address 0. All other devices on the I^2C interface will be set as address 1, and the I^2C message will be ignored by these devices. GS9001 #2 can then be selected as address 0 and the read /write process repeated. All devices can be accessed by selecting one unique address to be read/writable at one time.

I^2C Memory Maps

A graphic representation of the READ and WRITE memory maps of the GS9001 are shown in Figures 5 and 6 respectively. The software package contained in the EK9001 evaluation kit can be used to obtain these displays.

Table 2 summarizes the SMPTE RP165 locations of the samples included in the checkword calculations.

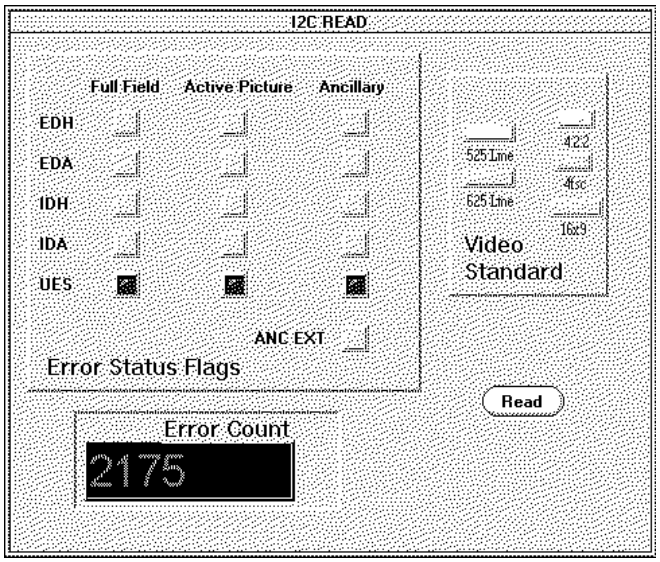


Fig. 5 Graphic Representation of the GS9001 I^2C Read Memory Map

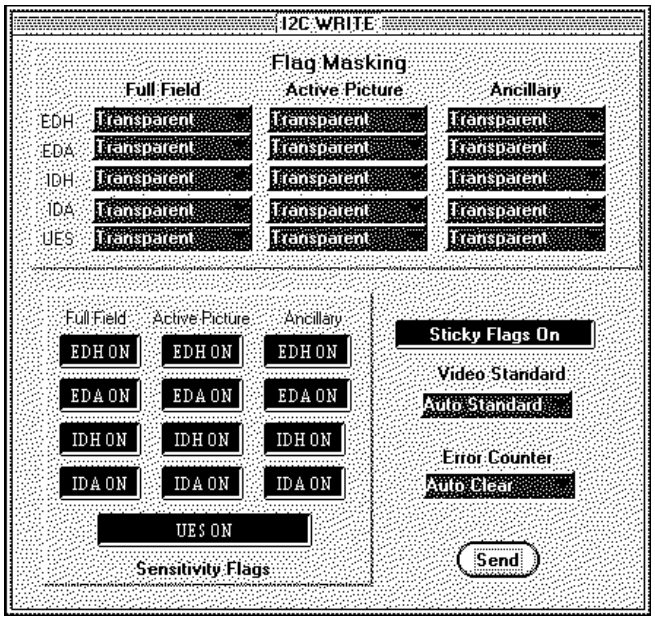


Fig. 6 Graphic Representation of the GS9001 I^2C Write Memory Map

AP	ACTIVE PICTURE	Only samples in the active picture area of each line
FF	FULL FIELD	All samples in all lines except the line containing the EDH packet and the two following lines.
ANC	ANCILLARY DATA AREA	Samples in the HANC and VANC data areas

TABLE 2 Sample Locations for SMPTE RP165 Checkword Calculations

EDH Flag Mask Bits

Each of the 15 EDH error flags in the GS9001 has an associated flag masking bit. After reset, all error flags are transparent and the mask bits are all reset to zero. Transparent error flags are always updated when a video data error occurs.

When a flag masking bit is set, the corresponding error flag is not updated when a video data error occurs. The error flag can then be set/reset by writing directly to the error flag memory location.

Sensitivity Status

All error flags in the GS9001 memory map have an associated Sensitivity Status bit. When the sensitivity status bit for an error flag is set, the 21 bit internal error counter will increment on every occurrence of that error flag. Setting the sensitivity status bit for an error flag will also cause the INTERRUPT output (pin 23) to go LOW on the occurrence of an error. The interrupt pin will stay LOW until an I^2C read has occurred.

Sticky Flags

The GS9001 will normally update EDH flags after every field. In systems where the I^2C interface is not read every field, it is possible that the occurrence of an EDH flag will be missed. The STICKY FLAG bit (word 2 bit 1) will force all EDH flags to stay set until they are read from the I2C interface. If the SENSITIVITY of an EDH flag is on, then the interrupt output of the GS9001 will remain low during this time. Although a sticky flag will remain set until an I^2C read has occurred, the error counter will increment only on the occurrence of the EDH flag.

Error Counter

The GS9001 error counter is an errored field counter. The counter will make a maximum of one increment per field. The 21 bit width of the counter will allow over nine hours of continuous errors to be recorded (60 fields/sec) before an overflow occurs.

The function of the internal error counter is determined by the Sensitivity Status bits as described above, and the AUTO CLR and CLR CNT bits (word 6 bits 1 and 2). Setting the AUTO CLR bit will force the GS9001 error counter to reset to zero after an I^2C read has occurred.

The default status for the error counter is to not clear after an I^2C read. Setting the CLR CNT bit will force the error counter to reset. The CLR CNT bit must be then be reset before the error counter will begin incrementing.

By referring to Table 2, it can be seen that there are locations in a video field that may contain errors that will not be detected by an EDH device. The two lines after the EDH packet are used for switching, and are ignored. Errors in the EDH packet are not visible to the errored field counter, but may be detected by reading the status of the ANC EXT bit (word 2 bit 1). The ANC EXT bit will be set if there is an error in the EDH packet checksum.

APPLICATIONS

Demultiplexing the FL1/FLO Pins

Figure 7 shows an interconnect between the GS9001 and a PLD. The PLD can be used to demultiplex the outputs of the GS9001 and provide access to all multiplexed Field and Standard information.

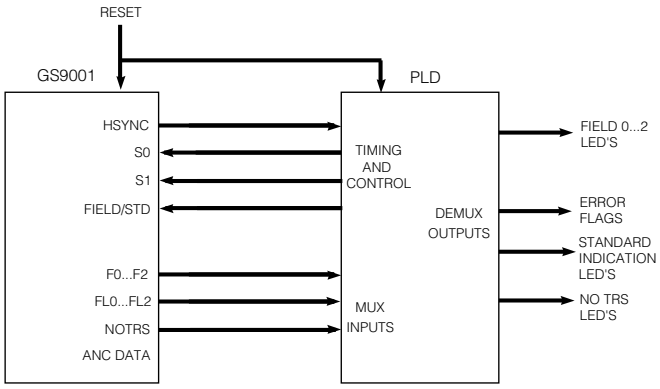


Fig. 7

The PLD is clocked by the HSYNC output of the GS9001. The HSYNC can be internally divided by four to provide a clock for the S0,S1 and Field/STD inputs of the GS9001. Figure 8 shows the timing relationship for the inputs to the GS9001.

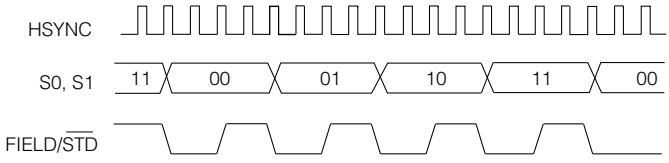


Fig. 8

Using the GS9001 in an Error Monitoring Distribution Amplifier

Figure 9 shows a block diagram of an EDH monitoring distribution amplifier. In this application, the DA only displays the EDH status of the video data stream, and does not update the EDH packet.

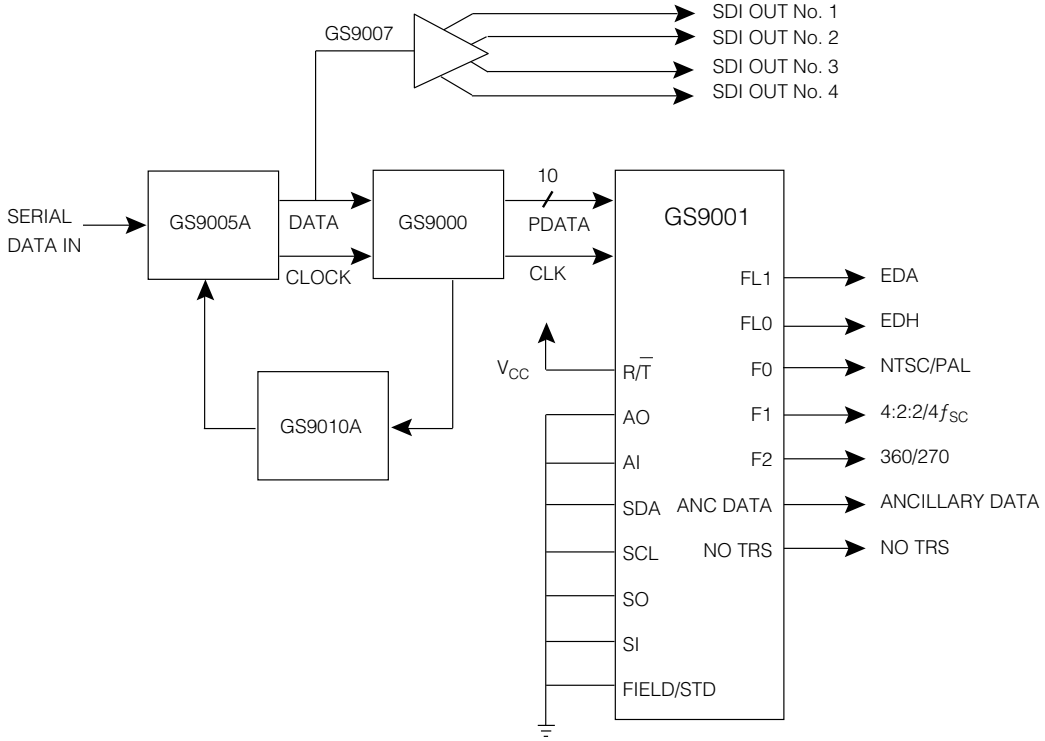


Fig. 9 EDH Monitoring Distribution Amplifier

Using the GS9001 in an Reserializing EDH Distribution Amplifier

An application using the GS9001 in a complete reserializing DA is shown in Figure 10. The DA uses the GS9001 to update the EDH packet and the GS9022 to reserialize the data. Conversion to the parallel domain has the advantage of reducing jitter present in the input data stream.

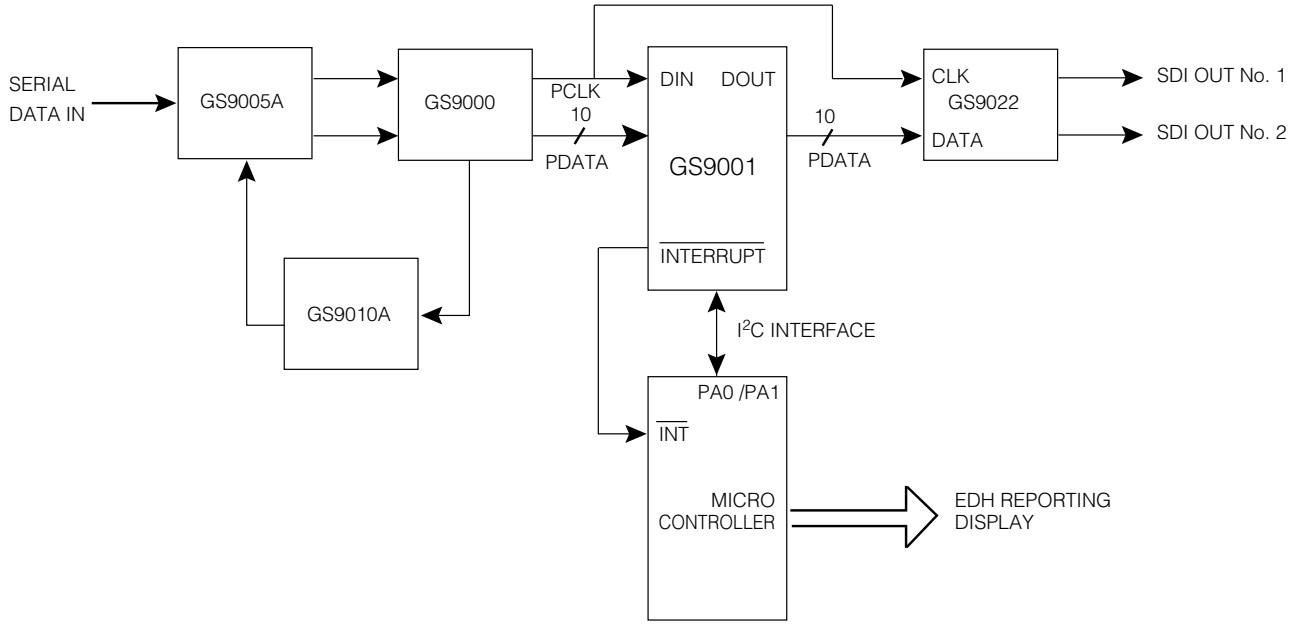
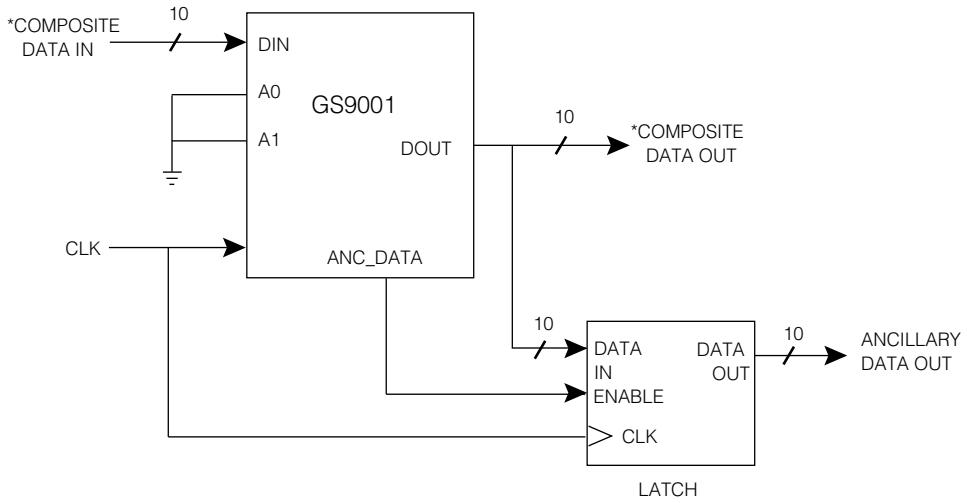


Fig. 10 EDH Handling Distribution Amplifier

Extracting ANC DATA using the ANC DATA flag

Figure 11 shows a basic circuit for extracting ancillary data from a composite video and ancillary data stream. The rising edge of the ANC_DATA pin is synchronous with the start of the ancillary data packet header. In this example, the Ancillary Data Out will also contain the ancillary data header information.



*Composite refers to Video and Ancillary Data

Fig. 11 Ancillary Data Extraction