DUAL PORT SYNCHRONOUS SRAM

256K/128K X 36 SRAM

+3.3V SUPPLY, FULLY REGISTERED
TWO BI-DIRECTIONAL DATA BUSES

FEATURES

- Fast clock speed: 100, and 83 MHz
- Fast Access Times: 5.0/6.0 ns Max
- Fully independent clock per port
- Single 3.3V -5% and +5% power supply VCC
- Separate VCCQ for output buffer
- Two chip enables for simple depth expansion
- Address, Data Input, CE1X#, CE2X, CE1Y#, CE2Y, WEX#, WEY#, and Data Output Registers On-Chip
- Concurrent Reads and Writes
- Two Bi-Directional Data Buses
- Can be Configured as Separate I/O
- Asynchronous Output Enables (OEX#, OEY#)
- LVTTL Compatible I/O
- Self-Timed Write
- Automatic power down
- 176-Pin TQFP Package

OPTIONS	MARKING
• Timing	
5.0ns access/10.0 cycle	-10
6.0ns access/12.0 cycle	-12
• Packages	
176-pin TQFP	T

GENERAL DESCRIPTION

The GVT81256K36/GVT81128K36 SRAM integrates 262,144x36/131,072x36 SRAM cells with advanced synchronous peripheral circuitry. It employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

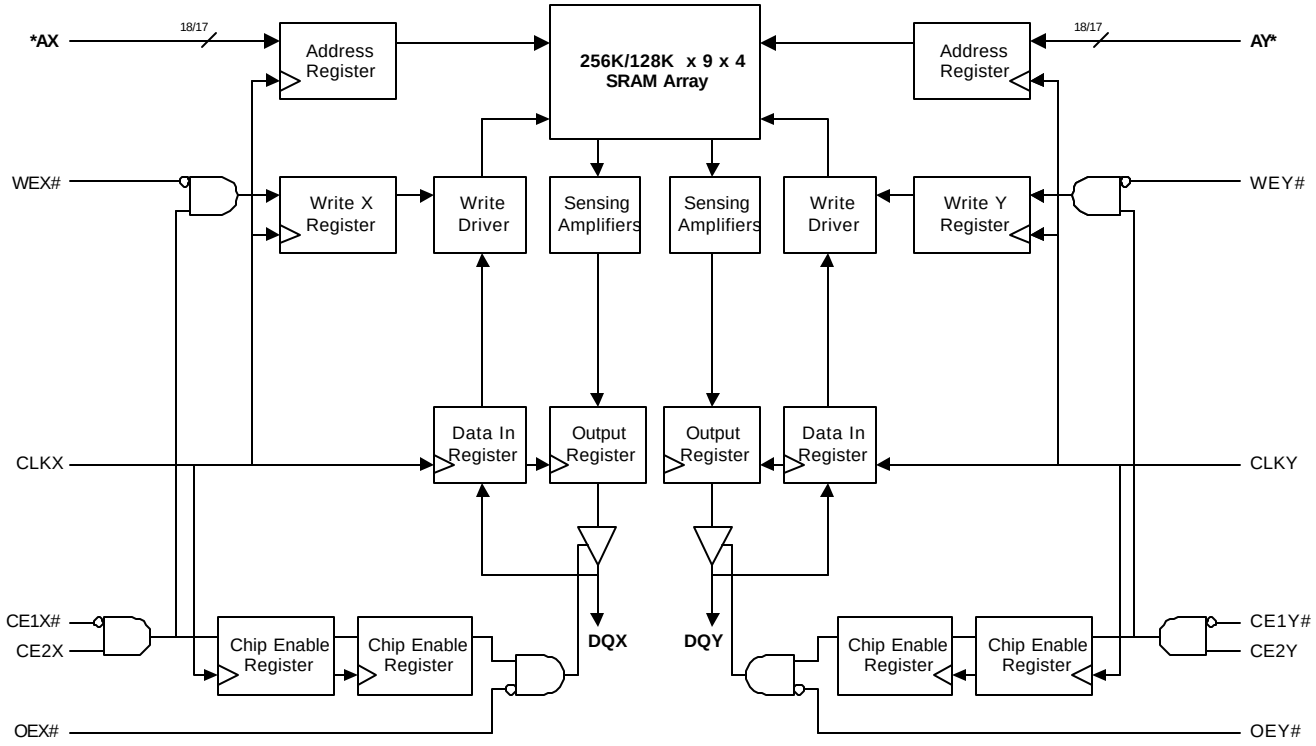
The GVT81256K36/GVT81128K36 allows the user to concurrently perform reads or writes cycles on the two data ports. The two address ports (AX, AY) determine the read or write locations for their respective data ports (DQX, DQY).

All input pins of each port, except output enable pins (OEX#, OEY#), are gated by registers controlled by the respective positive-edge-triggered clock inputs CLKX or CLKY. The synchronous inputs of Port X include all addresses (AX), all data inputs (DQX), depth-expansion chip enables (CE1X# and CE2X), and read-write control (WEX#). The synchronous inputs of Port Y include all addresses (AY), all data inputs (DQY), depth-expansion chip enables (CE1Y# and CE2Y), and read-write control (WEY#).

For the case when AX and AY are the same, certain protocols are followed. If the rising edges of the two clocks are separated by at least t_{CO}, the transaction associated with the earlier clock edge is guaranteed to be performed first. Otherwise, the transactions may occur in any order.

The GVT81256K36/GVT81128K36 operate from a +3.3V power supply. All inputs and outputs are LVTTL compatible. These dual I/O, dual address synchronous SRAMs are well suited for ATM, Ethernet switches, routers, cell/frame buffers, SNA switches and shared memory applications.

FUNCTIONAL BLOCK DIAGRAM

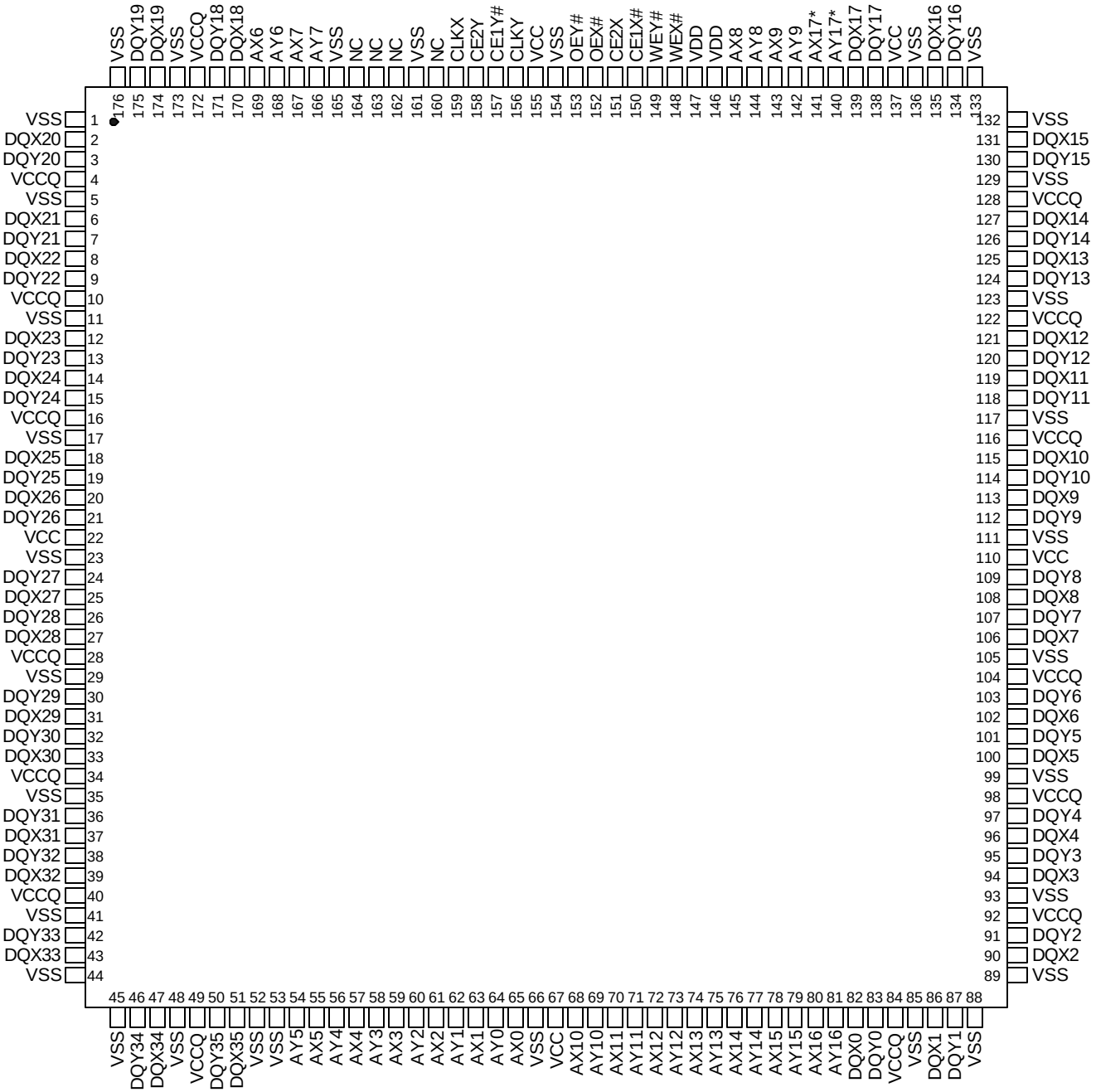


Note:
For 256K x 36 devices, AX and AY are 18-bit wide bus; for 128K x 36 devices, AX and AY are 17-bit wide bus.

GALVANTECH, INC.

GVT81256K36/GVT81128K36
256K/128K X 36 DUAL PORT SRAM

PIN ASSIGNMENT (Top View)



Notes:

1. AX17 and AY17 at pins 141 and 140 are for 256K x 36 devices only.
   For 128K x 36 devices, pins 141 and 140 are VSS.

PIN DESCRIPTIONS

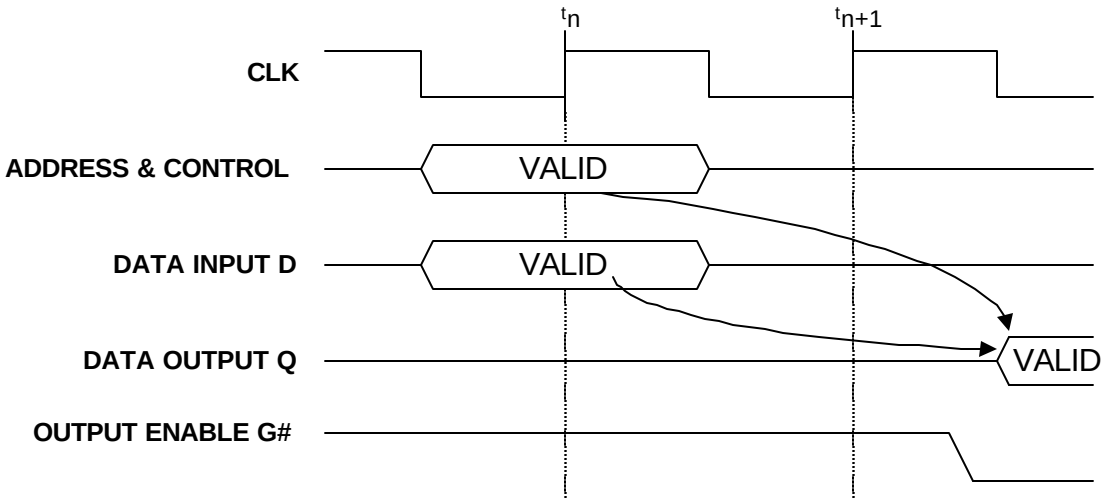
TQFP PINS	SYMBOL	TYPE	DESCRIPTION
65, 63, 61, 59, 57, 55, 169, 167, 145, 143, 68, 70, 72, 74, 76, 78, 80, 141	AX0 - AX17	Input-Synchronous	Synchronous Address Inputs of Port X: AX17 is for 256K x 36 devices only. Do not allow addresses AX0 - AX17 floating.
64, 62, 60, 58, 56, 54, 168, 166, 144, 142, 69, 71, 73, 75, 77, 79, 81, 140	AY0 - AY17	Input-Synchronous	Synchronous Address Inputs of Port Y: AY17 is for 256K x 36 devices only. Do not allow addresses AY0 - AY17 floating.
148	WEX#	Input-Synchronous	Read Write of Port X: WEX# signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
149	WEY#	Input-Synchronous	Read Write of Port Y: WEY# signal is a synchronous input that identifies whether the current loaded cycle is a Read or Write operation.
152	OEX#	Input	Asynchronous Output Enable of Port X: OEX# must be LOW to read data. When OEX# is HIGH, the DQXx pins are in high impedance state.
153	OEY#	Input	Asynchronous Output Enable of Port Y: OEY# must be LOW to read data. When OEY# is HIGH, the DQYx pins are in high impedance state.
82, 86, 90, 94, 96, 100, 102, 106, 108, 113, 115, 119, 121, 125, 127, 131, 135, 139, 170, 174, 2, 6, 8, 12, 14, 18, 20, 25, 27, 31, 33, 37, 39, 43, 47, 51	DQX0 - DQX35	Input/ Output	Data Inputs/Outputs of Port X: Both the data input path and data output path are registered and triggered by the rising edge of CLKX.
83, 87, 91, 95, 97, 101, 103, 107, 109, 112, 114, 118, 120, 124, 126, 130, 134, 138, 171, 175, 3, 7, 9, 13, 15, 19, 21, 24, 26, 30, 32, 36, 38, 42, 46, 50	DQY0 - DQY35	Input/ Output	Data Inputs/Outputs of Port Y: Both the data input path and data output path are registered and triggered by the rising edge of CLKY.
159	CLKX	Input-Synchronous	Clock Port X: This is the clock input to the Port X of this device. Except for OEX#, all timing references of the address, data in, and all control signals of Port X for the device are made with respect to the rising edge of CLKX.
156	CLKY	Input-Synchronous	Clock Port Y: This is the clock input to the Port Y of this device. Except for OEY#, all timing references of the address, data in, and all control signals of Port Y for the device are made with respect to the rising edge of CLKY.
150	CE1X#	Input-Synchronous	Synchronous Active Low Chip Enable Port X: CE1X# is used with CE2X to enable Port X of this device. CE1X# sampled HIGH at the rising edge of clock initiates a deselect cycle for Port X.
151	CE2X	input-Synchronous	Synchronous Active High Chip Enable Port X: CE2X is used with CE1X# to enable Port X of this device. CE2X sampled LOW at the rising edge of clock initiates a deselect cycle for Port X.
157	CE1Y#	Input-Synchronous	Synchronous Active Low Chip Enable Port Y: CE1Y# is used with CE2Y to enable Port Y of this device. CE1Y# sampled HIGH at the rising edge of clock initiates a deselect cycle for Port Y.
158	CE2Y	input-Synchronous	Synchronous Active High Chip Enable Port Y: CE2Y is used with CE1Y# to enable Port Y of this device. CE2Y sampled LOW at the rising edge of clock initiates a deselect cycle for Port Y.
22, 67, 110, 155	VCC	Supply	Power Supply: +3.3V -5% and +5%.
5, 11, 17, 23, 29, 35, 41, 48, 66, 85, 93, 99, 105, 111, 117, 123, 129, 136, 154, 161, 173	VSS	Ground	Ground: GND.
1, 44, 45, 52, 53, 88, 89, 132, 133, 165, 176	VSS	Ground	Ground: GND. No chip current flows through these pins. However, user needs to connect GND to these pins. Pins 140 and 141 are VSS for 128K x 36 device.
4, 10, 16, 28, 34, 40, 49, 84, 92, 98, 104, 116, 122, 128, 137, 172	VCCQ	I/O Supply	Output Buffer Supply: +3.3V -5% and +5%.
160, 162, 163, 164	NC	-	No Connect: These signals are not internally connected. User can connect them to VCC, VSS, or any signal lines or simply leave them floating.

TRUTH TABLE(1-4)

OPERATION NUMBER	CHIP ENABLES		OE#	WE#	OPERATION
	CE1#	CE2			
1	H	X	X	X	DESELECT CYCLE
2	X	L	X	X	DESELECT CYCLE
3	L	H	L	H	READ
4	L	H	H	L	WRITE
5	L	H	H	H	OUTPUT DISABLES

Note:

1. X means "don't care." H means logic HIGH. L means logic LOW.
2. All inputs, except OE#, must meet setup and hold times around the rising edge (LOW to HIGH) of the respective clock (CLK).
3. OEX# and OEY# must be asserted to avoid bus contention during WRITE cycles. For a WRITE operation following a READ operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.



ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN}.....-0.5V to VCC+0.5V
Storage Temperature (plastic).....-55°C to +125°
Temperature Under Bias.....-10°C to +85°
Junction Temperature.....+125°
Power Dissipation.....1.6W
Short Circuit Output Current.....20mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCC+0.5	V	1, 2
	All Other Inputs	V_{IH}	2.0	4.6	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-5	5	uA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-5	5	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		VCC	3.135	3.465	V	1
I/O Supply Voltage	3.3V I/O	VCCQ	3.135	3.465	V	1

DESCRIPTION	CONDITIONS	SYM	-10	-12	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH};VCC =MAX; CLK cycle time ≥ ^tKC MIN; outputs open	Icc	350	300	mA	3, 4
CMOS Standby	Device deselected; all inputs ≤ VSS +0.2 or ≥ VCC -0.2; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB1}	100	100	mA	4,

Note:

1. All voltages referenced to VSS (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ ^tKC /2
   Undershoot: V_{IL} ≤ -2.0V for t ≤ ^tKC /2.
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. "Device Deselected" means the device is in POWER -DOWN mode as defined in the truth table. "Device Selected" means the device is active.

AC ELECTRICAL CHARACTERISTICS

(Note 2) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +5%)

DESCRIPTION		-10 100MHz		-12 83MHz			
	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock							
Clock cycle time	^tKC	10		12		ns	
Clock HIGH time	^tKH	3.5		4.0		ns	
Clock LOW time	^tKL	3.5		4.0		ns	
Output Times							
Clock to output valid	^tKQ		5.0		6.0	ns	6
Clock to output invalid	^tKQX	1.5		1.5		ns	
Clock to output in Low-Z	^tKQLZ	0		0		ns	1, 3, 4
Clock to output in High-Z	^tKQHZ		3.0		3.0	ns	1, 3, 4
OEX#/OEY# to output valid	^tOEQ		5.0		6.0	ns	6
OEX#/OEY# to output in Low-Z	^tOELZ	0		0		ns	1, 3, 4
OEX#/OEY# to output in High-Z	^tOEHZ		3.0		3.0	ns	1, 3, 4
Port-to-Port delay	^tCO	3.0		3.0		ns	
Setup Times							
Addresses, Controls and Data In	^tS	1.5		2.0		ns	5
Hold Times							
Addresses, Controls and Data In	^tH	0.5		0.5		ns	5

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	6	pF	1
Input/Output Capacitance (DQ)		C_O	8	pF	1

THERMAL CONSIDERATION

DESCRIPTION	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient (@ 200 lfm) for Single-Layer Board	$R_{\Theta JA}$	40	$^oC/W$	
Thermal Resistance - Junction to Ambient (@ 200 lfm) for Four-Layer Board	$R_{\Theta JA}$	35	$^oC/W$	
Thermal Resistance - Junction to Board (Bottom)	$R_{\Theta JB}$	23	$^oC/W$	
Thermal Resistance - Junction to Case (Top)	$R_{\Theta JC}$	9	$^oC/W$	

Note:

1. This parameter is sampled.
2. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
3. Output loading is specified with CL=5pF as in Fig. 2.
4. At any given temperature and voltage condition, ^tKQHZ is less than ^tKQLZ and ^tOEHZ is less than ^tOELZ.
5. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
6. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

AC TEST CONDITIONS

Input pulse levels	0V to 3V
Input slew rate	1.0V/ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

OUTPUT LOADS

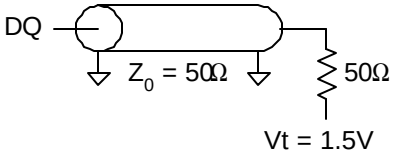


Fig. 1 OUTPUT LOAD EQUIVALENT

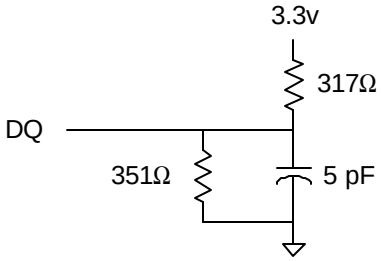
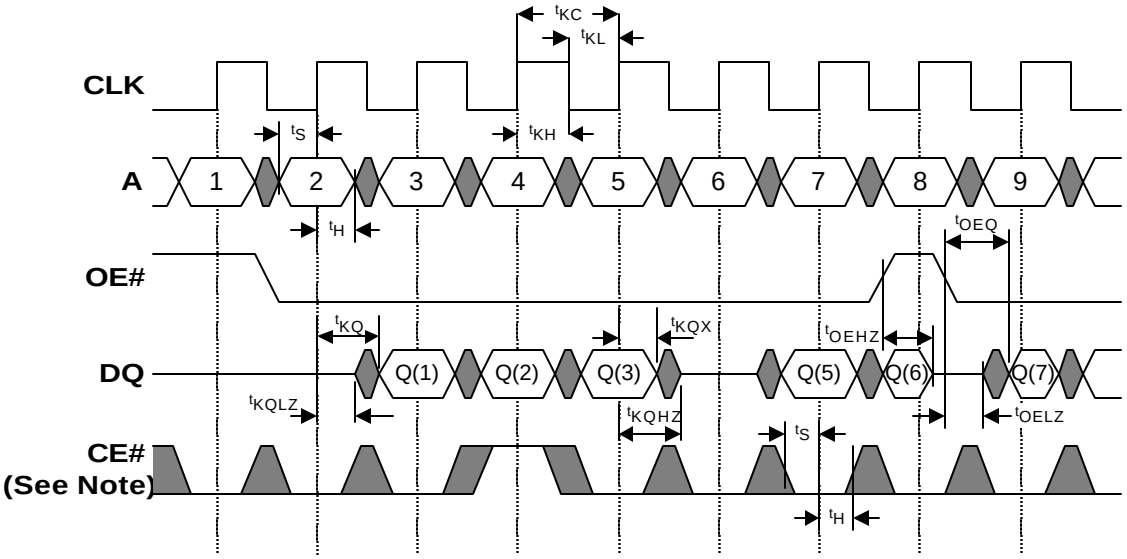


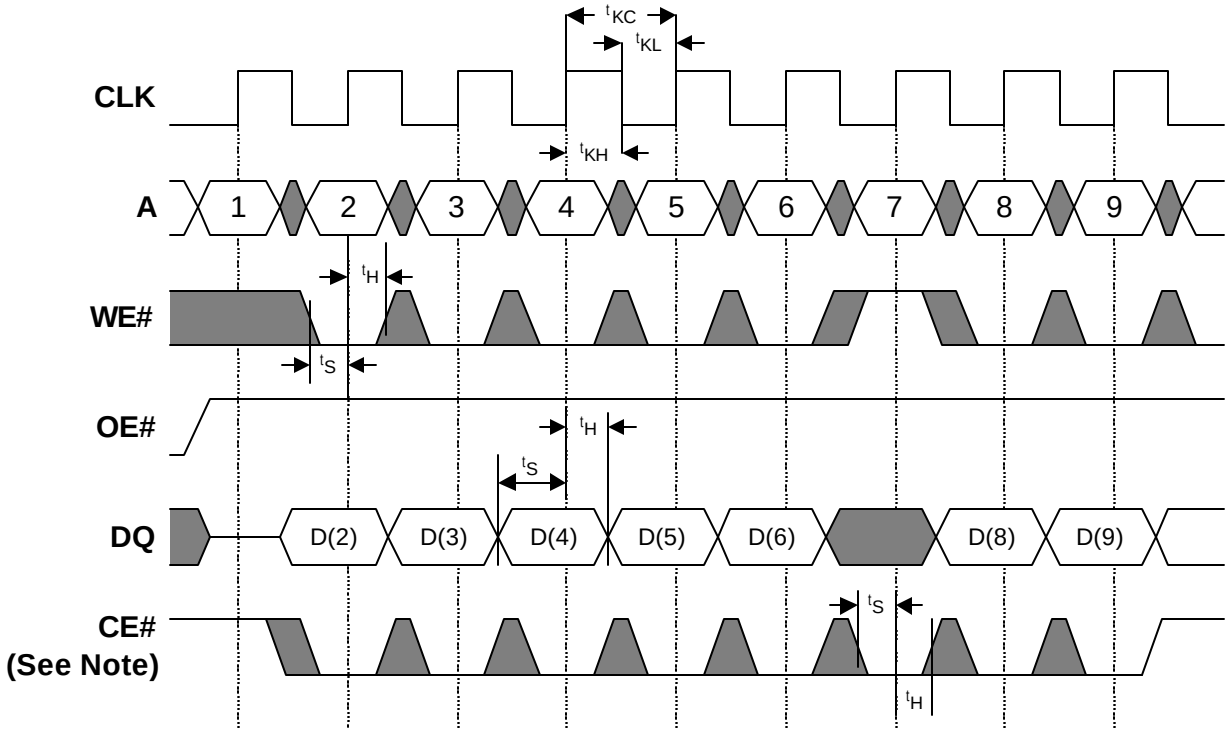
Fig. 2 OUTPUT LOAD EQUIVALENT

READ CYCLE TIMING FROM BOTH PORTS (WEX#, WEY# HIGH)

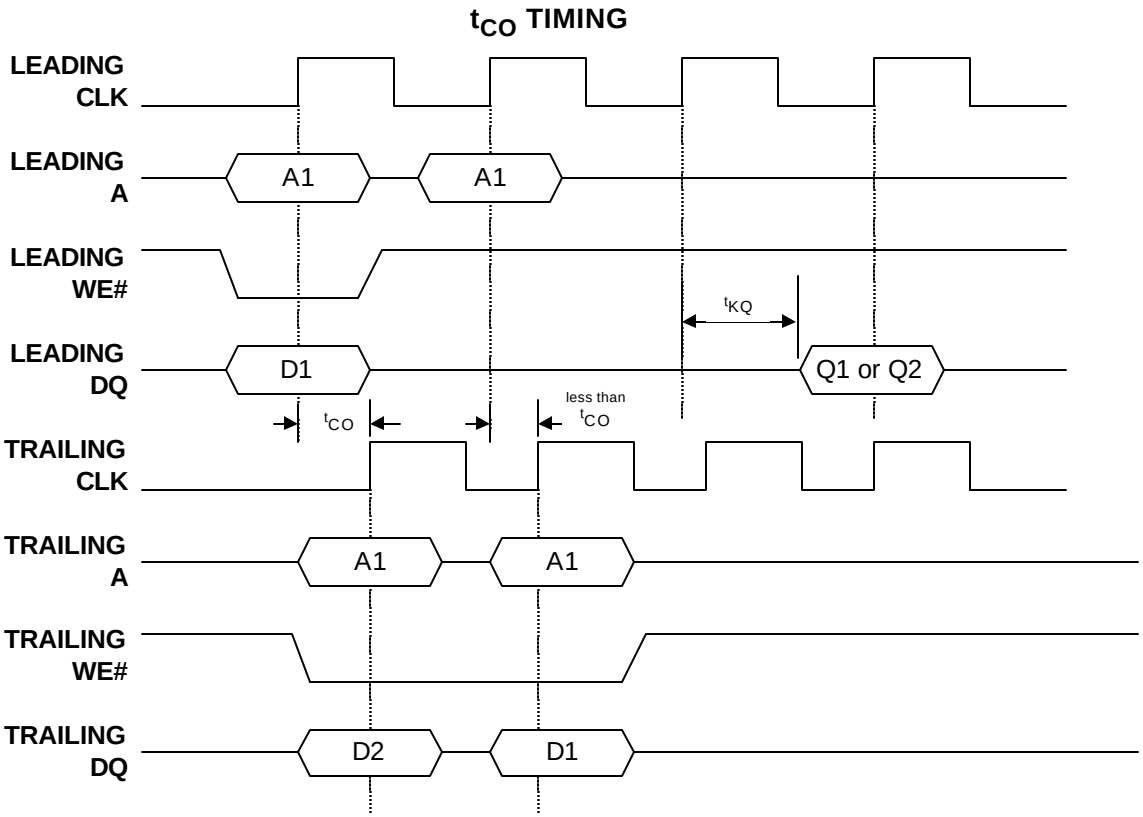


NOTE:
1. CE# LOW means CE1# equals LOW and CE2 equals HIGH. CE# HIGH means CE1# e HIGH or CE2 equals LOW.

WRITE CYCLE TIMING TO BOTH PORTS



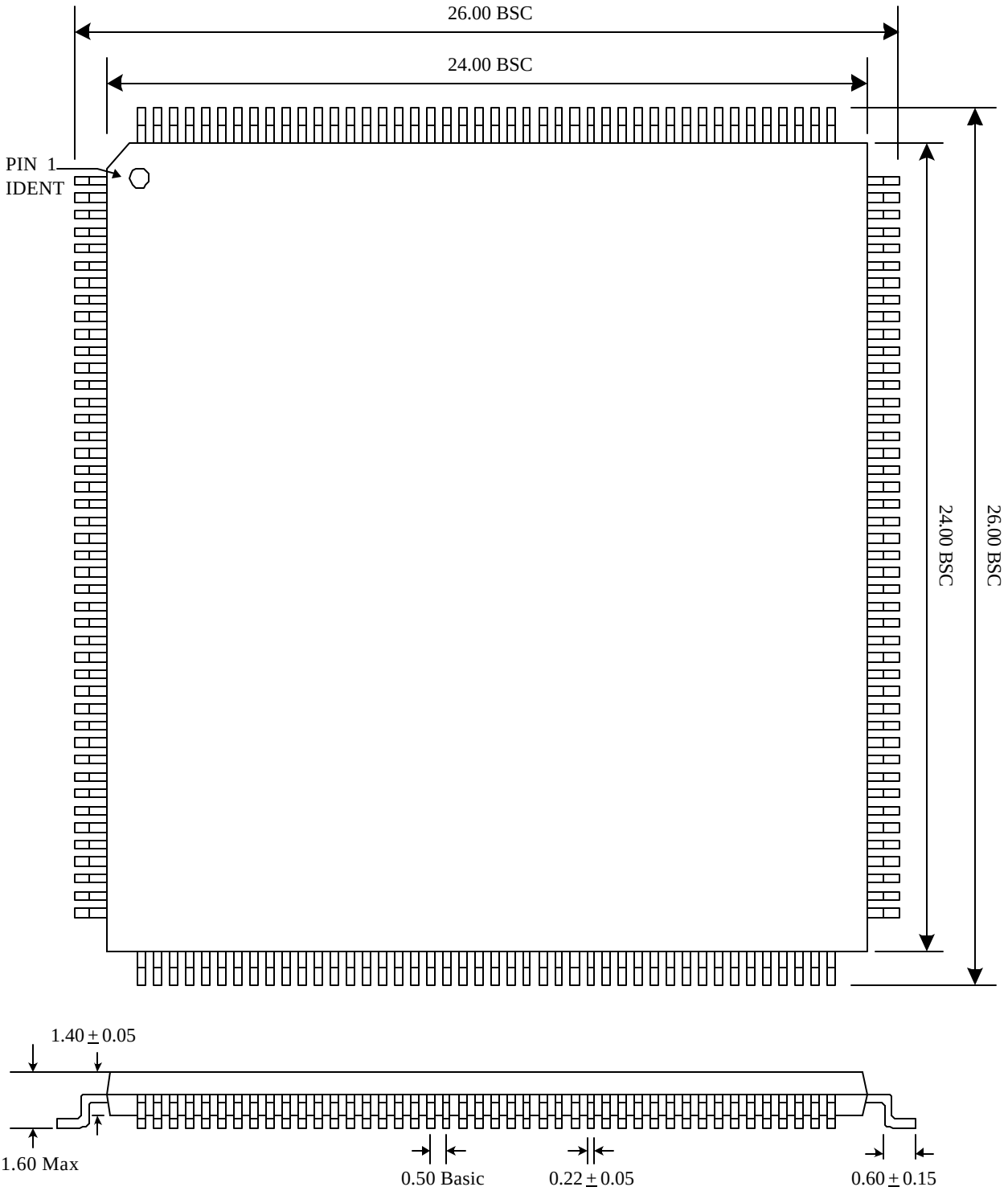
NOTE:
1. CE# LOW means CE1# equals LOW and CE2 equals HIGH. CE# HIGH means CE1# equals HIGH or CE2 equals LOW.



ADDRESS/CLOCK COLLISION (t_{CO} < 3ns, Leading Port Address = Trailing Port Address)

Leading Port	Trailing Port	Outcome
R	R	Internally, the reads may occur in any order. Externally, the user gets data from the address on both ports one cycle later.
W	W	These operations may occur in any order. Either the leading port data or the trailing port data will be written to the address location last
W R	R W	Internally, the reads may occur before or after the write. Therefore, the reading port may output the data that was written by the other port, or the data that was previously in the memory location pointed by the address.

176 Pin TQFP Package Dimensions



Note: All dimensions in Millimeters

Ordering Information

256K X 36

GVT 81256K36 X - XX

- Galvantech Prefix
- Part Number
- Package (T = 176 PIN TQFP)
- Speed (10 = 5.0ns access/10.0ns cycle
  12 = 6.0ns access/12.0ns cycle)

128K X 36

GVT 81128K36 X - XX

- Galvantech Prefix
- Part Number
- Package (T = 176 PIN TQFP)
- Speed (10 = 5.0ns access/10.0ns cycle
  12 = 6.0ns access/12.0ns cycle)