GAL®26CV12: Programmable Frequency Divider

Introduction

When designing with standard PLDs such as the GAL20V8 and GAL22V10, system design engineers are sometimes faced with a situation where a few extra product terms or macrocells are necessary to implement the design. These situations usually do not warrant adding a second standard PLD. The ideal solution is to find a way to add these extra product terms and/or outputs while still keeping the design in one device. The design example given in this application note illustrates one example of how the extra outputs of the GAL26CV12 can solve the common problem of needing additional outputs. The design will show a programmable frequency divider that uses a 10-bit counter as a base and can therefore divide the incoming frequency by up to 1024.

Design Example

The design requirements for the programmable logic device are 10 macrocells for the internal counter, one macrocell for the programmable output frequency, four inputs for the frequency selection and one input clock. Figure 1 below shows the simple block diagram of the programmable frequency divider.

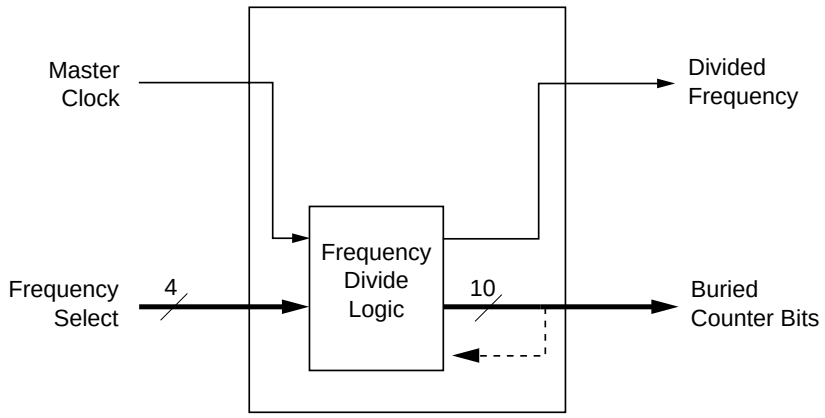
This frequency divider implementation, using D-type registers, requires more than eight product terms for the two most significant counter bits on the 10-bit counter. The programmable frequency output also requires more than eight products terms. Therefore, even two GAL20V8 devices (or other standard PAL devices) would not work for this design, since they only have a maximum of eight product terms per output. Since a total of 11 macrocells is required to implement the counter and the programmable frequency output, even a 22V10 device would not work.

A single GAL26CV12 device satisfies both the product term requirements and the output macrocell requirements for the example design. The equations and output pin assignments required to implement the 10-bit programmable frequency divider are provided in Example 1. Notice that the outputs that require more than eight product terms are assigned to the innermost pins of the device, since the innermost pins have the highest number of product terms available.

Summary

The GAL26CV12 has a total of 12 output logic macrocells and a product term distribution of eight terms on the outermost pins to 12 on the innermost pins. It comes in a 28-pin DIP and PLCC package, with center Vcc and Ground pins on the DIP package. When design engineers are frustrated by the limitations on the number of available product terms, output macrocells, or input pins on standard PLD devices, using the GAL26CV12 is a valuable design alternative. Since the GAL26CV12 can often save the cost of adding a second PLD, the design is simplified while also cutting cost and board space requirements.

Figure 1. Programmable Frequency Divider Block Diagram



Example 1. Equations and Output Pin Assignments for a 10-Bit Programmable Frequency Divider

```
Q0.D = (!Q0);          "PIN 27

Q1.D = (Q0 & !Q1
     # !Q0 & Q1);      "PIN 26

Q2.D = ( Q0 & Q1 & !Q2
     # !Q1 & Q2
     # !Q0 & Q2);      "PIN 25

Q3.D = (Q0 & Q1 & Q2 & !Q3
     # !Q2 & Q3
     # !Q1 & Q3
     # !Q0 & Q3);      "PIN 23

Q4.D = (Q0 & Q1 & Q2 & Q3 & !Q4
     # !Q3 & Q4
     # !Q2 & Q4
     # !Q1 & Q4
     # !Q0 & Q4);      "PIN 15

Q5.D = (Q0 & Q1 & Q2 & Q3 & Q4 & !Q5
     # !Q4 & Q5
     # !Q3 & Q5
     # !Q2 & Q5
     # !Q1 & Q5
     # !Q0 & Q5);      "PIN 16

Q6.D = (Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & !Q6
     # !Q5 & Q6
     # !Q4 & Q6
     # !Q3 & Q6
     # !Q2 & Q6
     # !Q1 & Q6
     # !Q0 & Q6);      "PIN 17

Q7.D = (Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6
        & !Q7
     # !Q6 & Q7
     # !Q5 & Q7
     # !Q4 & Q7
     # !Q3 & Q7
     # !Q2 & Q7
     # !Q1 & Q7
     # !Q0 & Q7);      "PIN 18

Q8.D = (Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7
        & !Q8
     # !Q7 & Q8
     # !Q6 & Q8
     # !Q5 & Q8
     # !Q4 & Q8
     # !Q3 & Q8
     # !Q2 & Q8
     # !Q1 & Q8
     # !Q0 & Q8);      "PIN 19

Q9.D = (Q0 & Q1 & Q2 & Q3 & Q4 & Q5 & Q6 & Q7
        & Q8 & !Q9
     # !Q8 & Q9
     # !Q7 & Q9
     # !Q6 & Q9
     # !Q5 & Q9
     # !Q4 & Q9
     # !Q3 & Q9
     # !Q2 & Q9
     # !Q1 & Q9
     # !Q0 & Q9);      "PIN 20

FDIV = (SEL0 & !SEL1 & !SEL2 & SEL3 & Q9
     # !SEL0 & !SEL1 & !SEL2 & SEL3 & Q8
     #  SEL0 &  SEL1 &  SEL2 & !SEL3 & Q7
     # !SEL0 &  SEL1 &  SEL2 & !SEL3 & Q6
     #  SEL0 & !SEL1 &  SEL2 & !SEL3 & Q5
     # !SEL0 & !SEL1 &  SEL2 & !SEL3 & Q4
     #  SEL0 &  SEL1 & !SEL2 & !SEL3 & Q3
     # !SEL0 &  SEL1 & !SEL2 & !SEL3 & Q2
     #  SEL0 & !SEL1 & !SEL2 & !SEL3 & Q1
     # !SEL0 & !SEL1 & !SEL2 & !SEL3 & Q0);
       "PIN 22
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Technical Support Assistance

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