GS1528
HD-LINX™ II Multi-Rate SDI Dual Slew-Rate Cable Driver

PRELIMINARY DATA SHEET

FEATURES

- **SMPTE 292M, SMPTE 344M and SMPTE 259M compliant**
- **dual coaxial cable driving outputs with selectable slew rate**
- **50Ω differential PECL input**
- **seamless interface to other HD-LINX™ II family products**
- **single 3.3V power supply operation**
- **operating temperature range: 0°C to 70°C**

APPLICATIONS

- SMPTE 292M, SMPTE 344M and SMPTE 259M Coaxial Cable Serial Digital Interfaces.

DESCRIPTION

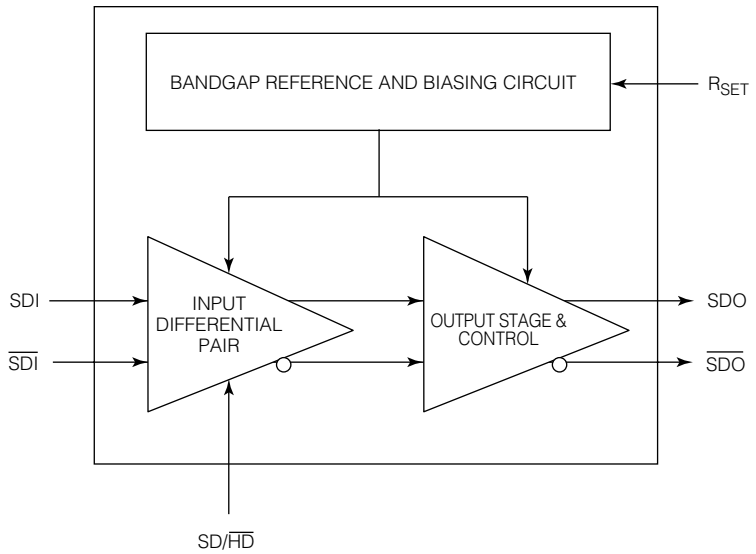
The GS1528 is a second generation high-speed bipolar integrated circuit designed to drive one or two 75Ω co-axial cables at data rates up to 1.485Gb/s. The GS1528 provides two selectable slew rates in order to achieve compliance to SMPTE 259M, SMPTE 344M and SMPTE 292M.

The GS1528 accepts a LVPECL level differential input that may be AC coupled. External biasing resistors at the inputs are not required.

Power consumption is typically 160mW using a 3.3V power supply.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE
GS1528-CKA	8 pin SOIC	0°C to 70°C



FUNCTIONAL BLOCK DIAGRAM

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise indicated

PARAMETER	VALUE
Supply Voltage	-0.5V to 3.6 V_{DC}
Input ESD Voltage	500V
Storage Temperature Range	-50°C < T_s < 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC} +0.3)V
Operating Temperature Range	0°C to 70°C
Power Dissipation	300mW
Lead Temperature (soldering, 10 sec)	260°C

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVELS
Supply Voltage		V_{CC}	3.135	3.3	3.465	V	±5%	3
Power Consumption	T_A = 25°C	P_D	-	160	-	mW		5
Supply Current	T_A = 25°C	I_s	-	48	-	mA		1
Output Voltage	Common mode	V_{CMOUT}	-	V_{CC} - V_{OUT}	-	-		6
Input Voltage	Common mode	V_{CMIN}	1.6 + V_{DIFFIN}/2	-	V_{CC} - V_{DIFFIN}/2	V		5

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	TEST LEVELS
Serial input data rate			-	-	1.485	Gb/s	2	1
Additive jitter	1.485Gb/s		-	15	-	ps_{p-p}		1
	270Mb/s		-	25	-	ps_{p-p}		1
Rise/Fall time	SD/$\overline{HD}$=0	t_r, t_f	-	-	220	ps	20% to 80%	1
	SD/$\overline{HD}$=1	t_r, t_f	400	-	800	ps	20% to 80%	1
Mismatch in rise/fall time			-	-	30	ps		1
Duty cycle distortion			-	-	30	ps		1
Overshoot			-	-	8	%		1
AC return loss			15	-	-	dB	1	7
Output Voltage Swing	Single Ended	V_{OUT}	750	800	850	mV_{p-p}	into 75Ω, R_{SET} = 750Ω	1
Input Voltage Swing	Differential	V_{DIFFIN}	80	200	800	mV_{p-p}		1

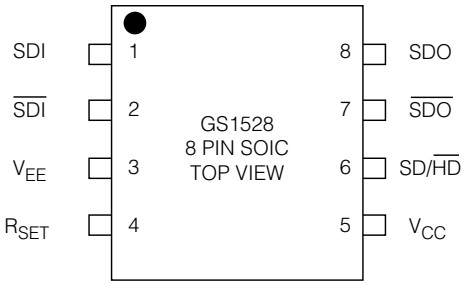
TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1, 2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

NOTES:

1. Tested on CB1528 board from 5MHz to 1.435GHz
2. The input coupling capacitor must be set accordingly for lower data rates.

PIN CONNECTIONS



8 PIN SOIC

PIN DESCRIPTION

PIN NUMBER	NAME	TYPE	DESCRIPTION
1,2	SDI, $\overline{SDI}$	PECL INPUT	Serial digital differential input.
4	R_{SET}	INPUT	External output amplitude control resistor.
6	SD/$\overline{HD}$	LOGIC INPUT	Output slew rate control. When HIGH, the output will meet SMPTE259M rise/fall time specifications. When LOW, the serial outputs will meet SMPTE292M rise/fall time specifications.
7, 8	$\overline{SDO}$, SDO	OUTPUT	Serial digital differential output.
3	V_{EE}	POWER	Most negative power supply connection. Connect to GND.
5	V_{CC}	POWER	Most positive power supply connection. Connect to +3.3V.

INPUT/OUTPUT CIRCUITS

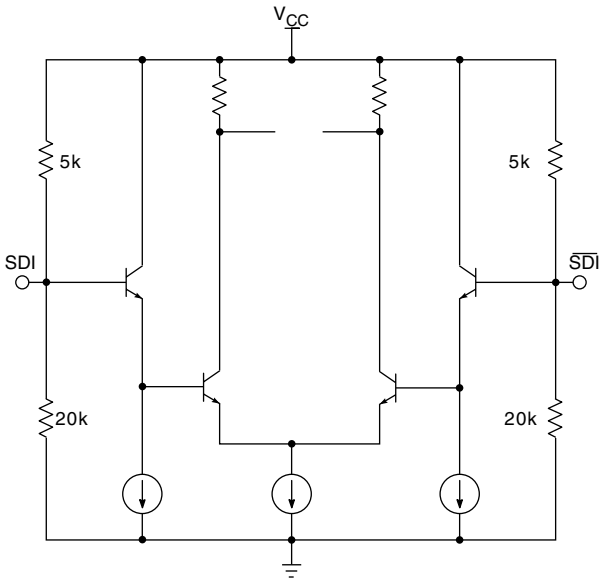


Fig. 1 Differential Input Stage

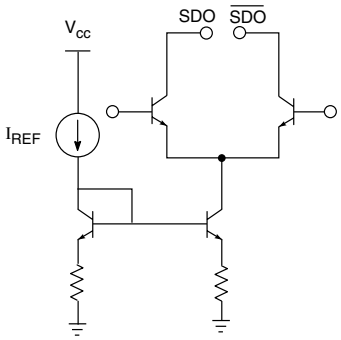


Fig. 2 Differential Output Stage, I_{REF} Derived using R_{SET}

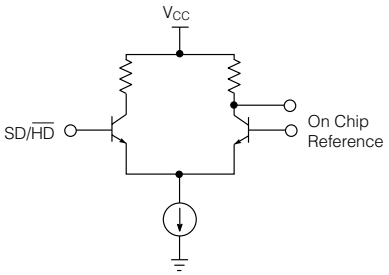


Fig. 3 Slew Rate Select Input Stage

DETAILED DESCRIPTION

INPUT INTERFACING

SDI/$\overline{\text{SDI}}$ are high impedance differential inputs. (*See Figure 1 for equivalent input circuit*).

Several conditions must be observed when interfacing to these inputs:

1. The differential input signal amplitude must be between 80 and 800mVpp.
2. The common mode voltage range must be as specified in the DC Characteristics Table. A 750mV differential input from the GS1524 HD cable equalizer, this corresponds to a common mode voltage range of between 1.975 to 2.925 volts.
3. For input trace lengths longer than approximately 1cm, the inputs should be terminated as shown in the Typical Application Circuit.

The GS1528 inputs are self-biased, allowing for simple AC coupling to the device. For serial digital video, a minimum capacitor value of 4.7µF should be used to allow coupling of pathological test signals. A tantalum capacitor is recommended.

SD/$\overline{\text{HD}}$

The GS1528 SDO rise and fall times can be set to comply with both SMPTE 259M/344M and SMPTE 292M. For all SMPTE 259M standards, or any data rate that requires longer rise and fall time characteristics, the SD/$\overline{\text{HD}}$ pin must be set to a HIGH INPUT. For SMPTE 292M standards and signals which require faster rise and fall times, this pin should be set to a LOW INPUT.

OUTPUT INTERFACING

The GS1528 outputs are current mode, and will drive 800mV into a 75Ω load. These outputs are protected from accidental static damage with internal static protection diodes.

The SMPTE 292M, SMPTE 344M and SMPTE 259M standards requires that the output of a cable driver have a source impedance of 75Ω and a return loss of at least 15dB between 5MHz and 1.485GHz.

In order for an SDI output circuit using the GS1528 to meet this specification, the output circuit shown in the Typical Application Circuit is recommended.

The values of L_{COMP} and C_{COMP} will vary depending on the PCB layout, but typical values are 5.6nH and 0pF respectively (*see the Application Information section in this data sheet for further details*). A 4.7µF capacitor is used for AC coupling the output of the GS1528. This value is chosen to ensure that pathological signals can be coupled without a significant DC component occurring.

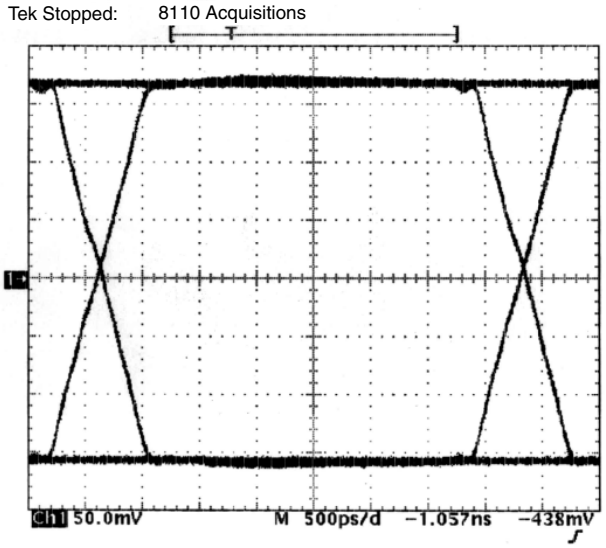


Fig. 4 Output signal for 270Mb/s input

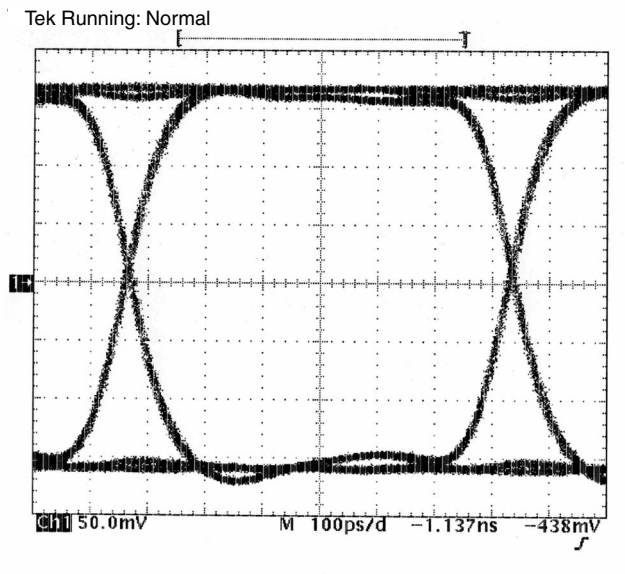


Fig. 5 Output signal for 1.485Gb/s input

When measuring return loss at the GS1528 output, it is necessary to take the measurement for both a logic high and a logic low output condition. This is because the output protection diodes act as a varactor (voltage controlled capacitor) as shown in Figure 6.

Consequently, the output capacitance of the GS1528 is dependent on the logic state of the output.

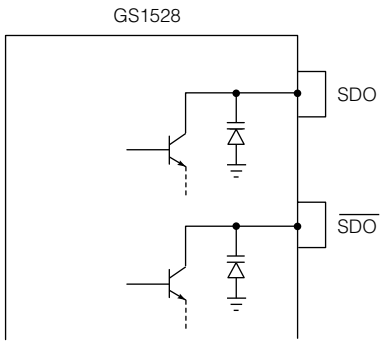


Fig. 6 Static Protection Diodes

OUTPUT RETURN LOSS MEASUREMENT

To perform a practical return loss measurement, it is necessary to force the GS1528 output to a DC high or low condition. The actual measured return loss will be based on the outputs being static at V_{CC} or V_{CC}-1.6V. Under normal operating conditions the outputs of the GS1528 swing between V_{CC}-0.4V and V_{CC}-1.2V, so the measured value of return loss will not represent the actual operating return loss.

A simple method of calculating the values of actual operating return loss is to interpolate the two return loss measurements. In this way, the values of return loss are estimated at V_{CC}-0.4V and V_{CC}-1.2V based on the measurements at V_{CC} and V_{CC}-1.6V.

The two values of return loss (high and low) will typically differ by several decibels. If the measured return loss is R_H for logic high and R_L for logic low, then the two values can be interpolated as follows:

$$R_{IH} = R_H - (R_H - R_L)/4 \text{ and}$$

$$R_{IL} = R_L + (R_H - R_L)/4$$

where R_{IH} is the interpolated logic high value and R_{IL} is the interpolated logic low value.

For example, if R_H = -18dB and R_L = -14dB, then the interpolated values are R_{IH} = -17dB and R_{IL} = -15dB.

OUTPUT AMPLITUDE ADJUSTMENT

The output amplitude of the GS1528 can be adjusted by changing the value of the R_{SET} resistor as shown in Figure 7 and Table 1. For an 800mV_{p-p} output with a nominal ±7% tolerance, a value of 750Ω is required. A ±1% SMT resistor should be used.

The R_{SET} resistor is part of the high speed output circuit of the GS1528. The resistor should be placed as close as possible to the R_{SET} pin. In addition, the PCB capacitance should be minimized at this node by removing the PCB groundplane beneath the R_{SET} resistor and the R_{SET} pin.

TABLE 1: R_{SET} vs V_{OD}

R_{SET} R (Ω)	OUTPUT SWING
995	608
824	734
750	800
600	884
573	1040

NOTE: For reliable operation of the GS1528 over the full temperature range, do not use an R_{SET} value below 573Ω.

APPLICATION INFORMATION

PCB LAYOUT

Special attention must be paid to component layout when designing serial digital interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

The PCB trace width for HD rate signals is closely matched to SMT component width to minimize reflections due to changes in trace impedance.

The PCB groundplane is removed under the GS1528 output components to minimize parasitic capacitance.

The PCB ground plane is removed under the GS1528 R_{SET} pin and resistor to minimize parasitic capacitance.

Input and output BNC connectors are surface mounted in-line to eliminate a transmission line stub caused by a BNC mounting via high speed traces which are curved to minimize impedance variations due to change of PCB trace width.

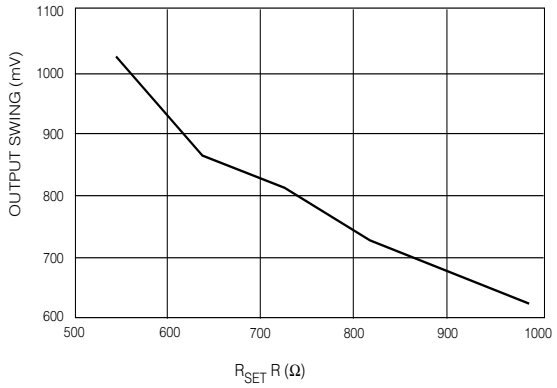
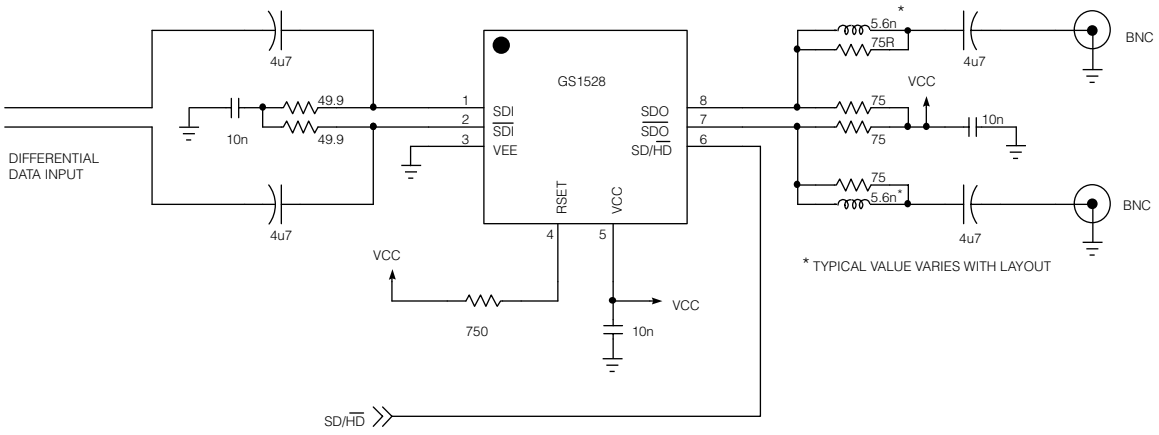
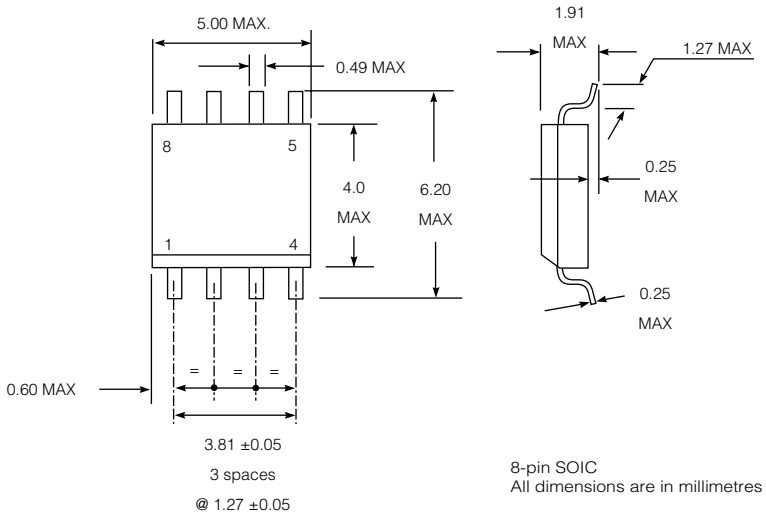


Fig. 7 Output Amplitude Adjustment

TYPICAL APPLICATION CIRCUIT



PACKAGE DIMENSIONS



8-pin SOIC
All dimensions are in millimetres

8 PIN SOIC

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

REVISION NOTES:
New Document

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