Microcircuits

CMOS Peripheral Interface Adapter

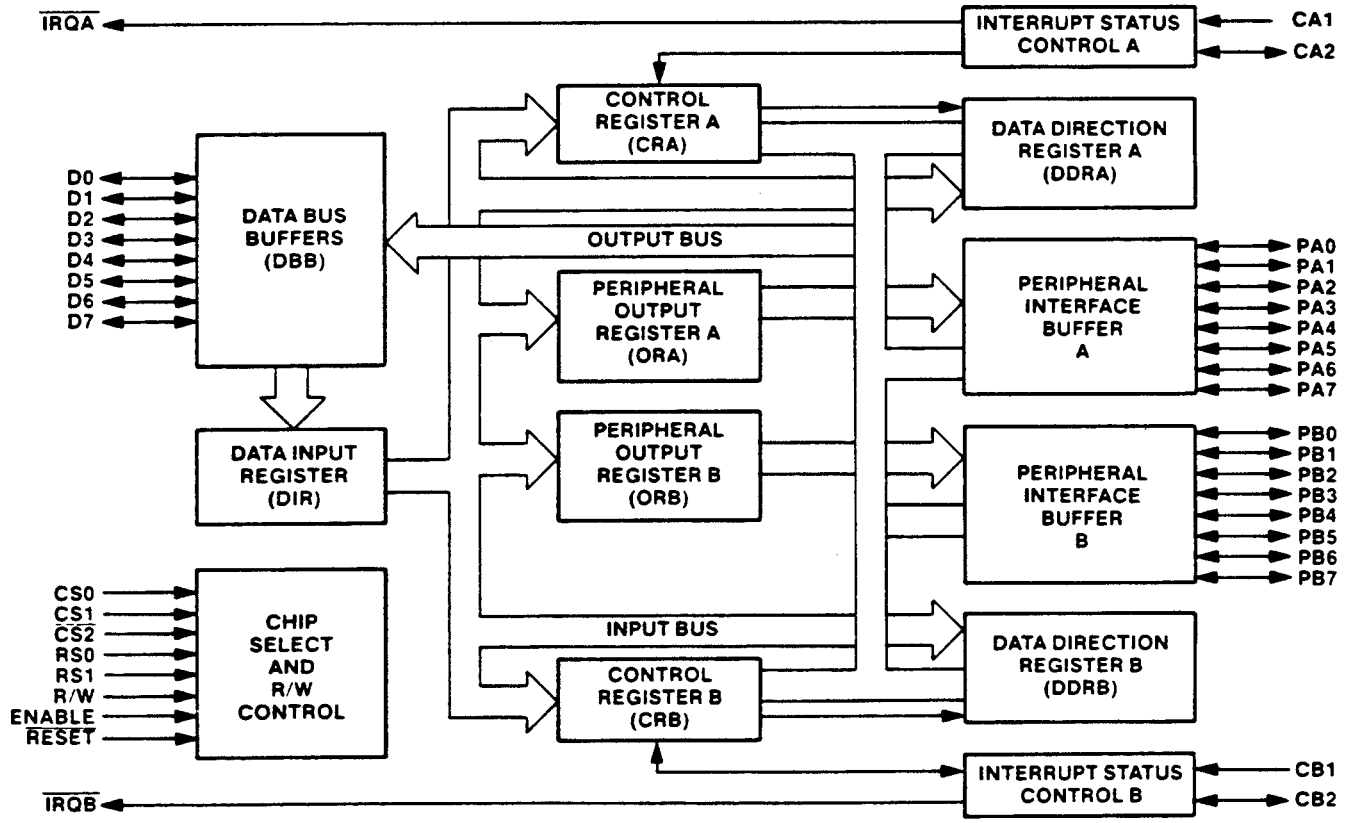
Features

- CMOS process technology for low power consumption
- Direct replacement for NMOS 6521 and 6821 devices manufactured by others
- Low power consumption (2 mA at 1MHz) allows battery powered operation
- Two programmable 8-bit bidirectional I/O Ports for peripheral device interfacing
- Individual Data Direction Registers for each I/O Port
- Microprocessor/peripheral "handshake" interrupt feature for enhanced data transfer control
- Programmable interrupt capability
- Four operating frequencies—1, 2, 3 and 4 MHz
- Automatic power-up initialization
- Single +5 volt power supply
- Available in 40-pin dual-in-line or 44-pin PLCC package

General Description

The CMD G65SC21 is a very flexible Peripheral Interface Adapter for use with CMD and other 8-bit microprocessor families. The G65SC21 provides programmed microprocessor control of up to two peripheral devices (Port A and Port B). Peripheral device control is accomplished through two 8-bit bidirectional I/O Ports, with individually assigned Data Direction Registers. The Data Direction Registers allow selection of data flow direction (input or output) at each respective I/O) Port. Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port. The "handshake" interrupt control feature is provided by four peripheral control lines. This capacity provides enhanced control over data transfer functions between the microprocessor and peripheral devices, as well as bidirectional data transfer between G65SC21 Peripheral Interface Adapters in multiprocessor systems.

Block Diagram



C0990500

Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value
Supply Voltage	V_{DD}	-0.3V to +7.0V
Input Voltage	V_{IN}	-0.3V to V_{DD} +0.3V
Operating Temperature	T_A	-40° C to +85° C
Storage Temperature	T_S	-55° C to +150° C

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may cause permanent damage, functional operation under these conditions is not implied.

DC Characteristics: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	Min.	Max.	Unit
Input High Voltage	V_{IH}	2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	0.8	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), Input Only Pins, R/$\overline{W}$, $\overline{RES}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, ϕ2	I_{IN}		±1.0	µA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), D0-D7, PB0-PB7, CB2, $\overline{IRQA}$, $\overline{IRQB}$	I_{TSI}		±10.0	µA
Input High Current (V_{IH} = 2.4V), Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IH}	-200		µA
Input Low Current (V_{IL} = 0.4V) Peripheral Inputs with Pullups, PA0-PA7, CA2	I_{IL}		-2.4	mA
Output Low Voltage (I_{OL} = 3.2 mA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OL}		0.4	V
Output High Voltage (I_{OH} = -200 µA), PA0-PA7, PB0-PB7, D0-D7, CA2, CB2, $\overline{IRQA}$, $\overline{IRQB}$	V_{OH}	2.4		V
Output High Current (Sourcing) (V_{OH} = 1.5V, Direct Transistor Drive), PB0-PB7, CB2	I_{OH}	-3.0		mA
Supply Current (No Load) f = 1 MHz f = 2 MHz f = 3 MHz f = 4 MHz	I_{DD} I_{DD} I_{DD} I_{DD}		2.0 4.0 6.0 8.0	mA mA mA mA
Power Dissipation (Inputs = V_{SS} or V_{DD}, No Loads), Operating (V_{DD} = 5.5V, f = 1 MHz) Standby (Static)	P_D P_{DSB}		11.0 11.0	mW µW
Input Capacitance (f = 1 MHz)	C_{IN}		5.0	pF
Output Capacitance (f = 1 MHz)	C_{OUT}		10.0	pF

AC Characteristics—Processor Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

		G65SC21-1		G65SC21-2		G65SC21-3		G65SC21-4		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle Time	t_{CYC}	1000	—	500	—	330	—	250	—	nS
Phase 2 Pulse Width High	t_{PWH}	450	—	220	—	160	—	110	—	nS
Phase 2 Pulse Width Low	t_{PWL}	450	—	220	—	160	—	110	—	nS
Phase 2 Transition	$t_{R,F}$	—	30	—	30	—	30	—	30	nS
Read Timing (Figure 1)										
Select, R/$\overline{W}$ Setup	t_{ACR}	140	—	70	—	53	—	35	—	nS
Select, R/$\overline{W}$ Hold	t_{CAR}	0	—	0	—	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	145	—	105	—	85	nS
Data Bus Hold	t_{HR}	10	—	10	—	10	—	10	—	nS
Peripheral Data Setup	t_{PCR}	300	—	150	—	110	—	75	—	nS

AC Characteristics: (Continued)

Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
Write Timing (Figure 2)										
Select R/$\overline{W}$ Setup	t_{ACW}	140	—	70	—	53	—	35	—	nS
Select, R/$\overline{W}$ Hold	t_{CAW}	0	—	0	—	0	—	0	—	nS
Data Bus Setup	t_{DCW}	180	—	90	—	65	—	45	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	10	—	10	—	nS
Peripheral Data Delay (Port A)	t_{CPW}	—	1000	—	500	—	330	—	320	nS
(Port B)		—	1000	—	500	—	330	—	250	

Note: Measurement points 0.8V and 2.0V unless otherwise specified.

AC Characteristics—Peripheral Interface Timing: V_{DD} = 5.0V ± 5%, V_{SS} = 0V, T_A = -40° C to +85° C Industrial, 0° C to +70° C Commercial

Parameter	Symbol	G65SC21-1 Min	G65SC21-1 Max	G65SC21-2 Min	G65SC21-2 Max	G65SC21-3 Min	G65SC21-3 Max	G65SC21-4 Min	G65SC21-4 Max	Unit
CA2 Delay Time, High-to-Low	t_{CA2}	—	1.0	—	0.5	—	0.33	—	0.25	µS
CA2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	µS
CA2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	µS
CB2 Delay Time, High-to-Low	t_{CB2}	—	1.0	—	0.5	—	0.33	—	0.25	µS
CB2 Delay Time, Low-to-High	t_{RS1}	—	1.0	—	0.5	—	0.33	—	0.25	µS
CB2 Delay Time, Handshake Mode	t_{RS2}	—	2.0	—	1.0	—	0.67	—	0.50	µS
CB2 Delay Time from Data Valid	t_{DC}	20	—	20	—	20	—	20	—	nS
Interrupt Input Pulse Width	P_{WI}	500	—	500	—	330	—	250	—	nS
Interrupt Response Time	t_{RS3}	—	1.0	—	1.0	—	0.67	—	0.33	µS
Interrupt Clear Delay	t_{IR}	—	1.6	—	0.85	—	0.67	—	0.33	µS
Rise and Fall Times— CA1, CA2, CB1, CB2	t_R, t_F	—	1.0	—	1.0	—	0.67	—	0.33	µS

Timing Diagrams

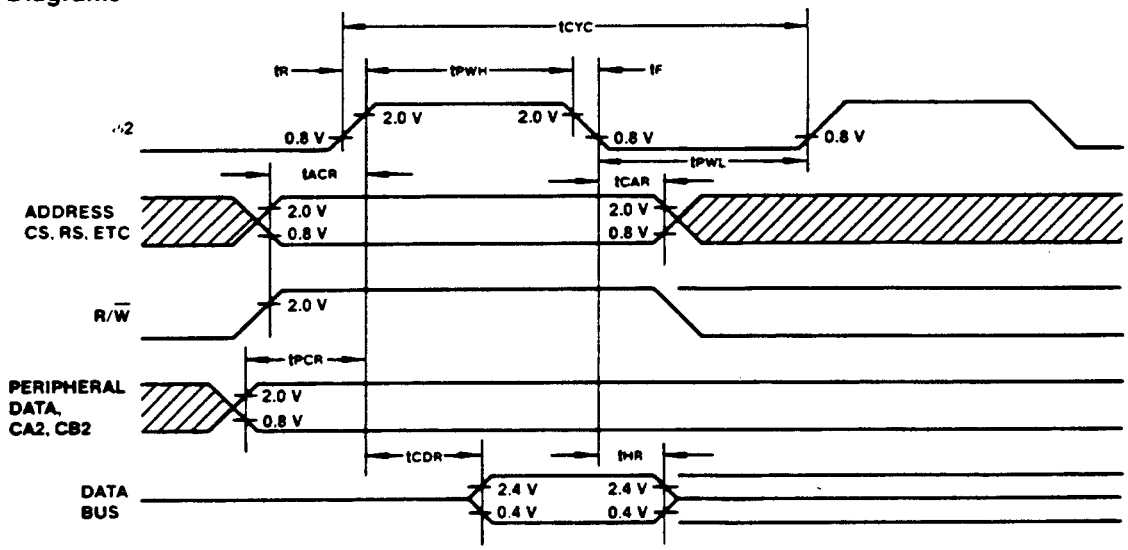


Figure 1. Read Timing

Timing Diagram (continued)

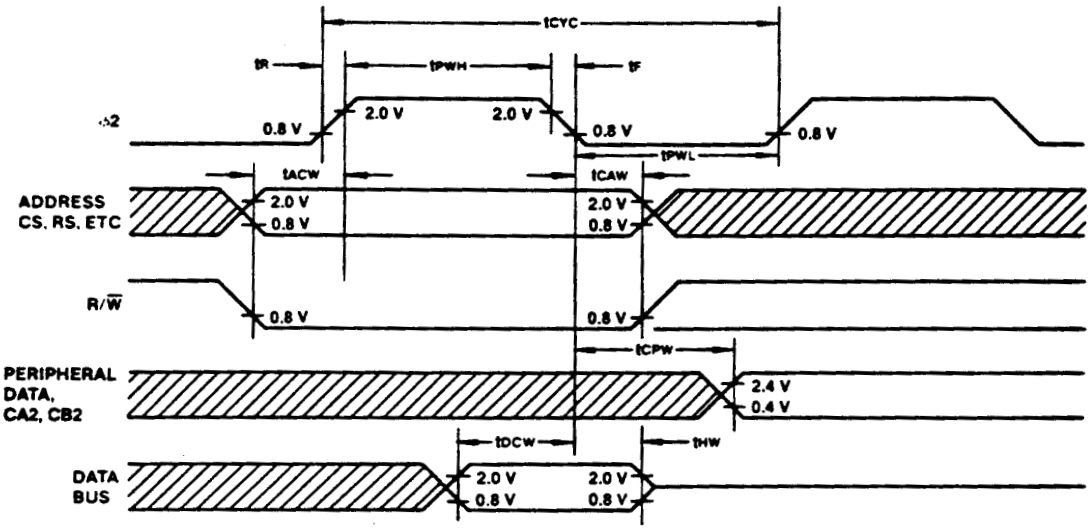


Figure 2. Write Timing

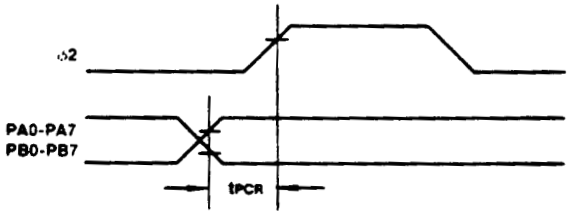


Figure 3. Peripheral Data Setup Time

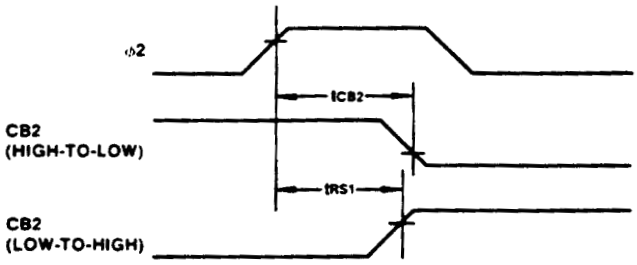


Figure 6. CB2 Timing

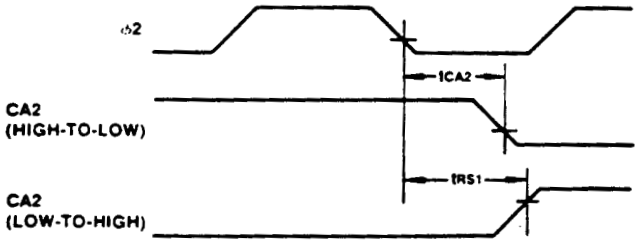


Figure 4. CA2 Timing

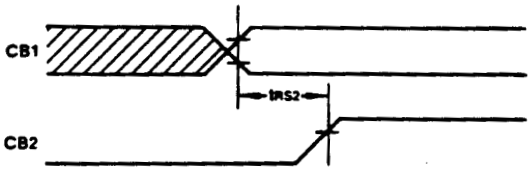


Figure 7. CB1/CB2 Handshake Timing

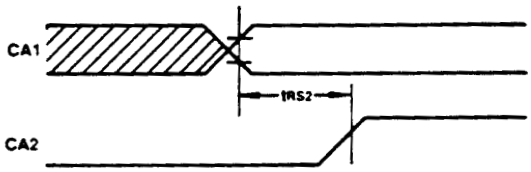


Figure 5. CA1/CA2 Timing

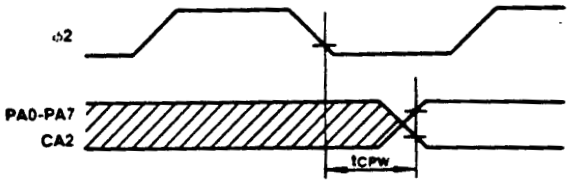


Figure 8. PA Port Delay Time

Timing Diagrams (continued)

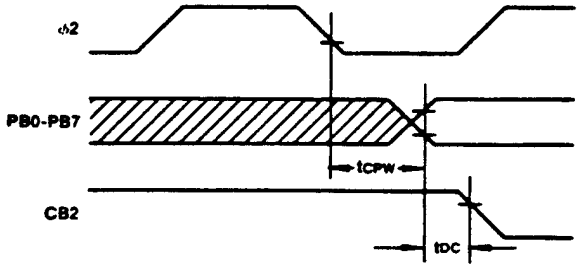


Figure 9. PB Port Delay Time

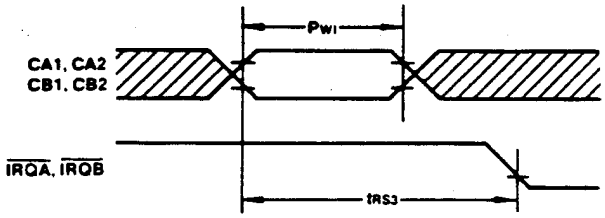


Figure 10. Interrupt Timing

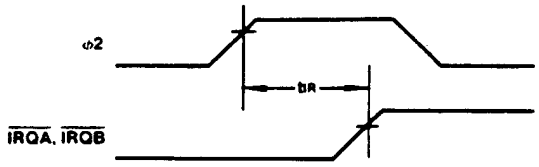
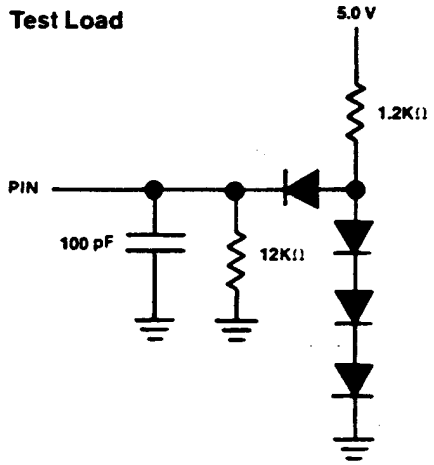
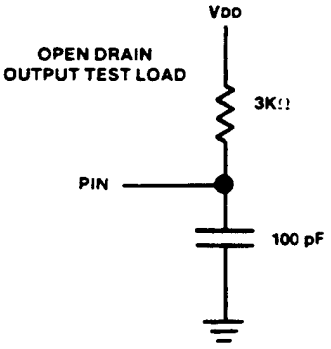


Figure 11. Interrupt Clear Timing





	7	6	5 4 3	2	1 0
CRA	IRQA1	IRQA2	CA2 Control	DDRA Access	CA1 Control
	7	6	5 4 3	2	1 0
CRB	IRQB1	IRQB2	CB2 Control	DDRB Access	CB1 Control

Figure 12. Control Registers

REGISTER SELECT PIN		DATA DIRECTION REGISTER ACCESS CONTROL BIT		
RS1	RS0	CRA-2	CRB-2	REGISTER SELECTED
0	0	1	—	Peripheral Interface A
0	0	0	—	Data Direction Register A
0	1	—	—	Control Register A
1	0	—	1	Peripheral Interface B
1	0	—	0	Data Direction Register B
1	1	—	—	Control Register B

Figure 13. Register Addressing

Signal Description

Data Bus (D0-D7)
The eight bidirectional data bus lines are used to transfer data between the G65SC21 and the microprocessor.

During a Read operation, the contents of the G65SC21 internal Data Bus Buffer (DBB) are transferred to the microprocessor via the Data Bus lines. During a Write operation, the Data Bus lines represent high impedance inputs over which data is transferred from the microprocessor to the Data Input Register (DIR). The Data Bus lines are in the high impedance state when the G65SC21 is unselected.

Chip Select (CS0, CS1, $\overline{CS2}$)
Normally, the three Chip Select lines are connected to the microprocessor address lines. This connection may be either direct or through an external decoder. To access the G65SC21, CS0 and CS1 must be high (Logic 1) and $\overline{CS2}$ must be low (Logic 0).

Register Select (RS0, RS1)
The Register Select inputs allow the microprocessor to select G65SC21 internal registers as presented in Figure 13.

Read/Write (R/$\overline{W}$)
The Read/Write signal is generated by the microprocessor and is used to control the transfer of data between the G65SC21 and the microprocessor. When R/$\overline{W}$ is in the high state (Logic 1) and the chip is selected, data is transferred from the G65SC21 to the microprocessor (Read operation). Conversely, when R/$\overline{W}$ is in the low state (Logic 0), data is transferred from the processor to the selected G65SC21 internal register (Write operation). Read/Write must always be preceded by Chip Select (CS0, CS1 and $\overline{CS2}$).

Input Clock (ϕ2)
The system ϕ2 Input Clock controls all data transfers between the G65SC21 and the microprocessor.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)
The Interrupt Request ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B) output signals become true (Logic 0) whenever an internal interrupt condition is determined by Interrupt Status Control Registers A and B. These two signals are active low and have open-drain outputs. The open-drain configuration allows the Interrupt Request signals to be wire-ORed to a common microprocessor $\overline{IRQ}$ input line.

Reset ($\overline{RES}$)
A low signal (Logic 0) on the Reset line serves to initialize the G65SC21, clearing all internal registers and placing all peripheral interface lines (PA and PB) in the input state.

Peripheral Data Port A (PA0-PA7)
Peripheral Data Port A is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Each data port bus line may be individually programmed as either an input or output under control of the Data Direction Register (DDRA). Data flow direction may be selected on a line-by-line basis with intermixed input and output lines within the same port.

Peripheral Data Port B (PB0-PB7)
Peripheral Data Port B is an 8-line, bidirectional bus used for the transfer of data, control and status information between the G65SC21 and a peripheral device. Functional operation is identical to Peripheral Data Port A, thus allowing the G65SC21 to independently control two peripheral devices.

Interrupt Status Control— CA1, CA2 (Port A) and CB1, CB2 (Port B)
The two Interrupt Status Control lines for each Data Port are controlled by the Interrupt Status Control logic (A and B). This logic interprets the contents of the corresponding Control Register (CRA and CRB), allowing the Interrupt Status Control lines to perform various peripheral control functions.

Functional Description

Organization of the G65SC21 consists of two independent control sections (A and B). Section A and Section B are identical—each consisting of a Control Register (CRA and CRB), Data Direction Register (DDRA and DDRB), Output Register (ORA and ORB), Interrupt Status Control (A and B) and Peripheral Interface Buffers (A and B). The Data Bus Buffers (DBB), Data Input Register (DIR) and the Chip Select and Read/Write control logic is common to both sections. Refer to the Block Diagram on Page 1.

Data Input Register (DIR)
During a Write data operation, the microprocessor writes data into the G65SC21 by placing data on the Data Bus. This data is then latched into the Data Input Register by the Phase Two (ϕ2) clock. Once in the Data Input Register, this data byte is transferred into one of six internal registers. This data transfer occurs after the trailing edge of the ϕ2 clock pulse that latched the data byte into the Data Input Register. This timing delay guarantees the data on the peripheral output lines (PA or PB) will make a smooth transition from low to high or high to low, and the output voltage will remain stable when there is to be no change in polarity.

Control Registers (CRA and CRB)
The individual Control Registers allow the microprocessor to program the operation of the Interrupt Control inputs (CA1, CA2, CB1, and CB2), and the Peripheral Control outputs (CA2 and CB2). Refer to Figure 4. Bit 2 in each Control Register controls the addressing of the Data Direction Registers (DDRA and DDRB) and also the Output Registers (ORA and ORB). Bits 6 and 7 are interrupt flag bits which indicate the status of the Interrupt Status Control input lines (CA1, CA2, CB1, and CB2). These two interrupt status flags are normally interrogated by the microprocessor during the interrupt service routine to determine the source of an active interrupt. These two interrupt lines drive the interrupt input ($\overline{IRQ}$ and $\overline{NMI}$) of the microprocessor.

Interrupt Status Control Logic (A and B)
The G65SC21 contains four interrupt/peripheral control lines (CA1, CA2, CB1, and CB2). These lines are controlled by the Interrupt Status Control logic (A and B). The Interrupt Status Control logic serves to interpret the contents of the corresponding Control Register, thus allowing these lines to perform various control functions as described in Figure 16.

Data Direction Registers (DDRA and DDRB)
By use of the Data Direction Registers (DDR), the microprocessor can program each individual peripheral I/O Port line as an input or output. Each bit within the register controls a corresponding line of the I/O Port, with DDRA controlling peripheral I/O Port A and DDRB controlling I/O Port B. A programmed "0" in any bit position of a DDR results in the corresponding I/O Port line being designated as an input. A "1" results in the line being an output.

Peripheral Output Registers (ORA and ORB)
All output data to a peripheral is stored in the corresponding Output Register (ORA or ORB). This data is then presented to the Peripheral Interface Buffer (A and B) and placed on the respective I/O Port lines. Writing a "0" into any bit position of ORA or ORB results in the corresponding peripheral I/O Port line going low (<0.4V), providing that particular line is programmed as an output. Writing a "1" into a bit position results in the corresponding output going high.

Register Access and Selection

Register Select lines RS0 and RS1 are used in combination with Chip Select to access the six function registers within the G65SC21. These lines are normally connected to the microprocessor address output lines. As can be seen from Figure 13, the Register Select lines are used in combination with bit 2 of the Control Registers (CRA and CRB) to access the Data Direction Registers (DDRA and DDRB) and the peripheral interface Output Registers (ORA and ORB). If bit 2 is a Logic 1, a Peripheral Output Register is selected, and if bit 2 is a Logic 0, a Data Direction Register is selected. Thus, with appropriate addressing the microprocessor can write directly into the Control Registers, the Data Direction Registers, and the peripheral interface Output Registers. Also, the microprocessor can read the contents of the Control Registers and the Data Direction Registers.

Data Access—Peripheral I/O Port A

Depending on the contents of Data Direction Register A, the eight lines of Peripheral I/O Port A may be programmed as either inputs or outputs. When a particular line(s) is programmed as an output, it will reflect the contents of the corresponding bit in peripheral Output Register A (ORA). When programmed as inputs, these lines will reflect the logic state of corresponding peripheral input data. Lines programmed as inputs are not affected by the peripheral Output Register (ORA). To perform a Read operation (RS1 = 0, RS0 = 0, and Data Direction Register Access Control bit (CRA-2) = 1), data on peripheral I/O Port A lines is directly transferred to the microprocessor via the Data Bus. The transferred byte will contain both input and output data from all eight I/O Port A lines. It is the responsibility of the microprocessor to recognize and interpret only those bits which are important to a particular peripheral operation being performed. Note that the microprocessor always reads the I/O Port A "pins" and not the contents of the ORA. This being the case, the actual data read into the microprocessor may differ from the contents of the peripheral ORA, i.e., for a particular data "output" line. This condition occurs when the I/O pin is not allowed to reach a full +2.4 volts DC for a Logic 1. When this occurs, the microprocessor will read a Logic 0, even though the corresponding bit in the peripheral ORA is a Logic 1.

Data Access—Peripheral I/O Port B

When reading peripheral I/O Port B, a combination of input and output data is read in a similar manner to peripheral I/O Port A above. The major difference is that for I/O Port B, data is read directly from peripheral Output Register B (ORB) for those lines programmed as outputs. This being the case, it is possible to load down I/O Port B lines without causing incorrect data to be transferred to the microprocessor during a Read operation.

Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$)

Both Interrupt Request ($\overline{IRQA}$, $\overline{IRQB}$) lines are active low, and serve to interrupt the microprocessor either directly or through external interrupt priority circuitry. Each line is "open drain" and is capable of sinking 3.2 milliamps from an external source, thus allowing all interrupts to be tied together in a wired-OR configuration. Each Interrupt Request line is assigned to a particular Peripheral Interface I/O Port ($\overline{IRQA}$ for Port A, and $\overline{IRQB}$ for Port B). Two interrupt flag bits are used with each Interrupt Request line. When true, these flag bits cause the Interrupt Request line to go low. The flag bits (bits 6 and 7 in each of the two Control Registers) act as the link between the peripheral interrupt signals and the microprocessor interrupt inputs. Each flag has a corresponding interrupt disable bit which allows the microprocessor to enable or disable the interrupts from each of the four interrupt inputs, i.e., CA1, CA2, CB1 and CB2. Each interrupt flag is set by an active transition on the interrupt input (CA1, CA2, CB1 and CB2).

Interrupt A Control ($\overline{IRQA}$)

Bit 7 of Control Register A is always set by an active transition of the CA1 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 0 of Control Register A to a Logic 0. Bit 6 of Control Register A is always set by an active transition of the CA2 interrupt control signal. This flag can be prevented from interrupting (disabled) by setting bit 3 of Control Register A to a Logic 0.

Both bit 6 and bit 7 in Control Register A are reset by a "Read Peripheral Output Register A" operation. To perform this Read operation, the proper Chip Select and appropriate Register Select signals must be present.

Interrupt B Control ($\overline{IRQB}$)

The control of Interrupt Request B ($\overline{IRQB}$) is performed in the same manner as that described above for $\overline{IRQA}$, except that for I/O Port B, Control Register bit 7 is set by an active transition on CB1 and interrupt enable/disable is controlled by Control Register bit 0. Control Register bit 6 is set by CB2 and its enable/disable is controlled by Control Register bit 3. Here again, both bit 6 and bit 7 in Control Register B are reset by a "Read Peripheral Output Register B" operation. Note that the interrupt disable bits (CRB bits 0 and 3) allow the microprocessor to control the interrupt function.

Interrupt Control Summary

$\overline{IRQA}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1
$\overline{IRQB}$ goes low when CRA-7 = 1 and CRA-0 = 1 or when CRA-6 = 1 and CRA-3 = 1

Peripheral I/O Ports

The G65SC21 provides two 8-bit bidirectional Data Ports (PA and PB) and four interrupt/control lines (CA1, CA2, CB1 and CB2) for interfacing to peripheral devices. Peripheral I/O Port A and I/O Port B allow the microprocessor to interface the peripheral device input lines by loading data into the corresponding Peripheral Output Register. The microprocessor interfaces the peripheral device output lines by reading data on the I/O Port input lines directly onto the Data Bus and into the internal registers of the microprocessor.

Peripheral I/O Port A (PA0-PA7)

Each Peripheral I/O Port line can be programmed to act as an input or an output, as determined by the corresponding bits in the Data Direction Register. Within the Data Direction Register, a Logic 1 in a particular bit position represents an output line. Likewise, a Logic 0 in a particular bit position represents an input line. The Data Buffers which drive the I/O Port A lines contain "active" pull-up transistors as shown in Figure 14. Since these pull-ups are p-channel transistors they allow the output voltage to go to V_{DD} for a Logic 1. Also, since these switches can sink a full 3.2 milliamp, the buffers are capable of driving one standard TTL load. In the input mode, the pull-up devices shown in Figure 14 remain connected to the I/O pin and continue to supply current to the pin. For this reason, these lines represent one standard TTL load in the input mode.

Peripheral I/O Port B (PB0-PB7)

The lines of Peripheral I/O Port B function in a similar manner to the discussion of I/O Port A above. Programmed selection for input/output function is identical. There are, however, several characteristics of the buffers driving these lines which affect their use in peripheral interfacing. Peripheral I/O Port B buffers are push-pull devices as shown in Figure 15.

The active pull-up devices can source up to 3 milliamp at 1.5 volts. This current drive capability is provided to allow direct connection to Darlington transistor switches. This allows

convenient control of relays, lamps, etc. Because the I/O Port B outputs are designed to drive transistors directly, the output data is read directly from Peripheral Output Register B for those lines programmed as inputs. The I/O Port B push-pull buffers also provide a high impedance input state. When these lines are programmed as inputs, the output buffer enters the high impedance state.

Interrupt Input/Peripheral Control Lines (CA1, CA2, CB1 and CB2)

The G65SC21 contains four interrupt input/peripheral control lines (CA1, CA2, CB1 and CB2) which offer a number of special peripheral control functions. These functions greatly enhance the performance of the two I/O Ports. Refer to Figure 16 for a summary of control line operation.

I/O Port A Interrupt Input/Peripheral Control Lines (CA1, CA2)

Line CA1 is an interrupt input only. An active transition on this line will set bit 7 in Control Register A to a Logic 1. This flag bit (bit 7) can be programmed to set on either a positive or negative CA1 transition. Bit 7 will be set on a negative transition if bit 1 in the Control Register is set to a Logic 0. Likewise, bit 7 can be set on a positive transition if bit 1 in the Control Register is set to a Logic 1.

It should be noted that a negative transition is defined as a transition from high to low, and a positive transition is a transition from low to high.

Setting the interrupt flag (bit 7 or the Control Register) will interrupt the microprocessor via $\overline{IRQA}$ if bit 0 in Control Register A is a Logic 1 as described in earlier paragraphs.

Line CA2 can act as a totally independent interrupt input or as a peripheral control output. CA2 acts as an interrupt input when Control Register A bit 5 is a Logic 0. In this case, CA2 will set the interrupt flag (bit 6 of Control Register A) to a Logic 1 on the active transition as selected by bit 4 of the Control Register. The Control Register bits and interrupt inputs serve the same basic function as that described above for CA1. The input transition sets the interrupt flag which serves as the link between the microprocessor interrupt configuration and the peripheral device. The interrupt disable bit allows the microprocessor to exercise control over the system interrupts.

CA2 serves in the output control mode when Control Register A bit 5 is a Logic 1. In this case, CA2 can operate independently to generate a sample pulse each time the microprocessor reads data on I/O Port A. This mode is selected by setting bit 4 of the Control Register to a Logic 0 and bit 3 to a Logic 1. This pulse output is normally used to control counters, shift registers, etc. which provide sequential data to the peripheral input lines.

A second output mode allows CA2 to be used in conjunction with CA1 to "handshake" between the peripheral device and the microprocessor. With respect to I/O Port A, this "handshake" allows positive control of data transfers from the peripheral device into the microprocessor. The "handshake" function operates as follows:

The CA1 input signals the microprocessor that data is available by interrupting the microprocessor. The microprocessor then reads the data and sets CA2 to a Logic 0. This signals the peripheral device that it can now place new data on the I/O Port line.

A third output mode can be selected by setting Control Register bit 4 to a Logic 1. In this mode, CA2 is a simple peripheral control output which can be set high or low by setting bit 3 of Control Register A to a Logic 1 or a Logic 0 respectively.

I/O Port B Interrupt Input/Peripheral Control Lines (CB1, CB2)

The CB1 line operates as an interrupt input only in the same manner as CA1 above. In this case, bit 7 of Control Register B is set by the active transition on CB1 as selected by bit 0 of the Control Register. The CB2 input modes operate identical to the CA2 input modes. However, the CB2 output modes (Control Register B bit 5 set to Logic 1) differ somewhat from those of CA2. That is, the pulse ouput occurs when the microprocessor writes data into Output Register B. Also, the "handshaking" operates on data transfers from the microprocessor into the peripheral device.

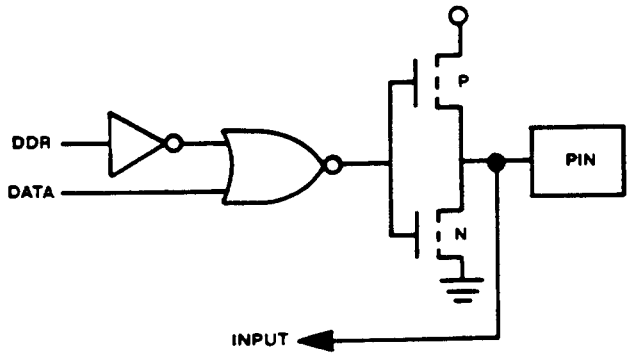


Figure 14. Port A Buffer Circuit (PA0-PA7)

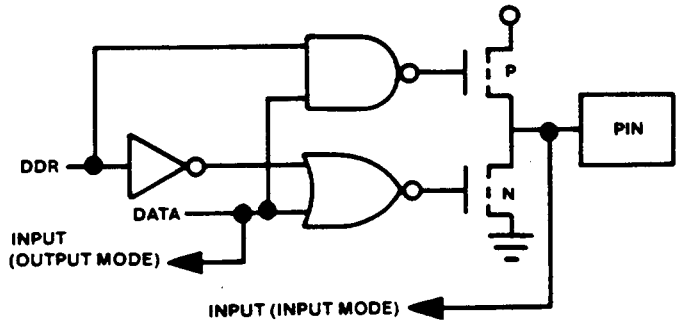


Figure 15. Port B Buffer Circuit (PB0-PB7)

CA1/CB1 CONTROL			
CRA (CRB)		ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
BIT 1	BIT 0		
0	0	Negative	Disable—remain high
0	1	Negative	Enable—goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	Positive	Disable—remain high
1	1	Positive	Enable—as explained above

*Note: Bit 7 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES				
CRA (CRB)			ACTIVE TRANSITION OF INPUT SIGNAL*	$\overline{IRQA}$ ($\overline{IRQB}$) INTERRUPT OUTPUTS
BIT 5	BIT 4	BIT 3		
0	0	0	Negative	Disable—remains high
0	0	1	Negative	Enable—goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	Positive	Disable—remains high
0	1	1	Positive	Enable—as explained above

*Note: Bit 6 of CRA (CRB) will be set to a Logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of bit 0 in CRA (CRB).

CA2 OUTPUT MODES				
CRA			MODE	DESCRIPTION
BIT 5	BIT 4	BIT 3		
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES				
CRB			MODE	DESCRIPTION
BIT 5	BIT 4	BIT 3		
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

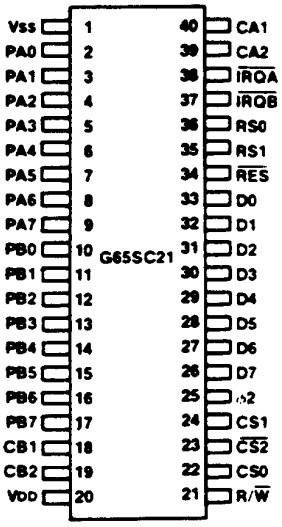
Figure 16. Interrupt Input/Peripheral Control Lines Operation

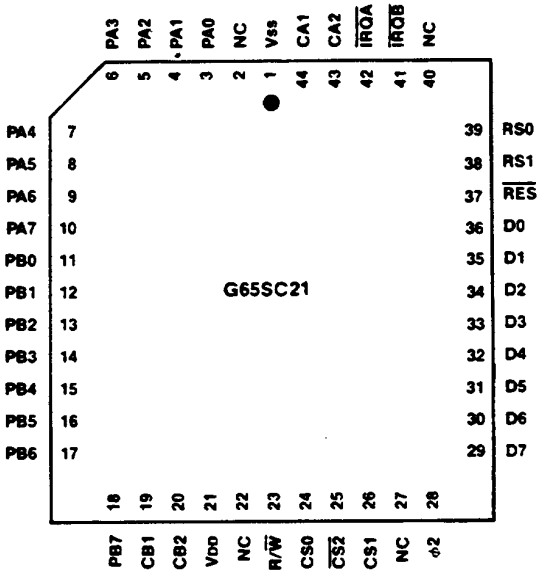
Pin Function Table

Pin	Description
D0-D7	Data Bus
PA0-PA7	Peripheral I/O Port A
PB0-PB7	Peripheral I/O Port B
$\phi 2$	Phase 2 Internal Clock
$\overline{RES}$	Reset
R/$\overline{W}$	Read/Write
$\overline{IRQA}$	Interrupt Request (Port A)

Pin	Description
$\overline{IRQB}$	Interrupt Request (Port B)
CS0, CS1, $\overline{CS2}$	Chip Select Inputs
RS0, RS1	Register Selects
CA1, CA2	Peripheral A Control Lines
CB1, CB2	Peripheral B Control Lines
VDD	Positive Power Supply (+5V)
VSS	Internal Logic Ground

Pin Configuration





Ordering Information