CMOS Communications Terminal Unit (Telecommunication Microcomputer)

Features

- Generates signals compatible with switched telephone networks or packet switched data networks
- Provides Dial Pulse (DP), Dual Tone Multi-Frequency (DTMF), and 0-600 baud modem signaling capabilities
- Low power mode (300 μA) enables telephone line-powered operation
- External microprocessor address and data bus facilitates memory and I/O expansion
- On-chip memory: 2K bytes ROM
  64 bytes RAM
- Standard DTMF and modem frequencies can be generated which are accurate to ±1.0% with a 3.58 MHz crystal
- Two sine wave generators
- 6800 and 6500 bus compatibility
- Utilizes G65SC00 microprocessor as CPU
- 27 TTL compatible I/O lines
- Bus expandable to address 65K bytes of external memory
- Single +5 volt power supply
- Available in 68-pin chip carriers

General Description

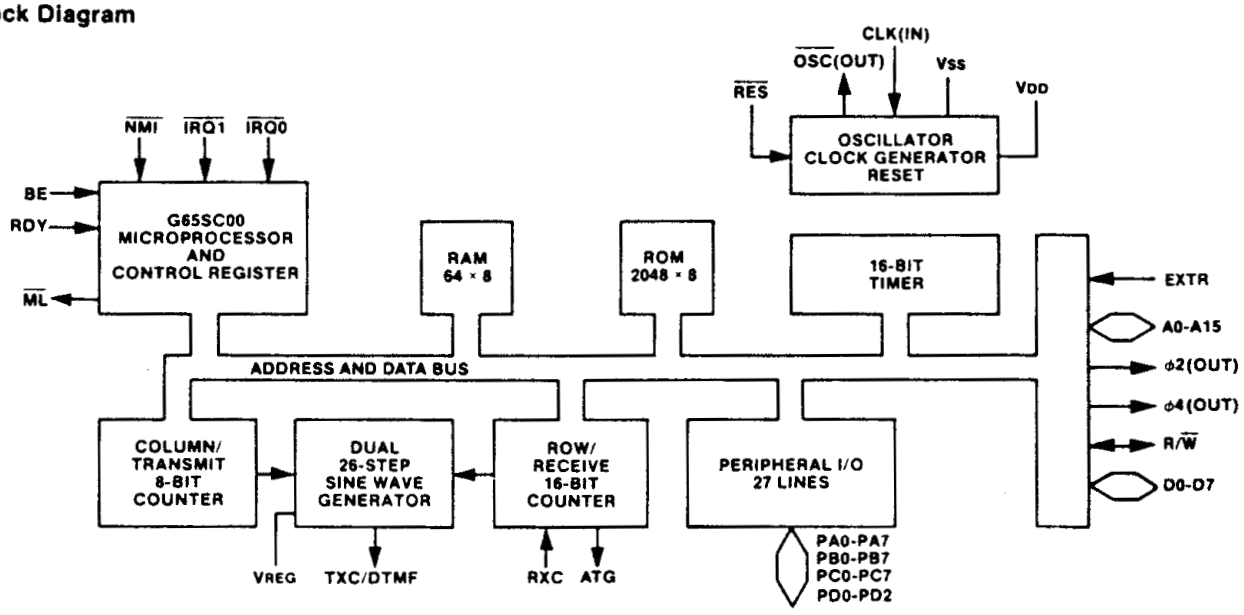
The CMD G65SC150 Communications Terminal Unit (CTU) is a single chip telecommunications microcomputer manufactured using state-of-the-art silicon gate CMOS process technology, which is optimized for telephone line signaling and data transmission applications. A functional block diagram is shown which illustrates the major system functions that are included on the integrated circuit.

The CTU uses the CMD G65SC00 8-bit microprocessor which executes the complete G65SC00 series instruction set. With 2K bytes of ROM and 64 bytes of RAM, the CTU operates as a single-chip microcomputer.

The internal bus interconnects all microcomputer functions. The address and databus buffers permit expansion of ROM, RAM and memory mapped I/O using the full 65K addressing space of the microprocessor. A peripheral mode is available for use with multiprocessor systems. A test and prototyping mode switches internal ROM addresses to external access. An on-chip oscillator may be driven by an external clock source.

The telecommunications interface circuitry consists of a timer, row/receive counter, column/transmit counter and dual sine wave generators. In addition, 27 general purpose I/O lines can be used for keyboard, telephone Dial Pulse (DP) signaling, phone line control, and other peripheral devices.

Block Diagram



Absolute Maximum Ratings: (Note 1)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.3 to +7.0	V
Input Voltage	V_{IN}	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-40 to +85	°C
Storage Temperature	T_S	-65 to +150	°C
Regulated Voltage	V_{REG}	-0.3 to V_{DD} + 0.3	V

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

Notes:
1. Exceeding these ratings may result in permanent damage. Functional operation under these conditions is not implied.

DC Characteristics: All signals except TXC/DTMF, V_{DD} = 5.0V ± 10% unless otherwise stated, T_A = -40°C to +85°C

Parameter	Symbol	Min	Max	Units
Input High Voltage	V_{IH}			
CLK (IN)		2.4	V_{DD} + 0.3	V
All Other Inputs		2.0	V_{DD} + 0.3	V
Input Low Voltage	V_{IL}			
CLK (IN)		-0.3	0.4	V
All Other Inputs		-0.3	0.8	V
Output High Voltage	V_{OH}	2.4		V
Address, Data, R/W (I_{OH} = -100µA)				
Peripheral I/O				
Option B (I_{OH} = -10 µA)				
Option C (I_{OH} = -200µA)				
Option D (I_{OH} = -1.0mA)				
Output Low Voltage (I_{OL} = 3.2mA)	V_{OL}		0.4	V
Input Leakage Current (V_{IN} = 0 to V_{DD}), No Pullup Option, RES, NMI, IRQ0, IRQ1, RDY, BE, CLK(IN)	I_{IN}		±1.0	µA
Three-State Leakage Current (V_{IN} = 0.4 to 2.4V), I/O Ports	I_{TSI}		±10.0	µA
Pull Down Current (Control Register Bit 5 = 0)	I_{PD}		20	µA
Input Pullup Current (Inputs with Pullup Option), RES, NMI, IRQ0, IRQ1, RDY, BE	I_{PLP}	-20.0		µA
Input High Current (V_{IH} = 2.4V)	I_{IH}			
Option A		0		µA
Option B		-10		µA
Option C		-200		µA
Input Low Current (V_{IL} = 0.4V)	I_{IL}			
Option B			-100	µA
Option C			-2.4	mA
Output Source Current (V_{OH} = 1.5V)	I_{OH}			
I/O Ports Option D		3.0		mA
Supply Current	I_{DD}			
Standby Mode (No Clock, V_{DD} = 3.0V)			300	µA
4 MHz (ϕ2 = 10 KHz — Bus Off)			1	mA
4 MHz (ϕ2 = 1 MHz — Bus Off)			4	mA
4 MHz (ϕ2 = 1 MHz — Bus On)			6	mA
8 MHz (ϕ2 = 2 MHz — Bus On)			11	mA
Supply Current (V_{REG} = V_{DD})	I_{REG}		1.7	mA
Capacitance (V_{IN} = 0V, T_A = 25°C, F = 1 MHz)				
A0-A15, R/W, Data (Off State)	C_{TS}		15	pF
All Other Signals	C_{IN}		10	pF

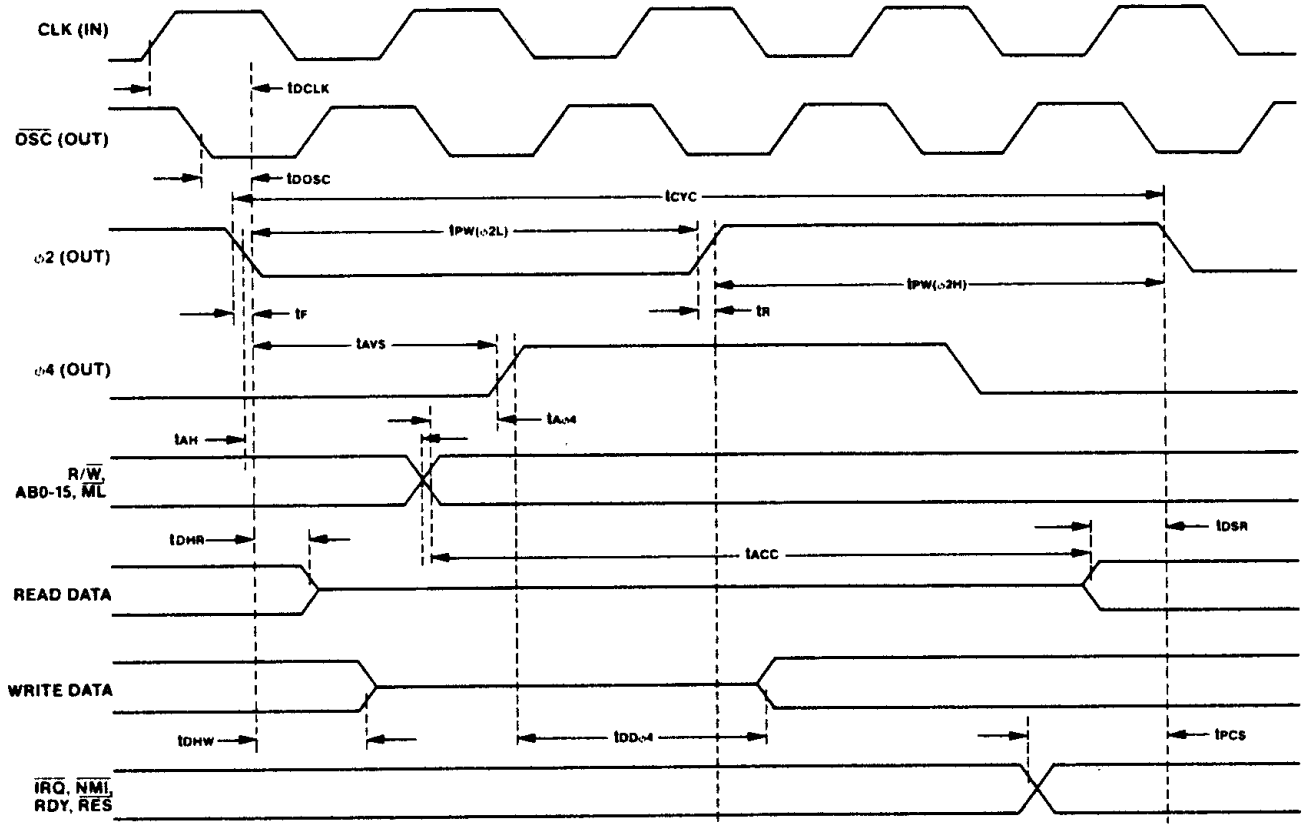
AC Characteristics: V_{DD} = 5.0V ± 10%, T_A = -40° C to +85° C

Parameter	Symbol	1 MHz		2 MHz		Units
		Min	Max	Min	Max	
Delay Time, CLK(IN) to ϕ2(OUT)	t_{DCLK}	—	100	—	100	nS
Delay Time, OSC(OUT) to ϕ2(OUT)	t_{DOSC}	—	75	—	75	nS
Cycle Time	t_{CYC}	1.0	DC	0.50	DC	µS
Clock Pulse Width Low	$t_{PW(\phi 2L)}$	470	—	240	—	nS
Clock Pulse Width High	$t_{PW(\phi 2H)}$	470	—	240	—	nS
Fall Time, Rise Time	t_F, t_R	—	25	—	25	nS
Delay Time, ϕ2(OUT) to ϕ4(OUT)	t_{AVS}	—	250	—	125	nS
Address Valid to ϕ4(OUT)	$t_{A\phi 4}$	50	—	25	—	nS
Address Hold Time	t_{AH}	10	—	10	—	nS
Access Time	t_{ACC}	695	—	340	—	nS
Read Data Hold Time	t_{DHR}	10	—	10	—	nS
Read Data Setup Time	t_{DSR}	90	—	90	—	nS
Write Data Hold Time	t_{DHW}	30	—	30	—	nS
Write Data Delay Time	$t_{DD\phi 4}$	—	200	—	110	nS
Processor Control Setup Time	t_{PCS}	90	—	90	—	nS
Select, R/W Setup	t_{AC}	160	—	90	—	nS
Select, R/W Hold	t_{CA}	0	—	0	—	nS
Data Bus Delay	t_{CDR}	—	320	—	180	nS
Data Bus Hold	t_{HR}	10	—	10	—	nS
Data Bus Setup	t_{DCW}	195	—	90	—	nS
Data Bus Hold	t_{HW}	10	—	10	—	nS

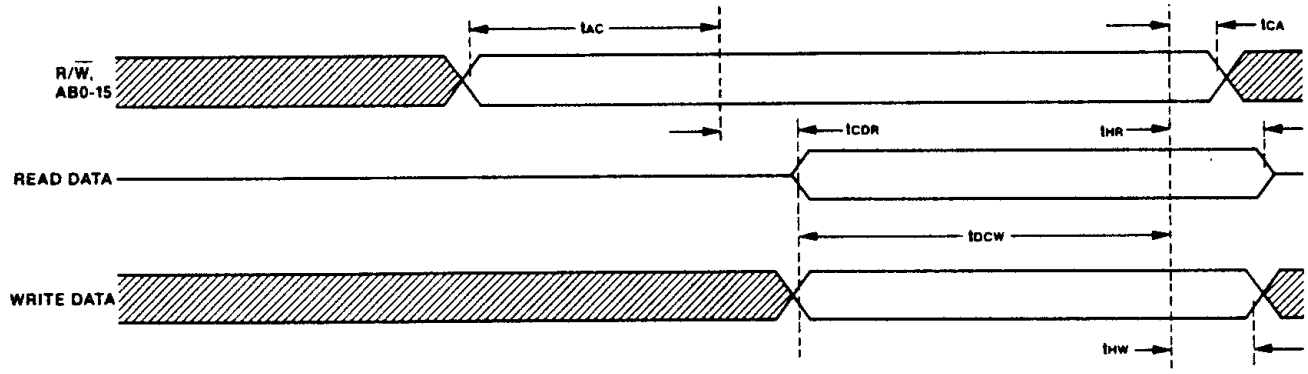
AC Characteristics, TXC/DTMF Output: V_{REG} = V_{DD}, R_L = 10KΩ, V_{DD} = 5.5V

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Row Tone	V_{OR}	303	340	382	mVrms	
Column and Transmit Tone	V_{OC}	392	440	494	mVrms	
Pre-emphasis, DTMF High Group	PE_{HB}	1.0	2.0	3.0	dB	
DTMF Total Distortion	DIS_T			-25	dB	Total out-of-band power relative to sum of Row and Column fundamental power.
DTMF Single Frequency Distortion	DIS_S			-30	dB	0 to 3.4 KHz band. (Any spectral component.)
Idle Noise	V_{IDLE}			-80	dB	

Timing Diagram



Peripheral Mode Timing



Notes: 1. Load = 100 pF.
2. Voltage levels shown are $V_L \leq 0.4V$, $V_H \geq 2.4V$, unless otherwise specified.
3. Measurement points shown are 0.8V and 2.0V, unless otherwise specified.
4. T_{AH} measured at 1.5V.

Characteristic Curve

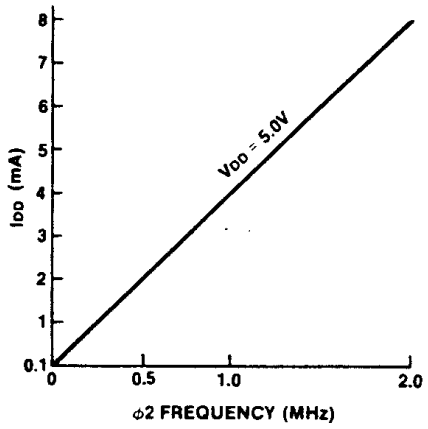


Figure 1. Typical Supply Current (I_{DD}) Versus φ2 Frequency—Microprocessor Only

Test Circuits

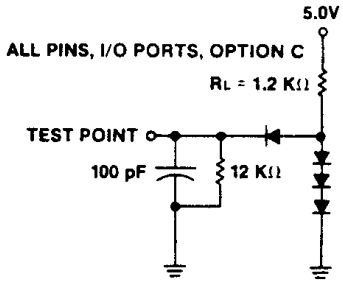


Figure 2(a). Test Load

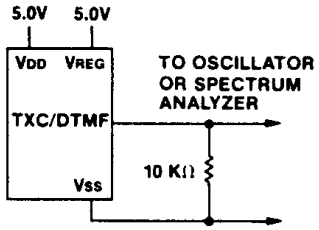


Figure 2(b). Audio Test Load

Signal Description

Microprocessor Signals

Interrupt Request ($\overline{IRQ0}$, $\overline{IRQ1}$)—These TTL compatible signals (bidirectional, active low—two lines) request that an interrupt sequence begin within the microprocessor. The $\overline{IRQ}$ signals are sampled during φ2(OUT) operation. If the interrupt flag in the status register is zero, the current instruction is completed and the interrupt sequence begins when φ2(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no other maskable interrupts occur. The program counter is loaded with the interrupt vector thereby transferring program control to an interrupt routine. Interrupt and vector addresses are shown in Figure 3. Note that this is a level sensitive input. As a result, another interrupt will occur as soon as the interrupt flag is cleared if $\overline{IRQ}$ remains low. No interrupt will occur when the interrupt flag is cleared and $\overline{IRQ}$ is high but was low prior to clearing the flag. Also note that these are bidirectional signals which are "wire-ORed" with both internal and external interrupt sources. The signals are decoded to form three separate interrupt vector addresses as shown in Figure 3. Since these signals are "wire-ORed" for both internal and external interrupts, the generation of internal interrupts will cause high and low logic level swings at the $\overline{IRQ}$ pins. As outputs, these signals serve to indicate that a specific internal interrupt has occurred. This being the case, caution should be used to prevent connecting these signals to external circuitry which could falsely respond to an internal interrupt condition.

Vector Address	Description	Comment
FFFE, F	Break	Software Interrupt
FFF8, 9	Row/Receive Counter	Pulls $\overline{IRQ0}$ and $\overline{IRQ1}$ Low
FFFA, B	External	$\overline{IRQ1}$
FFFC, D	Timer/Counter	Pulls $\overline{IRQ0}$ Low
FFEE, F	Reset	$\overline{RES}$
FFEC, D	Non-Maskable	$\overline{NMI}$

Figure 3. Interrupt and Vector Addresses

Non-Maskable Interrupt ($\overline{NMI}$)—A negative-going edge on this input, active low signal unconditionally starts a non-maskable interrupt sequence within the microprocessor. The $\overline{NMI}$ signal is sampled during φ2(OUT) operation. The current instruction is completed and the interrupt sequence begins when φ2(OUT) goes low. The program counter and processor status register are stored in the stack. The interrupt flag is set so that no maskable interrupts occur. The program counter is loaded with the interrupt vector from locations FFEC (low byte) and FFED (high byte), thereby transferring program control to the non-maskable interrupt routine. Note that this is an edge-sensitive input. As a result, another interrupt will occur if there is another negative-going transition and the program has not returned from a previous interrupt. No interrupt will occur if $\overline{NMI}$ is low and a negative-going edge has not occured since the last non-maskable interrupt.

Bus Enable (BE)—When this input, active high signal is high, (R/$\overline{W}$) is an output, indicating internal control of read and write operations. When BE is low, the address/data bus is reversed allowing access to internal ROM, RAM and I/O from an external device. R/$\overline{W}$ becomes an input, controlling the internal read and write operations. The φ2(OUT) and φ4(OUT) outputs are used for system timing. BE is also used to switch the computer to the test and prototype mode. During processor initialization, BE is high before Reset ($\overline{RES}$) goes high for normal operation. When in the Test and Prototype Mode, internal ROM may be disabled, thus allowing the use of external memory addresses F800 through FFFF. To initiate the Test and Prototype Mode, BE must be held low while bringing Reset high. Note that BE must remain low for at least one clock cycle after Reset becomes high. For additional information, refer to the Test and Prototype Mode section under Operating Modes.

Ready (RDY)—This input, active high signal provides a single cycle stepping capability and allows operation with slow memory devices for read or write cycles. If this signal is low when φ2(OUT) is low, the processor will stop when φ2(OUT) goes high. The address and data lines remain at their current state. When RDY goes high, the processor resumes operation.

Memory Lock ($\overline{ML}$)—This signal is an active low output and, in a multiprocessor system, $\overline{ML}$ indicates the need to defer the rearbitration of the next bus cycle to ensure the integrity of read-modify-write instructions. $\overline{ML}$ goes low during ASL, DEC, INC, LSR, ROL, ROR, TRB and TSB memory referencing instructions. This signal is low for two cycles: the modify and write cycles, and is available as a metal mask option in place of PD2.

Bus Signals

Address Bus (A0-A15)

Output (BE = 1)
A0-A15 forms a three-state, 16-bit, input/output, active high address bus (65,536 locations) for memory and I/O exchanges on the data bus. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Input (BE = 0)
These lines drive the internal address decoder to select internal ROM, RAM or I/O for external read and write cycles.

Clocks (ϕ2(OUT) and ϕ4(OUT))—These output, active high signals (2 lines) provide timing for external bus read and write operations.

Data Bus (D0-D7)—D0-D7 constitute an 8-bit bidirectional active high, three-state data bus, used for data exchanges with memory and I/O. If the TSC control register bit is set, these lines are pulled to the low state by a high resistance device.

Read/Write (R/$\overline{W}$)

Output (BE = 1)
This output, active low signal is normally in the high state indicating that the CPU is reading data from memory or I/O. In the low state the data bus has valid data from the CPU to be stored at the addressed memory or I/O location. If the TSC control register bit is set, this line is pulled to ground by a high resistance device.

Input (BE = 0)
In systems where this part is used as a peripheral controller, R/$\overline{W}$ is an input, active low signal which controls the output data buffers. When R/$\overline{W}$ is high, the buffers are active and internal data is read by the external microprocessor.

Telecommunications Signals

Transmit Carrier and Dual Tone Multifrequency (TXC/DTMF)—This output signal is connected to the output of an operational amplifier which mixes the two sine wave generator outputs. In a telecommunication application, these signals may be the row and column tones used in DTMF signaling. The level of the dual-tone output is the sum of the levels of a single row and single column output. The modem Transmit Carrier (TXC) is generated by the column/transmit counter and sine wave generator. This signal level is controlled by VREG voltage reference supply and is gated by CC0, CC1, and CC2 control register bits.

Audible Tone Generator (ATG)—This output signal is derived from the carry output of the row/receive counter. The square wave output is gated by the ATG control register bit.

Receive Carrier (RXC)—When the row/receive counter is in the pulse width timer mode, this input signal generates a maskable interrupt after both positive and negative transitions. At the same time, the counter contents are transferred to the row/receive register. In this way, the time between transitions can be measured by an interrupt servicing program.

Peripheral Signals

There are 27 peripheral input/output lines: PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD2. Four memory addressable registers are associated with these signals. Depending upon the mask option chosen, the output can source either 0, 10 or 400 μA at VOH = 2.4 volts. The higher sourcing current may be used to directly drive the base of an external NPN transistor having a grounded emitter, or in a Darlington configuration.

Miscellaneous Signals

Reset ($\overline{RES}$)—A positive transition of this input, active low signal causes an initialization sequence to begin. Reset must be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition. After this time R/$\overline{W}$ is high. The I/O ports (PA, PB, PC and PD) are forced to the high state. All bits in the control register are set to zero. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. The interrupt mask flag is set and the program counter is loaded with the restart vector from locations FFEE (low byte) and FFEF (high byte).

Clock In (CLK(IN))—The microcomputer contains an internal clock generator operating at four times the ϕ2 frequency. The frequency of these clocks is externally controlled by a crystal oscillator circuit as shown in Figure 4. The internal generator may also be controlled by an input signal from any external clock source.

Oscillator Out (OSC(OUT))—An inverter whose input is CLK(IN) and output is OSC(OUT) is connected between these two clock pins. This active low inverter has sufficient loop gain to provide oscillation using a crystal. Frequency deviation, usually less than 0.05%, will affect the tone output frequency. There is a bias resistor mask option between the two pins.

External ROM(EXTR—Normally PD1)—When in the Test and Prototype Mode, the PD1 pin assumes an additional function and becomes PD1/EXTR, where an active high input selects external memory and an active low input switches back to internal ROM only. For additional information, refer to the Test and Prototype Mode section under Operating Modes.

Regulated Supply Voltage (VREG)—The D-to-A resistor networks and summing amplifier are powered by connecting VREG. The TXC/DTMF output level is directly proportional to VREG.

Internal Logic Ground (Vss)—This connection is used for the power supply internal logic ground.

Positive Supply Voltage (VDD)—This connection serves as the positive power supply input. Reset (RES) should be held low for at least two clock cycles after VDD reaches operating voltage from a power down condition.

Operating Modes

Normal Mode

In the normal mode, the internal microprocessor is operating and its memory map includes the internal 2K bytes of ROM, 64 bytes of RAM, four general purpose I/O registers, one control register and five timer/counter registers. The three-state control bit in the control register determines whether the external bus is active, thus allowing access to the full 65K addressing space.

Test and Prototype Mode

The Test and Prototype Mode provides a convenient means for system testing and debugging without the need for mask-programmed ROM. The Test and Prototype Mode enables the use of external memory at address locations normally occupied by internal ROM (F800 through FFFF), with internal ROM being disabled. In this mode, system programs can be developed using external memory for the prototype system. The program can then be developed using the same memory locations as reserved for internal ROM. Once the program has been debugged and tested, it can then be committed to internal ROM. The Test and Prototype Mode is initiated during the Reset sequence by holding Bus Enable (BE) low while bringing Reset high. Note that BE must remain low for at least one clock cycle after Reset becomes high. Also, BE must be high before the beginning of the first Vector Read cycle. During the Reset sequence, the Reset Vector will be accessed from external memory locations FFEE and FFEF. Note that the Control Register TSC bit has no effect in the Test and Prototype Mode. Also, in this mode the PD1 I/O line is assigned an additional function and becomes PD1/EXTR. An active high input on this I/O pin selects external memory, while an active low input disables external memory and places internal ROM back into the memory map.

Peripheral Mode

In the peripheral mode, internal ROM, RAM and I/O may be accessed from an external device. This mode is useful when the G65SC150 is used as a peripheral device in a microprocessor system. To enable this mode, the Bus Enable (BE) signal is held low. This stops the microprocessor and reverses the address and data buses. Read/Write becomes an input, thus allowing external control of internal read and write operations.

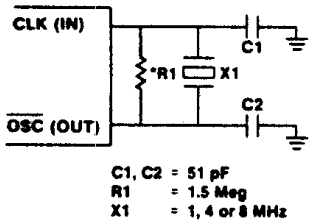
Low Power Mode

Since power consumption in CMOS circuits is directly related to operating frequency, this mode allows operation at greatly reduced power by reducing the microprocessor clock frequency. This mode is enabled by storing a value in the 16-bit Timer register and then setting the ϕ2 mode bit in the control register. The timer counter becomes a programmable clock divider. To further reduce power, the external address and data bus may be disabled by clearing the three-state control bit in the control register.

Functional Description

G65SC150 Microprocessor Unit

For a detailed functional and software programming description of the



*R1 is deleted if internal option (R ≈ 1.5 Meg) is selected.

Figure 4. Crystal Circuit for Internal Oscillator

microprocessor, refer to the data sheet for the G65SCXXX family of 8-bit microprocessors. Figure 17 (page 12) illustrates a microprocessor programming model, while a complete listing of operational codes, execution times and memory requirements is provided in Figure 19 (page 13). A brief functional description of the G65SCXXX microprocessor is as follows:

Timing Control—The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each $\phi 1$ clock pulse for as many cycles as is required to complete the instruction. Each data transfer which takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

Program Counter—The 16-bit program counter provides the addresses which step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

Instruction Register and Decode—Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

Arithmetic and Logic Unit (ALU)—All arithmetic and logic operations take place in the ALU including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

Accumulator—The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

Index Registers—There are two 8-bit index registers (X and Y), which may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction which specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible.

Stack Pointer—The stack pointer is an 8-bit register used to control the addressing of the variable-length stack. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts ($\overline{NMI}$ and $\overline{IRQ}$). The stack allows simple implementation of nested subroutines and multiple level interrupts.

Processor Status Register—The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled both by the program and the CPU. The 6500 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags.

Oscillator/Clock Generator

A functional block diagram of the oscillator/clock generator circuitry is shown in Figure 5. The circuits are described in the following three paragraphs:

Oscillator—The clock oscillator accommodates a crystal of up to 8 MHz. CLK(IN) and $\overline{OSC}$(OUT) are TTL compatible. An oscillator bias resistor between these pads is a mask option. With the resistor connected, the circuit requires only an external crystal. For an external oscillator, the resistor is disconnected to eliminate static current drain in low-power system.

Microcomputer Clock—In the maximum frequency mode ($\phi 2$ mode = 0) the oscillator frequency divided-by-four provides the microcomputer bus timing signals $\phi 2$(OUT) and $\phi 4$(OUT). The quadrature clock generator delays the $\phi 2$(OUT) signal by one oscillator period. The low-power mode ($\phi 2$ mode = 1) uses the timer counter as a programmable $\phi 2$(OUT) clock divider.

Random Access Memory (RAM)

The 64-byte memory resides in two ranges in the microcomputer address map. Address bit A8 is not decoded for the RAM, allowing addressing at both 01C0-01FF and 00C0-00EF (00F0-00FF is reserved for the telecommunication register set). In a typical program, the RAM would be partitioned for both stack addressing (01XX) and zero page addressing (00XX).

Read Only Memory (ROM)

The 2048-byte ROM is used for program and constant data storage in the microcomputer system. The ROM occupies addresses F800-FFFF in the microcomputer address map.

Control Register

The on-chip timer and counters with their associated interrupts are configured by setting bits in the control register at address 00F7 as shown in Figure 6.

A functional description of the various control register bits is contained in the following paragraphs:

Communication Mode Select—CC2, bit 2; CC1, bit 1; CC0, bit 0—These bits select one of eight operating modes for the row/receive and column/transmit registers and counters.

000—Idle Mode
Both the Row/Receive Counter (RRC) and Row/Receiver Register (RRR) are inactive, with no interrupt generated and no tone output.

001—Interval Timer Mode
In this mode, the row/receive counter is configured as an additional interval counter based on the contents of the row/receive register.

010—Pulse Width Timer Mode
In this mode, the row/receive counter is configured as a pulse width interval timer...measuring the period between transitions of the receive carrier input.

011—Single Tone Row/Tone Generator Mode
As determined by the ATG bit, a square wave is generated at the Audible Tone Generator (ATG), or a sine wave is generated which appears at the TXC/DTMF output.

100—Single Tone Column Mode
In this mode, a single frequency is generated at the TXC/DTMF output.

101—Modem
This mode is a concurrent application of the pulse width timer mode and the single tone column mode.

110—Modem—Divide-by-Two Prescaler Mode
This mode allows transmit and receive, plus low frequency transmit carrier generation.

111—Dual Tone Multifrequency Mode
This mode allows the generation of standard DTMF signaling tones.

Phase 2 Mode Select—Phase 2, Bit 3—This mode controls the frequency at which the microprocessor oscillator operates. Refer to Figure 5, Clock Functional Block Diagram.

0—Maximum Frequency Mode
The frequency at CLK (IN) divided by four is the microprocessor clock.

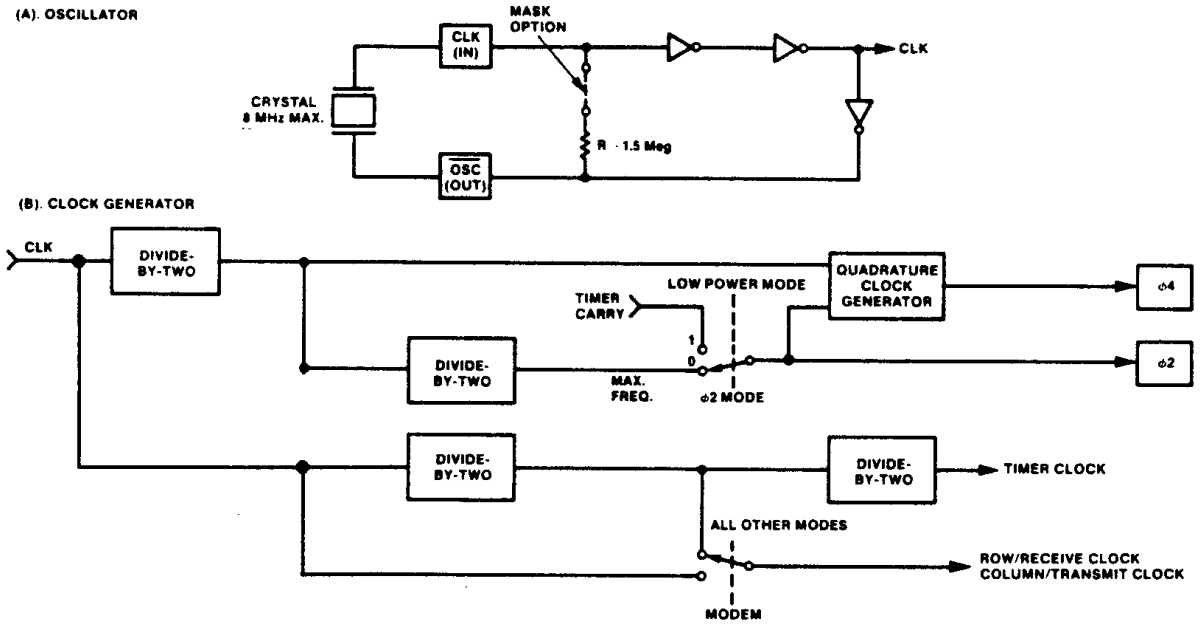


Figure 5. Clock Functional Block Diagram

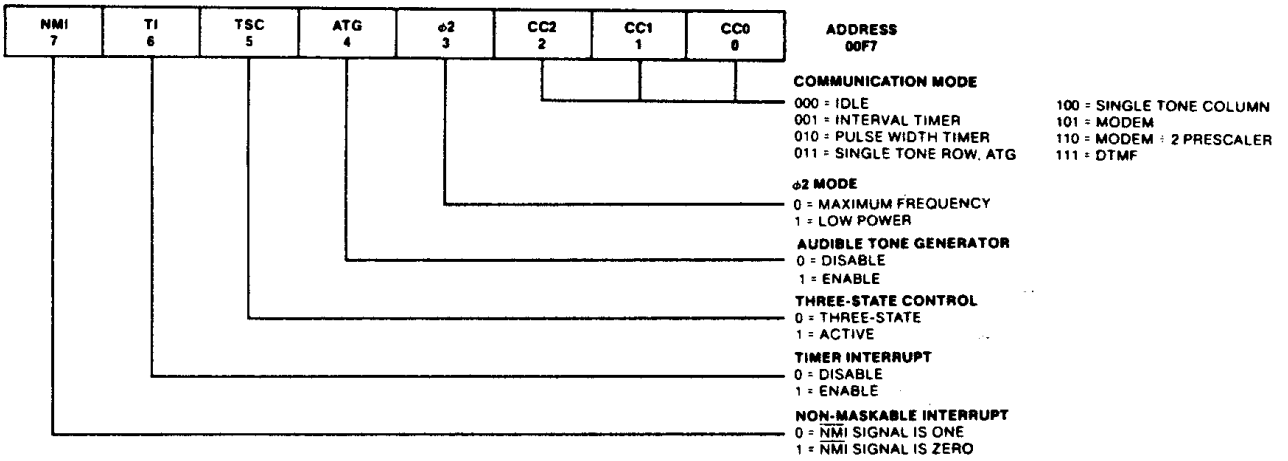


Figure 6. Control Register Functional Block Diagram

1—Low Power Mode
The timer overflow signal is the microprocessor clock. The timer clock input is the frequency CLK(IN) divided by either four or eight depending on a mask option in the clock circuitry. The timer divide ratio is the contents of the timer register plus two.

Audible Tone Generator Enable—ATG, Bit 4

0—Audible Tone Disabled

1—Audible Tone Enabled

Three-State Control Enable—TSC, Bit 5

0—Three-State
The external address and data buses and R/$\overline{W}$ are pulled to Vss by a high resistance device. In a typical application TSC is set to zero when operating in low or back-up power condition. The bus is powered down and not driven externally.

1—Bus Active

Timer Interrupt Enable—TI, Bit 6

0—Timer Interrupt Disabled
The timer register value is transferred to the counter when changing to the enabled interrupt state.

1—Timer Interrupt Enabled

Non-Maskable Interrupt Input—$\overline{NMI}$, Bit 7

0—$\overline{NMI}$ Signal = One (No Interrupt)

1—$\overline{NMI}$ Signal = Zero (Interrupt)
In a typical application this condition indicates low or back-up power system operation. The microprocessor program would monitor this condition to return to normal power operation.

Timer

The 16-bit free-running timer counter and register operates in one of two modes determined by timer interrupt signal and φ2 bits in the control register. Figure 7 illustrates the timer functional block diagram. With a 3.579545 MHz clock, the timer mode is capable of 1.1175 μS resolution. An interrupt is generated at intervals from 2.2349 μS to 73.234 mS. In the low power mode, the counter carry output becomes the microprocessor φ2(OUT) clock. Refer to Figure 18 (page 12), Microprocessor Clock Frequency and Timer Interval.

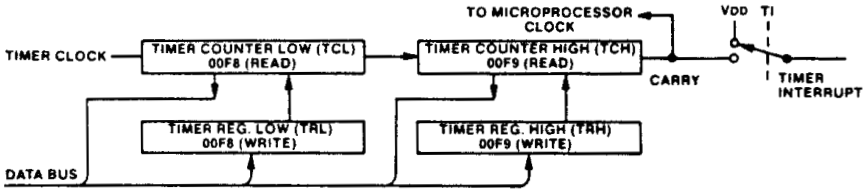


Figure 7. Timer Functional Block Diagram

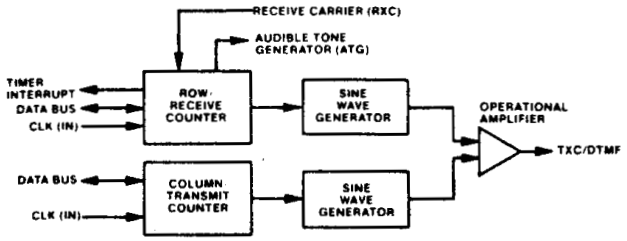


Figure 8. Frequency Detection/Generation Block Diagram

Timer Operation—The timer operating mode is enabled by setting the control register timer interrupt bit to one. The desired time interval is written in the 16-bit timer register (00F8,9). When the timer interrupt (TI) bit is set to one the timer carry interrupts the microprocessor; the counter decrements toward a zero value. When the counter generates a carry by counting past zero, the timer register is again transferred to the counter and interrupts the microprocessor if the interrupt bit in the status register is zero. A read operation will read the contents of the counter and reset the interrupt latch.

Low Power Operation—This mode is enabled by setting the control register $\phi 2$ mode bit to one. Since chip power consumption is directly related to operating frequency, power can be reduced by lowering the microprocessor clock frequency. The desired clock divide ratio is written in the 16-bit timer register at address 00F8 and 00F9. When the counter decrements from zero, the timer register is transferred to the counter. In this configuration, the counter carry output becomes the system $\phi 2$ clock (See Figure 5b).

Frequency Detection/Generation

The frequency detection/generation section of the G65SC150 contains the necessary circuitry to generate a wide range of sine waves, either singularly or in pairs. See Figure 8, Frequency Detection/Generation Block Diagram. In addition, a square wave may be generated as a separate frequency output. Furthermore, a frequency detection input (RXC) is provided for measurement or duplex communications. The row/receive counter and column/transmit counter operate independently or in conjunction with each other to perform the various communications modes as determined by bits CC0, CC1 and CC2 of the control register. The row/receive and column/transmit counters are programmable. Register values for typical applications are shown in Figure 16 (page 12).

Row/Receive Counter

The 16-bit Row/Receive Counter (RRC) and Row/Receive Register (RRR) (address 00F4, 5) operate as a tone generator, pulse width interval timer or interval timer as determined by CCX bits in the Control Register. Figure 9 illustrates the RRC/RRR functional block diagram for these three modes.

In the Idle Mode (CCX = 000), both the counter (RRC) and the register (RRR) are inactive, no interrupt is generated and there is no tone output. With the exception of the single tone column (CCX = 100), any change in CCX to any other state will cause the row/receive counter to be initialized with the current register value and the counter to begin counting.

In the Interval Timer Mode (CCX = 001), the row/receive counter serves as an additional interval timer. The counter interval is received from the row/receive register via the Data Bus. Upon generation of a carry, a timer interrupt is generated and the new contents of RRR is transferred to the counter (RRC). The counter continues counting and the process (cycle) continues until modified. In the interval timer mode, an interrupt is generated at intervals from 2.2349 microseconds to 73.234 milliseconds with a resolution of 1.1175 microseconds.

In the Pulse Width Timer Mode (CCX = 010), the row/receiver counter is used as a pulse width timer, measuring the period between Receive Carrier (RXC) transitions. In this case, both positive and negative transitions of the RXC input cause an interrupt and transfers the counter value to the row/receive register where it may be read by the microprocessor. Following each transfer, the counter continues counting. In telecommunications applications, receive carrier detect and dial tone detect functions can be accomplished.

In the Single Tone Row/Tone Generator mode (CCX = 011), a row/receive counter overflow reloads the counter from the row/receive register. No interrupt is generated. The overflow (carry signal) goes to either the ATG divide-by-two circuit, or to the sine wave generator and TXC/DTMF depending on the state of the ATG control register bit. With a clock frequency of 3.579545 MHz, a square wave with a frequency in the range of 13.7 Hz to 447 KHz may be generated at the Audible Tone Generator (ATG) output. For the same set of inputs, a sine wave with a frequency in the range of 1.05 Hz to 34.4 KHz appears at the TXC/DTMF output.

Column/Transmit Counter

The column/transmit counter circuit is enabled by the CC2 control register bit. A sine wave frequency in the range of 267.8 Hz to 34.4 KHz appears at the TXC/DTMF output. Figure 10 illustrates the column/transmit functional block diagram. For modem operation without the prescaler, the frequency range is 535.7 Hz to 68.8 KHz. A binary count is loaded into the register (CTR) at address location 00F6. The input is then transferred to the counter (CTC). As the counter continues to count, an overflow is generated which serves to reload the counter (CTC) from the contents of the register (CTR).

In the Single Tone Column Mode (CCX = 100), no interrupt is generated. In this mode, the overflow signal serves as one of the clock input signals to the sine wave generator. In this way, a single tone is generated at the TXC/DTMF output.

Combined Modes

In the Modem Mode (CCX = 101), both the pulse width timer mode of the row/receive counter and the single tone column mode are active. This allows simultaneous reception and transmission of data. In telecommunications applications such as duplex 300 bps modem, the row/receive circuitry demodulates the receive carrier at the RXC input while

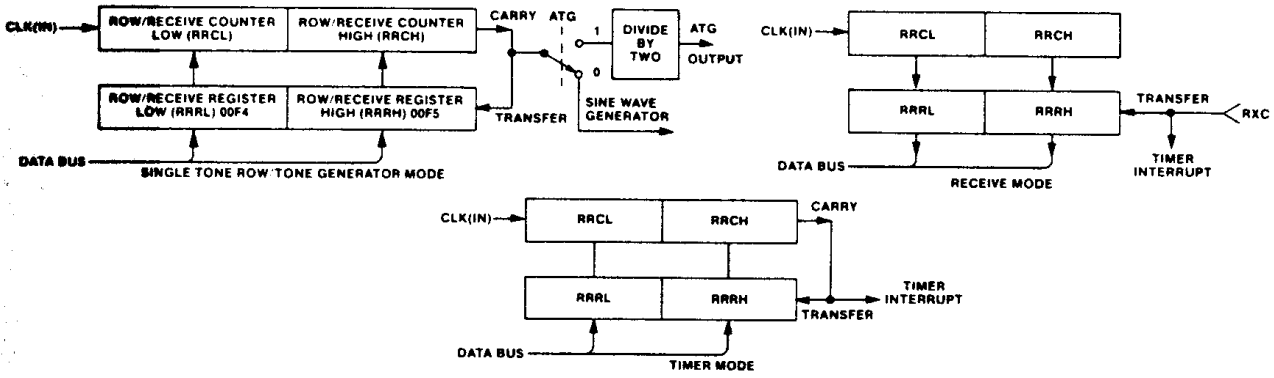


Figure 9. Row/Receive Functional Block Diagram

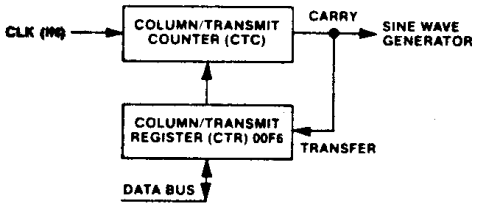


Figure 10. Column/Transmit Functional Block Diagram

the column/transmit circuitry generates the modulated transmit carrier at the TXC/DTMF output. Maximum clock frequency is applied to increase the precision of the transmit carrier frequencies.

In the Modem—Divide-by-Two Prescaler Mode (CCX = 110), operation is the same as the modem mode except that the divide-by-two prescaler is used. In this way, this mode allows low frequency transmit carrier generation.

In the Dual Tone Multifrequency Mode (CCX = 111), a combination of the single tone row mode and single tone column mode is used. In telecommunications applications, this arrangement allows standard DTMF signaling tones to be generated.

Sine Wave Generator

The modem and DTMF output signals are synthesized by the sine wave generator. An approximation of a sine wave is formed by a series of 26 voltage steps per cycle as shown in Figure 11. Figure 12 illustrates the sine wave generator functional block diagram. The two identical divide by 26 circuits are step counters that determine the fixed number of steps per cycle of the sine wave. The inputs to these counters are the outputs of the row/receive and column/transmit dividers that determine the variable step length, or frequency, of each sine wave.

A step select PLA translates the step number from the step counter to a number corresponding to the step voltage level. The D-to-A resistor networks convert these numbers to voltage levels to form the sine wave as shown in Figure 11. The column (high group) frequency amplitude is approximately 2.0 dB greater than the row frequency amplitude to compensate for the high frequency roll-off of the telephone circuit. The outputs of the two D-to-A converters are combined to drive the operational amplifier. V_{REG} is the power supply for the converters and amplifier to ensure a constant tone output level independent of V_{DD} variations. The amplifier output appears on the TXC/DTMF output depending on control register bits, CC0, CC1 and CC2.

To avoid transients when starting or stopping sine wave generation, the output remains at the voltage level defined by the step counters and D-to-A resistor networks when the step counters are stopped.

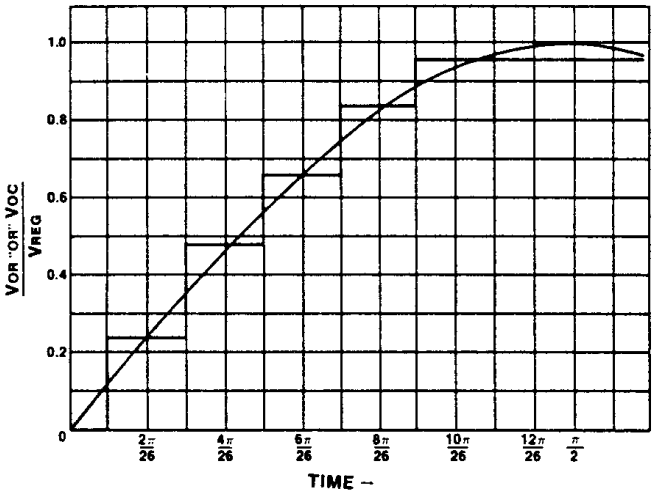


Figure 11. Sine Wave Generator Step Heights

General Formula for Determining Register Values

$$\text{Register Value} = \frac{OSC}{K \times F} - 2$$

$$\text{Register Value (Timer)} = \frac{OSC \times T}{K} - 2$$

OSC = Oscillator Frequency
F = Desired Frequency
T = Timer Period
K = Constant

		Desired Frequency (F) Limits
Modem	K = 26	Limit = 535.7 Hz to 68.8 KHz
DTMF and Modem with Prescaler	K = 52	Limit = 267.8 Hz to 34.4 KHz
ATG	K = 4	Limit = 13.7 Hz to 447 KHz
μP Clock	K = 4	Limit = 13.7 Hz to 447 KHz
Timer	K = 4	Limits = 2.2349 μS to 73.234 mS

F = 3.579545 MHz

Input/Output Registers

Figure 13 illustrates the I/O registers and their addresses. There are 27 I/O lines (PA0-PA7, PB0-PB7, PC0-PC7 and PD0-PD2) associated with four memory addressable registers (00F0-3).

Outputs are set by loading the desired bit pattern into the corresponding I/O register. A logic "1" selects a high output (or OFF), and a logic "0" selects a low output. A read operation always detects the logic state at the I/O pin, regardless of the previously loaded register value. When using the I/O pins as inputs, the I/O register should be loaded to provide the appropriate active level. When reset is active ($\overline{RES}$ = 0), all I/O registers and pins are initialized to a logic "1".

Figure 14 illustrates the circuitry associated with each I/O pin. Depending on the mask option chosen, the output can source either 0 μA, 10 μA, 200 μA, or 1.0mA at V_{OH} = 2.4 volts, or 3mA at 1.5 volts.

Address and Data Buffer

These buffers allow memory and I/O expansion of the microprocessor bus. Each buffer is TTL compatible. Control register bit TSC is set to one for normal operation (bus active). When TSC is set to zero, R/$\overline{W}$, and address lines AB0-AB15 and DB0-DB7 are pulled to ground by a high resistance device. In a typical application, TSC is set to zero when the external bus is not powered. Figure 15 illustrates a complete memory address map.

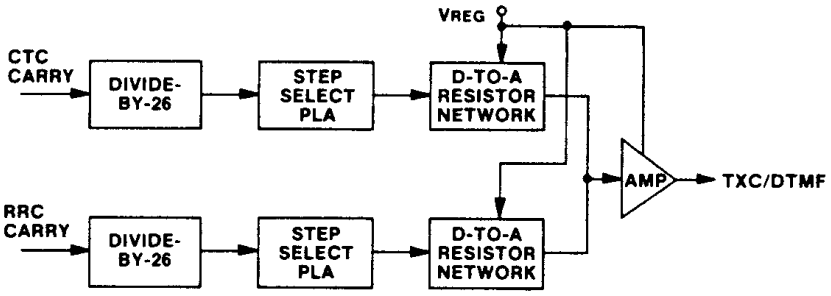


Figure 12. Sine Wave Generator Functional Block Diagram

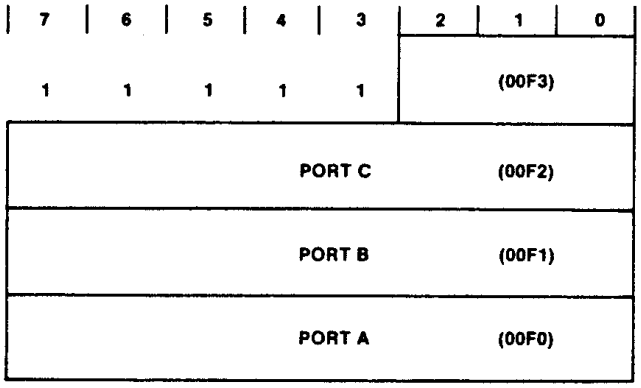


Figure 13. I/O Port Functional Block Diagram

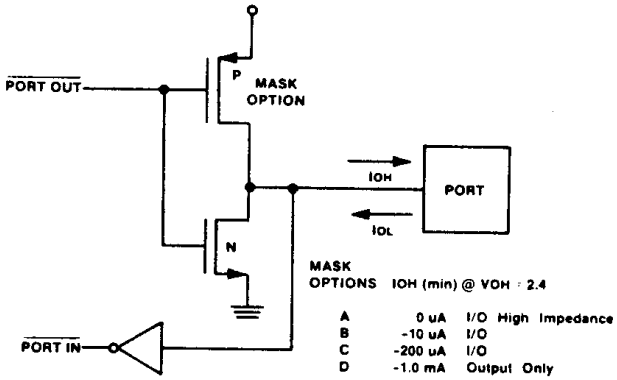


Figure 14. I/O Port Schematic

ADDRESS	DESCRIPTION		
FFFE, F	BREAK	INTERRUPT VECTORS	2048 BYTES ROM
FFFC, D	TIMER COUNTER		
FFFA, B	EXTERNAL		
FFF8, 9	ROW/RECEIVE COUNTER		
FFEE, F	RESET		
FFEC, D	NON-MASKABLE		
FFEB			
F800			
01FF			64 BYTES RAM
01C0			
00FF			TELECOM. REGS.
00F8, 9	TIMER		
00F7	CONTROL		
00F6	COLUMN/TRANSMIT		
00F4, 5	ROW/RECEIVE		
00F3	PD0-2 I/O		
00F2	PC0-7 I/O		
00F1	PB0-7 I/O		
00F0	PA0-7 I/O		
00EF	SEE RANDOM ACCESS MEMORY PARAGRAPH	(SAME AS 01C0 THRU 01EF, 48 BYTES)	
00C0			

Figure 15. Memory Map

Standard Frequency (Hz)	Oscillator 3.579545 MHz Register Value	Oscillator 3.579545 MHz Actual Frequency (Hz)	Oscillator 4.000000 MHz Register Value	Oscillator 4.000000 MHz Actual Frequency (Hz)
• DTMF Row				
697	98	695	109	699
770	88	773	99	769
852	80	850	89	855
941	72	943	81	938
• DTMF Column				
1209	56	1208	63	1202
1336	51	1324	57	1326
1477	46	1465	51	1479
1633	41	1639	46	1637
• Call Progress Tones				
350	196	349	219	350
440	155	441	174	440
480	142	481	159	481
620	110	620	123	620
• U.S. 110,300 Baud Modem				
1070	63	1076	71	1068
1270	53	1275	60	1261
2025	33	2025	37	2024
2225	30	2221	34	2198
• European 110,300 Baud Modem				
980	69	983	77	986
1180	57	1187	64	1183
1650	41	1639	46	1637
1850	36	1860	41	1832
• Teletext				
390	176	389	196	390
450	152	450	170	450
1300	52	1299	58	1304
2100	32	2086	36	2079
• U.S. 1200 Baud Modem				
390	176	389	196	390
450	152	450	170	450
1200	56	1208	63	1202
2200	30	2221	34	2198

Figure 16. Communications Frequency Generated by Row/Receive and Column/Transmit Counters

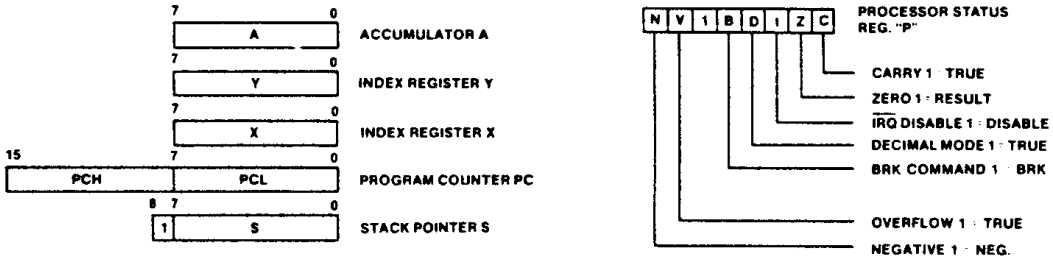


Figure 17. Microprocessor Programming Model

Maximum Frequency Mode (Phase 2, bit 3 is 0)			
Crystal Frequency		Microprocessor Clock	
8 MHz		2 MHz	
4 MHz		1 MHz	
3.579545 MHz		894.9 KHz*	
Lower Power Mode (Phase 2, bit 3 is 1)			
Crystal Frequency	Timer Count	Microprocessor Clock	Timer Interrupt Interval (max. freq. mode)
8 MHz	1	1.0 MHz	1 μS
	19	100 KHz	10 μS
	199	10 KHz	100 μS
	1999	1 KHz	1 mS
	19999	100 Hz	10 mS
	65535	30.5 Hz*	131.072 mS
4 MHz	1	500 KHz	2 μS
	9	100 KHz	10 μS
	99	10 KHz	100 μS
	999	1 KHz	1 mS
	9999	100 Hz	10 mS
	65535	15.3 Hz*	65.536 mS
3.579545 MHz	1	447.4 KHz*	2.2 μS*
	8	99.4 KHz*	10.1 μS*
	88	10.1 KHz*	99.5 μS*
	894	999.8 Hz*	1.0 mS*
	8948	100.0 Hz*	10.0 mS*
	65535	13.7 Hz*	73.2 mS*

*Approximate value

Figure 18. Microprocessor Clock Frequency and Timer Interval

MNE-MONIC	OPERATION	IMMEDIATE OP	n	#	ABSOLUTE OP	n	#	ZERO PAGE OP	n	#	(4) IMPLIED OP	n	#	(IND. X) OP	n	#	(1) (IND), Y OP	n	#	ZPG,X OP	n	#	(1) ABS,X OP	n	#	(1) ABS,Y OP	n	#	RELATIVE (2) OP	n	#	INDIRECT OP	n	#	ZPG,Y OP	n	#	PROCESSOR STATUS CODE 7 6 4 3 2 1 0 N V B D I Z C	MNE-MONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← [7 0] ←0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3													N • • • • Z C	ASL
BCC	BRANCH IF C=0																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3													M₇ M₆ • • Z •	BIT
BMI	BRANCH IF N=1																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3													N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A ∀ M →A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3													N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0→ [7 0] → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3													0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A→Ms S-1→S										48	3	1																									• • • • • • •	PHA
PHP	P→Ms S-1→S										08	3	1																									• • • • • • •	PHP
PHX	X→Ms S-1→S										DA	3	1																									• • • • • • •	PHX
PHY	Y→Ms S-1→S										5A	3	1																									• • • • • • •	PHY
PLA	S+1→S Ms→A										68	4	1																									N • • • • Z •	PLA
PLP	S+1→S Ms→P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1→S Ms→X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1→S Ms→Y										7A	4	1																									N • • • • Z •	PLY
ROL	← [7 0] ←C				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3													N • • • • Z C	ROL
ROR	→C→ [7 0]				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3													N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-C̄→A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STX	X → M				8E	4	3	86	3	2																													• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2															96	4	2	• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	ĀAM → M (6)				1C	6	3	14	5	2																													• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																													• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA

Notes:

1. Add 1 to "n" if page boundary is crossed, except STA and STZ.
2. Add 1 to "n" if branch occurs to same page. Add 2 to "n" if branch occurs to different page.
3. Add 1 to "n" if decimal mode.
4. Accumulator address is included in Implied address.
5. "N" and "V" flags are unchanged in immediate mode.
6. "Z" flag indicates A∧M result (same as BIT instruction).

X Index X
Y Index Y
A Accumulator
M Memory per effective address
Ms Memory per stack pointer

\+ Add
\- Subtract
∧ And
V Or
∀ Exclusive or

n No. Cycles
No. Bytes
M₆ Memory Bit #6
M₇ Memory Bit #7

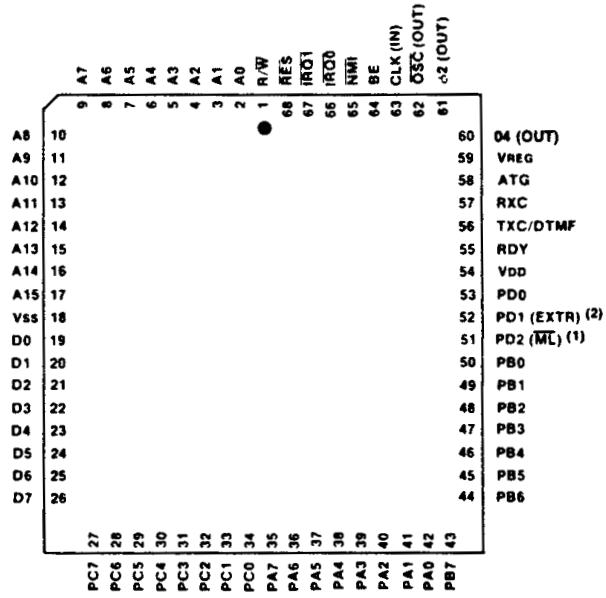
Figure 19. Operational Codes, Execution Times, and Memory Requirements

Pin Function Table

PIN	DESCRIPTION	PIN	DESCRIPTION
A0-Axx	Address Bus	PA0-PA7	Port A
ATG	Audible Tone Generator	PB0-PB7	Port B
BE	Bus Enable	PC0-PC7	Port C
D0-D7	Data Bus	PD0-PD2	Port D
TXC/DTMF	Transmit Carrier/Dual Tone Multifrequency	RDY	Ready
$\overline{IRQ}$	Interrupt Request	$\overline{RES}$	Reset
$\overline{ML}$	Memory Lock	RXC	Receive Carrier
EXTR	External ROM	R/$\overline{W}$	Read/Write
$\overline{NMI}$	Non-Maskable Interrupt		
CLK(IN)	Clock Input		
$\overline{OSC}$(OUT)	Oscillator Output	VDD	Positive Power Supply (+5.0 volts)
ϕ2(OUT)	Phase 2 Out	VREG	Regulated Supply Voltage
ϕ4(OUT)	Phase 4 Out	VSS	Internal Logic Ground

Pin Configuration

68-Pin Leaded Plastic and Ceramic Chip Carrier
(Top-side View)



NOTES:
1. METAL MASK OPTION
2. EXTR SELECTED ONLY IN TEST AND PROTOTYPE MODE

G65SC150 Mask Options

The following mask options are available for the G65SC150, and must be specified before an order can be placed. To ensure that the proper options are selected, always contact the nearest CMD Microcircuits Sales Office prior to placing an order.

1. Oscillator feedback resistor
   - Feedback resistor between CLK(IN) and OSC(OUT)
   - No feedback resistor

2. The following signals are available with or without pull-up resistors:
   BE, $\overline{NMI}$, $\overline{IRQ0}$, RDY, $\overline{IRQ1}$, $\overline{RES}$

3. Pin 51 is available with the following signal option:
   PD2 or $\overline{ML}$

4. Three optional I/O source currents are available for the following signals. These source currents include: 0μA, 10μA, 200μA @ 2.4V, and 1mA @ 2.4V or 3mA @ 1.5V.
   PA0-PA7
   PB0-PB7
   PC0-PC7
   PD0-PD2
   ATG

Ordering Information

G 65SC150 PE I -2

Description
C—Special G—Standard

Product Identification Number

Package
P—Plastic E—Leaded Chip Carrier
C—Ceramic L—Leadless Chip Carrier
D—Cerdip X—Dice

Temperature/Processing
W— -40° C to +85° C, ± 10% P.S. Tol.

Performance Designator
Designators selected for speed and power specifications.
—1 1 MHz —2 2 MHz

Consult factory for lower V_{DD} operating specifications.