*Multi*GEN™ GF9330
High Performance SDTV/HDTV Deinterlacer

PRELIMINARY DATA SHEET

GF9330

FEATURES

- De-interlace, Pass-Through and Film Frame Rate Down Conversion modes of operation
- support for multiple input data formats with multiplexed and separate Y/C channels
- support for multiple output data formats
- programmable noise reduction and detail enhancement
- ability to extract HVF information from embedded TRS
- support for both 8-bit and 10-bit video signals
- flexibility to handle generic input data formats that have less than 2046 active samples per line
- 12-bit output resolution
- selectable rounding and clipping of output data (7 modes)
- internal clock doubler
- selectable blanking of active video lines for Y and C channels
- HVF output signals with programmable output video cropping
- 3:2 pull-down sequence reporting
- user configuration through a dedicated host interface, supporting parallel and serial interfaces
- seamless interface to Gennum's GF9331
- seamless interface to Gennum's GS1500/GS1510/GS9020
- seamless interface to Gennum's GS1501/GS1511/ GS9021
- seamless interface to popular NTSC/PAL decoders
- 3.3V supply for device I/O and 2.5V for core logic
- 5V tolerant inputs
- IEEE 1149.1 compliant JTAG test port

DEVICE OVERVIEW

The GF9330 is a high performance VDSP engine that performs high quality de-interlacing of interlaced digital television signals. The GF9330 supports both standard definition (SDTV) and high definition (HDTV) signal formats and clock rates.

The GF9330 includes nine directional adaptive filters, an adaptive vertical motion filter and an adaptive inter-field motion filter. The GF9330 includes a robust 3:2 pull-down detection circuit in addition to detail enhancement and noise reduction capabilities. The GF9330 also supports static/freeze-frame detection and compensation. The GF9330 may operate as a stand-alone de-interlacer or may be used with the GF9331 Motion Co-processor. The GF9331 contains adaptive edge detectors that cover nine different directions and a vertical motion detector. Edge and motion sensitive control signals are fed back directly to the GF9330. These control signals adaptively switch the GF9330's internal de-interlacing filters on a pixel by pixel basis.

The GF9330 integrates all required line delays and seamlessly interfaces to off chip SDRAMs that form the required field delays. The GF9330 can be used to perform film rate down conversions (60Hz → 24Hz). The GF9330 may also operate in by-pass mode should no processing of the input signal be desired.

APPLICATIONS

- HDTV Upconverters/Downconverters
- Projection Systems
- Plasma Displays/LCD Displays
- Video Walls
- Home Theater Systems
- HD DVD Players

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP RANGE
GF9330-CBP	328 PIN BGA	0°C to 70°C

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Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
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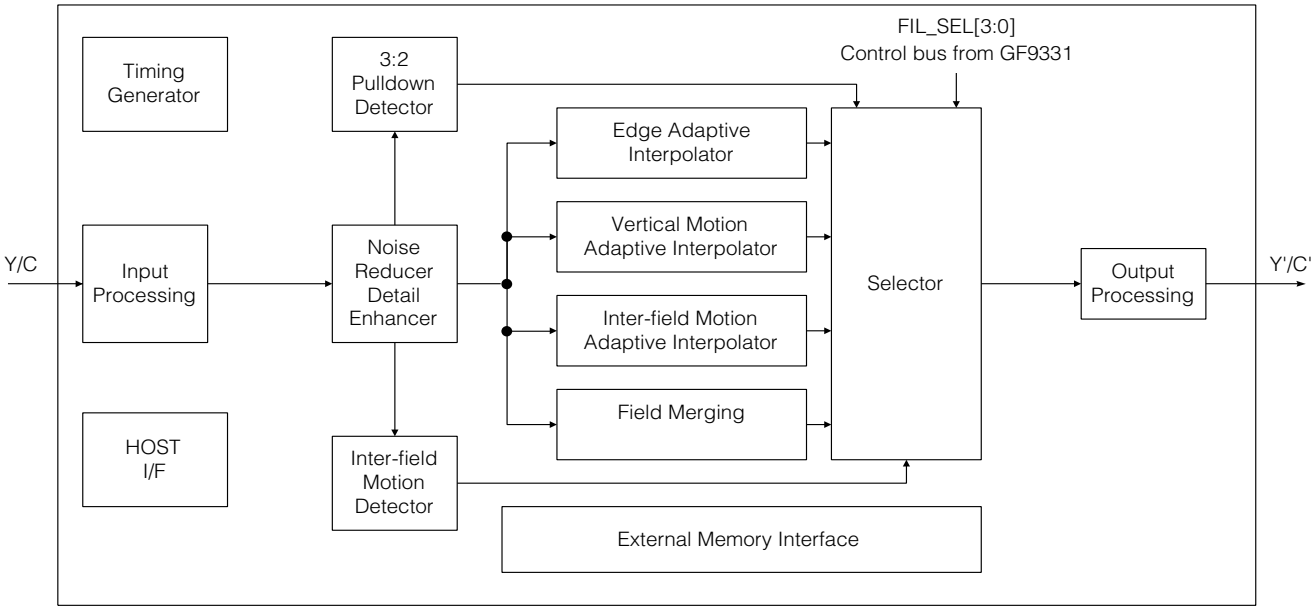


BLOCK DIAGRAM

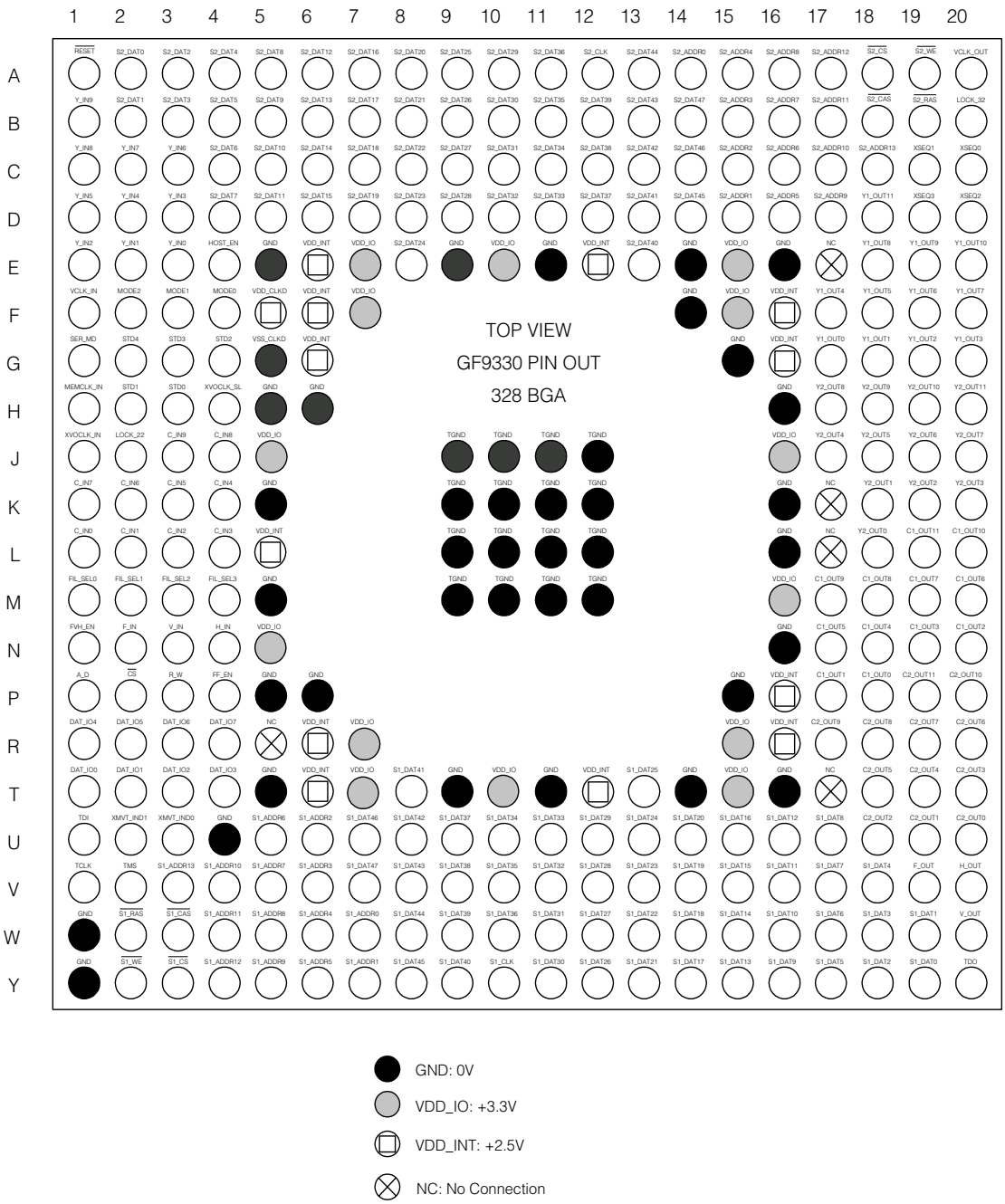


Fig.1 Top View Pin Out 328 BGA

PIN DESCRIPTIONS

SYMBOL	PIN GRID	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	A1	I	Active low, asynchronous $\overline{\text{RESET}}$, resets all internal state machines to their default conditions.
VCLK_IN	F1	I	Input clock. When the input is SDTV the input clock will be 27, 36, 54 or 72MHz. When the input format is HDTV, the input clock will be 74.25 or 74.25/1.001MHz.
MEMCLK_IN	H1	I	Input clock for SDRAM operation to support HD modes, 90MHz input (supplied by an off-chip crystal oscillator).
XVOCLK_IN	J1	I	Input clock. This input may be used instead of the internal VCLK_IN clock doubler to supply the video output clock VCLK_OUT.
XVOCLK_SL	H4	I	Control signal input. When high, selects XVOCLK_IN; when low, selects the internal VCLK_IN clock doubler for generation of the video output VCLK_OUT signal.
Y_IN[9:0]	B1,C1,C2,C3,D1, D2,D3,E1,E2,E3	I	8/10-bit input data bus for separate luminance or multiplexed luminance and colour difference video data. When supplying 8-bit data to the GF9330, Y_IN[1:0] will be set low and the 8-bit data supplied to Y_IN[9:2].
C_IN[9:0]	J3,J4,K1,K2,K3, K4,L4,L3,L2,L1	I	8/10-bit input data for colour difference for video data. When supplying 8-bit data to the GF9330, C_IN[1:0] will be set low and the 8-bit data supplied to C_IN[9:2].
FIL_SEL[3:0]	M4,M3,M2,M1	I	Filter Selection control bus. FIL_SEL[3:0] are used to switch the GF9330's internal directional filters on a pixel by pixel basis. FIL_SEL[3:0] is supplied by the GF9331.
F_IN	N2	I	Video timing control. F_IN identifies the ODD and EVEN fields in the incoming video signal. F_IN will be low in Field 1 and high in Field 2.
V_IN	N3	I	Video timing control. V_IN represents the vertical blanking signal associated with the incoming video signal. V_IN is high during the vertical blanking interval and low during active video.
H_IN	N4	I	Video timing control. H_IN represents the horizontal blanking signal associated with the incoming video signal. H_IN is high during horizontal blanking and low during active video.
FVH_EN	N1	I	Control signal input. When high, the F_IN, V_IN, and H_IN input pins will be used for video data signalling. When low, embedded TRS's will be detected for video data signaling.
FF_EN	P4	I	Control signal input. When high, FF_EN enables the GF9330's internal freeze frame compensation.
XMVT_IND[1:0]	U2,U3	I	Control signal input. Provides optional external control for motion compensation.
LOCK_22	J2	I	Control signal input. For 2:2 pull-down compensation, the LOCK_22 pin will be used to identify the presence of a 2:2 sequence in the input video stream.
STD[4:0]	G2,G3,G4,H2,H3	I	Video format definition. Defines the video standard when operating without the host interface. See table 1.
MODE[2:0]	F2,F3,F4	I	Operation mode selection. Defines the mode of operation when operating without the host interface. See section 8.
HOST_EN	E4	I	Host interface enable. When set high, the GF9330 is then configured through the host interface. When set low, the GF9330 is manually configured via input pins,

PIN DESCRIPTIONS (continued)

SYMBOL	PIN GRID	TYPE	DESCRIPTION
SER_MD	G1	I	Host interface mode selection. Enables serial mode operation when high. Enables parallel mode operation when low.
$\overline{CS}$	P2	I	Functions as an active low chip select input for host interface parallel mode operation. Functions as a serial clock input for host interface serial mode operation.
DAT_IO[7:0]	R4,R3,R2,R1,T4,T3, T2,T1	I/O	Host interface bi-directional data bus for parallel mode. In serial mode, DATA[7] serves as the serial data output pin and DATA[0] serves as the serial data input pin.
R_W	P3	I	Host interface Read/Write control for parallel mode. A read cycle is defined when high, a write cycle is defined when low.
A_D	P1	I	Host interface Address/Data control for parallel mode. The DATA bus contains an address when high, a data word when low. In serial mode, this pin serves as the chip select (active low).
VCLK_OUT	A20	O	Video output clock. Ouput frquency based on selected output standard. See section 9.
Y1_OUT[11:0]	D18,E20,E19,E18, F20,F19,F18,F17, G20,G19,G18,G17	O	Output data bus for separate luminance or multiplexed luminance and colour difference video data. See section 9.
Y2_OUT[11:0]	H20,H19,H18,H17, J20,J19,J18,J17,K20, K19,K18,L18	O	Output data bus for luminance video data during dual pixel mode operation. See section 9.
C1_OUT[11:0]	L19,L20,M17,M18, M19,M20,N17,N18, N19,N20,P17,P18	O	Output data bus for colour difference video data. See section 9.
C2_OUT[11:0]	P19,P20,R17,R18, R19,R20,T18,T19, T20,U18,U19,U20	O	Output data bus for colour difference video data during dual pixel mode operation. See section 9.
LOCK_32	B20	O	Control signal output. When the GF9330's internal algorithm detects a 3:2 sequence in the video stream, the LOCK_32 signal is set high. Otherwise, LOCK_32 is low.
XSEQ[3:0]	D19,D20,C19,C20	I/O	Control signal input/output. For external 3:2 sequence detection, the XSEQ[3:0] pins will be used to provide the 3:2 sequence information. For internal 3:2 detection, the XSEQ[3:0] pins output the detected 3:2 sequence information.
H_OUT	V20	O	Output control signal. H_OUT is a horizontal blanking output.
F_OUT	V19	O	Output control signal. F_OUT is an ODD/EVEN field indicator.
V_OUT	W20	O	Output control signal. V_OUT is a vertical blanking output.
S1_CLK	Y10	O	SDRAM bank 1 clock.
$\overline{S1\_CS}$	Y3	O	Active low SDRAM chip select for Field Buffer 1.
$\overline{S1\_RAS}$	W2	O	Active low SDRAM row address strobe for Field Buffer 1.
$\overline{S1\_CAS}$	W3	O	Active low SDRAM column address strobe for Field Buffer 1.
$\overline{S1\_WE}$	Y2	O	Active low SDRAM write enable for Field Buffer 1.
S1_ADDR[13:0]	V3,Y4,W4,V4,Y5,W5, V5,U5,Y6,W6,V6, U6,Y7,W7	O	SDRAM address for Field Buffer 1.

PIN DESCRIPTIONS (continued)

SYMBOL	PIN GRID	TYPE	DESCRIPTION
S1_DAT[47:0]	V7,U7,Y8,W8,V8, U8,T8,Y9,W9,V9, U9,W10,V10,U10, U11,V11,W11,Y11, U12,V12,W12,Y12, T13,U13,V13,W13, Y13,U14,V14,W14, Y14,U15,V15,W15, Y15,U16,V16,W16, Y16,U17,V17,W17, Y17,V18,W18,Y18, W19,Y19	I/O	SDRAM data for Field Buffer 1.
S2_CLK	A12	O	SDRAM bank 2 clock.
$\overline{\text{S2\_CS}}$	A18	O	Active low SDRAM chip select for Field Buffer 2.
$\overline{\text{S2\_RAS}}$	B19	O	Active low SDRAM row address strobe for Field Buffer 2.
$\overline{\text{S2\_CAS}}$	B18	O	Active low SDRAM column address strobe for Field Buffer 2.
$\overline{\text{S2\_WE}}$	A19	O	Active low SDRAM write enable for Field Buffer 2.
S2_ADDR[13:0]	C18,A17,B17,C17, D17,A16,B16,C16, D16,A15,B15,C15, D15,A14	O	SDRAM address for Field Buffer 2.
S2_DAT[47:0]	B14,C14,D14,A13, B13,C13,D13,E13, B12,C12,D12,A11, B11,C11,D11,D10, C10,B10,A10,D9, C9,B9,A9,E8,D8,C8, B8,A8,D7,C7,B7, A7,D6,C6,B6,A6, D5,C5,B5,A5,D4, C4,B4,A4,B3,A3, B2,A2	I/O	SDRAM data for Field Buffer 2.
TDI	U1	I	JTAG data input.
TMS	V2	I	JTAG mode select.

PIN DESCRIPTIONS (continued)

SYMBOL	PIN GRID	TYPE	DESCRIPTION
TCLK	V1	I	JTAG test clock.
TDO	Y20	O	JTAG data output.
VDD_CLKD	F5	NA	2.5 V supply for the internal clock doubler.
VSS_CLKD	G5	NA	Ground connection for the internal clock doubler.
VDD_IO	E7,E10,E15,F7,F15, J5,J16,M16,N5,R7, R15,T7,T10,T15	NA	3.3 V supply.
VDD_INT	E6,E12,F5,F6,F16, G6,G16,L5,P16,R6, R16,T6,T12	NA	2.5 V supply.
GND / TGND	E5,E9,E11,E14,E16, F14,G15,H5,H6, H16,K5,K16,L16, M5,N16,P5,P6,P15, T5,T9,T11,T14,T16, J9,J10,J11,J12, K9,K10,K11,K12, L9,L10,L11,L12, M9,M10,M11,M12, U4,W1,Y1	NA	Device ground / Thermal ground (electrically equivalent).
NC	E17,K17,L17,R5,T17		No Connection.

ELECTRICAL CHARACTERISTICS

5V Tolerant Inputs

Input cells used in the design are able to withstand a 5 V CMOS input signal without degrading performance or long-term reliability. The GF9330 supports TTL compatible inputs as well as 3/5V CMOS inputs.

ESD Tolerance

GF9330 has 2 kV ESD protection. ESD testing is done in accordance with Gennum's standard ESD testing procedure.

3.3V Supply for Device I/0 and 2.5V for Core Logic

The GF9330 operates from a single +3.3V supply for device I/O. The GF9330 operates off a single +2.5V supply for core logic.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	SYMBOL	VALUE
Device I/O Supply Voltage	V_{DDIO}	-0.5 to tbd V
Device Core Supply Voltage	V_{DDCORE}	-0.5 to tbd V
Input Voltage Range (any input)	V_{IN}	$-0.5 < V_{IN} < +4.6V$
Operating Temperature Range	T_A	$0°C < T_A < 70°C$
Storage Temperature Range	T_S	$-40°C < T_S < 125°C$
Lead Temperature (soldering 10 seconds)		260°C

DC ELECTRICAL CHARACTERISTICS

V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Device I/O Supply Voltage		V_{DDIO}	+3.0	+3.3	+3.6	V	1
Device Core Supply Voltage		V_{DDCORE}	+2.25	+2.5	+2.75	V	1
Device I/O Supply Current	V_{DDIO}=3.6V	I_{DDIO}			tbd	mA	1
Device Core Supply Current	V_{DDCORE}=2.75V	I_{DDCORE}			tbd	mA	1
Input Leakage Current	I_{IN}=0V or I_{IN}=V_{DD}	I_{LEAK}			10	µA	1
Input Logic LOW Voltage		V_{IL}	--	--	0.8	V	1
Input Logic HIGH Voltage		V_{IH}	2.1	--	--	V	1
Output Logic LOW Voltage	I_{OL}= 4mA	V_{OL}	--	0.2	0.4	V	1
Output Logic HIGH Voltage	I_{OH}= -4mA	V_{OH}	2.7	--	--	V	1

NOTES:
1. Production, test and QA are performed at room temperature.

AC ELECTRICAL CHARACTERISTICS - Video Interfaces

The Video Interface signals include
VCLK, Y_IN, C_IN, FIL_SEL[3:0], F_IN, V_IN, H_IN, FVH_EN, FF_EN MVT_IND[1:0], LOCK_22, Y1_OUT[11:0], Y2_OUT[11:0], C1_OUT[11:0], C2_OUT[11:0], LOCK_32 SEQ[3:0], H_OUT, F_OUT and V_OUT.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI}	--	74.25	83	MHz	1, 2
Input Data Setup Time		t_{SU}	2.5	--	--	ns	1, 3
Input Data Hold Time		t_{IH}	1.5	--	--	ns	1, 3
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD}	--	--	10.0	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN}	--	--	10	ns	1
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS}	--	--	10	ns	1
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF}	--	--	2.0	ns	1, 4

NOTES:
1. Based on simulation results, verified during device characterization process.
2. Also supports 74.25/1.001MHz.
3. 50% levels.
4. 20% to 80% levels.

AC ELECTRICAL CHARACTERISTICS - SDRAM Interfaces

The SDRAM 1 Interface signals include S1_CLK, $\overline{S1\_CS}$, $\overline{S1\_RAS}$, $\overline{S1\_CAS}$, $\overline{S1\_WE}$, S1_ADDR[13:0] and S1_DATA[47:0].
The SDRAM 2 Interface signals include S2_CLK, $\overline{S2\_CS}$, $\overline{S2\_RAS}$, $\overline{S2\_CAS}$, $\overline{S2\_WE}$, S2_ADDR[13:0] and S2_DATA[47:0]. SDRAM Interfaces
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI_SD}	--	85	90	MHz	1
Input Data Setup Time		t_{SU_SD}	2.0	--	--	ns	1, 2
Input Data Hold Time		t_{IH_SD}	2.5	--	--	ns	1, 2
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_SD}	--	--	9.1	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_SD}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_SD}	--	--	20	ns	1, 4
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_SD}	--	--	20	ns	1, 4
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_SD}	--	--	2.0	ns	1, 3

NOTES:
1. Based on simulation results, verified during device characterization process.
2. 50% levels.
3. 20% to 80% levels.
4. Two clock cycles allocated for data bus turnaround.

AC ELECTRICAL CHARACTERISTICS - Host Interface

The host interface signals include HOST_EN, SER_MD, $\overline{CS}$, DAT_IO[7:0], R_W and A_D.
V_{DDIO} = 3.0 to 3.6V, V_{DDCORE} = 2.25 to 2.75V, T_A = 0°C to 70°C, unless otherwise shown

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Input Frequency		F_{HSCI_HI}	--	--	20	MHz	1
Input Data Setup Time		t_{SU_HI}	5	--	--	ns	1, 2
Input Data Hold Time		t_{IH_HI}	1.5	--	--	ns	1, 2
Input Clock Duty Cycle			40	--	60	%	1
Output Data Delay Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OD_HI}	--	--	10.0	ns	1
Output Data Hold Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OH_HI}	2.0	--	--	ns	1
Output Enable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{OEN_HI}	--	--	15	ns	1
Output Disable Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODIS_HI}	--	--	15	ns	1
Output Data Rise/Fall Time	V_{DDIO}=3.6V, C_L=15pF load	t_{ODRF_HI}	--	--	2.0	ns	1, 3

NOTES:
1. Based on simulation results, verified during device characterization process.
2. 50% levels.
3. 20% to 80% levels.

DETAILED DEVICE DESCRIPTION

1. SUPPORTED INPUT VIDEO FORMATS

The GF9330 supports multiple input data formats with multiplexed or separate Y/C channels. Data is supplied to the GF9330 through the Y_IN[9:0] and the C_IN[9:0] busses. Table 1 outlines the data formats that are supported according to the setting of the control register bits STD[4:0]

TABLE 1: Encoding of STD[4:0] for Selecting Input Data Format

STD	STD[4:0]	DESCRIPTION
0	00000	525i (30/1.001) component SMPTE 125M. Multiplexed Y Cb Cr data applied to Y_IN. C_IN is set low. Note: Input clock is 27MHz.
1	00001	RESERVED.
2	00010	525i (30/1.001) component 16x9 SMPTE 267M. Multiplexed Y Cb Cr data applied to Y_IN. C_IN is set low. Note: Input clock is 36MHz.
3	00011	RESERVED
4	00100	625i (25Hz) component EBU tech. 3267E. Multiplexed Y Cb Cr data applied to Y_IN. C_IN is set low. Note: Input clock is 27MHz.
5	00101	RESERVED
6	00110	625i (25Hz) component 16x9 ITU-R BT.601-5 Part B. Multiplexed Y Cb Cr data applied to Y_IN. C_IN is set low. Note: Input clock is 36MHz.
7	00111	RESERVED
8	01000	525p (60/1.001Hz) SMPTE 293M. Y Cb Cr data stream applied to Y_IN. C_IN is set low. Note: Input clock is 54MHz.
9	01001	RESERVED
10	01010	RESERVED
11	01011	RESERVED
12	01100	625p (50Hz) ITU-R BT.1358. Y Cb Cr data stream applied to Y_IN. C_IN is set low. Note: Input clock is 54MHz.
13	01101	625p (50Hz) 16 x 9 with 18MHz sampling. Y Cb Cr data stream applied to Y_IN. C_IN is set low. Note: Input clock is 72MHz.
14	01110	Generic SD input data format with 4:1:1 sampling. Y Cb Cr data is applied to both Y_IN and C_IN. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. Note: Input clock is 27MHz.
15	01111	Generic SD input data format with 4:2:2 sampling and single multiplexed Y Cb Cr input format. Y Cb Cr data applied to Y_IN. C_IN is set low. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. Note: Input clock is 27 or 36MHz.
16	10000	720p (60 & 60/1.001Hz) SMPTE 296M January 1999 Draft (System #1 and #2). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25 MHz or 74.25/1.001MHz.
17	10001	720p (30 & 30/1.001Hz) SMPTE 296M January 1999 Draft (System #4 and #5). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
18	10010	1080p (30 & 30/1.001Hz) SMPTE 274M (System #7 and #8). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
19	10011	720p (50Hz) SMPTE 296M January 1999 Draft (System #3). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.

TABLE 1: Encoding of STD[4:0] for Selecting Input Data Format (continued)

STD	STD[4:0]	DESCRIPTION
20	10100	1080p (25Hz) SMPTE 274M (System #9). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
21	10101	720p (25Hz) SMPTE 296M January 1999 Draft (System #6). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
22	10110	1080p (24 & 24/1.001Hz) SMPTE 274M (System # 10 and #11). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25 MHz or 74.25/1.001 MHz.
23	10111	720p (24 & 24/1.001Hz) SMPTE 296M January 1999 Draft (System #7 and #8). Y Data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001 MHz.
24	11000	1080i (30 & 30/1.001Hz) SMPTE 274M (System #4 and #5). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
25	11001	1080p (30 & 30/1.001Hz in Segmented Frame Format) SMPTE Draft RP May 99 (System #12 and #13). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
26	11010	1080i (25Hz) SMPTE 274 (System # 6). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
27	11011	1080p (25 Hz in Segmented Frame Format) SMPTE Draft RP May 99 (System #14). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
28	11100	1080i (25Hz) SMPTE 295M (System #2). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
29	11101	1080p (24 & 24/1.001Hz in Segmented Frame Format) Draft RP May 99 (System #15 & #16). Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz or 74.25/1.001MHz.
30	11110	1035i (30Hz) SMPTE 260M. Y data applied to Y_IN. Cb Cr data applied to C_IN. Note: Input clock is 74.25MHz.
31	11111	Generic HD input data format with 4:2:2 sampling and a separate Y/C format. Y Data applied to Y_IN. Cb Cr data applied to C_IN. Externally supplied F_IN, V_IN and H_IN signals are used to synchronize the input data stream. Note: Input clock is 74.25MHz or 74.25/1.001MHz.

2. INPUT SYNCHRONIZATION

The GF9330 obtains relevant timing information from either embedded TRS information or externally supplied H_IN, V_IN, and F_IN signals.

When both the FVH_EN pin and the FVH_EN bit within the host interface are high, the GF9330 relies on the externally supplied H_IN, V_IN and F_IN signals for timing information. When both the FVH_EN pin and the FVH_EN bit within in the host interface are low, the GF9330 will extract the embedded TRS timing information from the video data stream and will ignore any timing information present on the F_IN, V_IN, and H_IN pins.

2.1 Support for both 8-bit and 10-bit input data

The GF9330 supports 8 and 10-bit input data. When operating with 8-bit input data, the two LSBs of the GF9330's 10-bit input should be set low and the input data is applied to the 8 MSBs of the input bus.

2.2 Generic Input Format Signaling

The GF9330 supports generic input data formats with either 4:1:1 or 4:2:2 sampling structures handling up to 2046 active samples per line with a total maximum line width of 4096 (active + blanking) samples. In addition, there is a limit of 2048 lines per interlaced frame. The following host interface parameters are used to describe the generic input data format relative to the F_IN, V_IN and H_IN signals.

2.2.1 OUTPUT H_BLANK_SIZE

This parameter defines the number of samples that comprise the horizontal blanking region. This parameter has a maximum value of 4095 and is to be less than the total line width (active + blanking) sample size. Twelve bits within the host interface are dedicated to this parameter. The GF9330 stores and processes active video samples only (i.e. H_IN=0).

2.2.2 V_BLANK_SIZE_ODD

This parameter defines the number of lines that comprise the vertical blanking interval that follows the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9330 stores and processes active video samples only (i.e. V_IN=0). See Figure 2.

2.2.3 V_BLANK_SIZE_EVEN

This parameter defines the number of lines that comprise the vertical blanking interval that follows the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. The GF9330 stores and processes active video samples only (i.e. V_IN=0). See Figure 2.

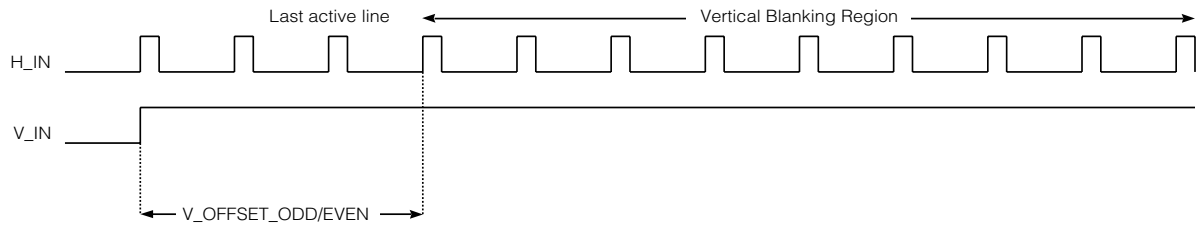


Fig. 2 Vertical Offset Definition

2.2.4 V_OFFSET_ODD

This parameter defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the V_IN signal.

2.2.5 V_OFFSET_EVEN

This parameter defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter 1 has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the V_IN signal.

2.2.6 F_OFFSET_ODD

This parameter defines the number of lines from the F_IN pin EAV transition to the desired position within the vertical blanking interval following the odd field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the F_IN signal.

2.2.7 F_OFFSET_EVEN

This parameter defines the number of lines from the F_IN pin EAV transition to the desired position within the vertical blanking interval following the even field. This parameter has a maximum value of 255. Eight bits within the host interface are dedicated to this parameter. This parameter has been added to accommodate all video decoders which output non-standard timing for the F_IN signal.

2.2.8 H_POLARITY

This parameter defines the polarity of the H_IN pin. With H_POLARITY set low, a high-to-low transition on the H_IN pin indicates end of active video. With H_POLARITY set high, a low-to-high transition on the H_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter.

2.2.9 F_POLARITY

This parameter defines the polarity of the F_IN pin. Refer to Table 2 for F_POLARITY encoding. One bit within the host interface is dedicated to this parameter.

TABLE 2: F_POLARITY

F_POLARITY	F PIN	F PIN FUNCTION
0	0	Even field
0	1	Odd Field
1	0	Odd Field
1	1	Even Field

2.2.10 V_POLARITY

This parameter defines the polarity of the V_IN pin. With V_POLARITY set low, a high-to-low transition on the V_IN pin indicates the end of active video. With V_POLARITY set high, a low-to-high transition on the V_IN pin indicates the end of active video. One bit within the host interface is dedicated to this parameter.

3. SEAMLESS INTERFACE TO THE GF9331 MOTION CO-PROCESSOR FOR DIRECTIONAL FILTER CONTROL

The GF9330 can operate as a stand-alone de-interlacer or can operate in conjunction with the GF9331 Motion Co-processor. The GF9331 contains adaptive edge detectors that cover nine different directions and a vertical motion detector. Edge sensitive control signals are fed back directly to the GF9330.

These control signals adaptively switch the GF9330's internal de-interlacing filters on a pixel by pixel basis. These control signals are fed to the GF9330 by the GF9331 over the FIL_SEL[3:0] control bus. When the GF9330 is not being used with the GF9331, the FIL_SEL[3:0] inputs should be set low.

NOTE: When using the GF9331, the Y_IN[9:0] of the GF9330 must be connect to the Y_OUT[9:0] of the GF9331 and the C_IN[9:0] of the GF9330 must be connected to the C_OUT[9:0] of the GF9331. FIL_SEL[3:0] of the GF9330 must also be connected to FIL_SEL[3:0] of the GF9331.

4. SEAMLESS INTERFACE TO EXTERNAL SDRAMS

For all SD video formats, the GF9330 requires two independent external field buffers, each implemented with a 1 Meg (min) x 24-bit SDRAM configuration. This configuration supports all SD operational modes.

For all HD video formats, the GF9330 requires two independent external field buffers, each implemented with a 1 Meg (min) x 48-bit SDRAM configuration. This configuration supports all HD and SD operational modes. The following external SDRAM devices are supported for the external field buffer function.

- NEC: uPD4516161AG5, uPD4564163G5, uPD45128163G5
- Micron: MT48LC4M16A2, MT48LC8M16A2
- Samsung: K4S161622C, K4S641632C, K4S281632B

5. HOST INTERFACE

The GF9330 provides both a serial and parallel host interface control port for the configuration of internal parameters. The GF9330 is also be able to operate in stand-alone mode, with no host interface control. In stand-alone mode, the video standard STD[4:0] and mode of operation MODE[2:0] are set using dedicated pins on the device. Both the serial and parallel interfaces share common pins as described in Table 4.

TABLE 4: Host Interface Common Pins

GF9330 PIN NAME	PARALLEL MODE	SERIAL MODE
$\overline{CS}$	CHIP select	SCLK - Serial Clock
DAT_IO0	Data/address (bit 0)	SDI - Serial data in
DAT_IO1	Data/address (bit 1)	(not used)
DAT_IO2	Data/address (bit 2)	(not used)
DAT_IO3	Data/address (bit 3)	(not used)
DAT_IO4	Data/address (bit 4)	(not used)
DAT_IO5	Data/address (bit 5)	(not used)
DAT_IO6	Data/address (bit 6)	(not used)
DAT_IO7	Data/address (bit 7)	SDO - Serial data out
A_D	Address/data select	$\overline{SCS}$ - Serial chip select
R_W	Read/write select	(not used)
HOST_EN	Host interface enable	Host interface enable
SER_MD	low = parallel mode enable	high = Serial mode enable

5.1 Host Interface Serial Mode

The Gennum Serial Peripheral Interface (GSPI) is a 4 wire interface comprised of serial data in (SDI), serial data out (SDO), an active low serial chip select ($\overline{SCS}$) and a clock (SCLK). The interface operates in a master/slave configuration, where the master provides the SCLK, SDI, and $\overline{SCS}$ signals to the slave or slaves. The master uC_SDO drives the slave(s) SDI input. The SDO pin is a tristate output to allow multiple devices to drive the master uC_SDI. Serial mode operation supports both a continuous clock and a burst clock configuration. The serial mode interface is illustrated in the Figure 3.

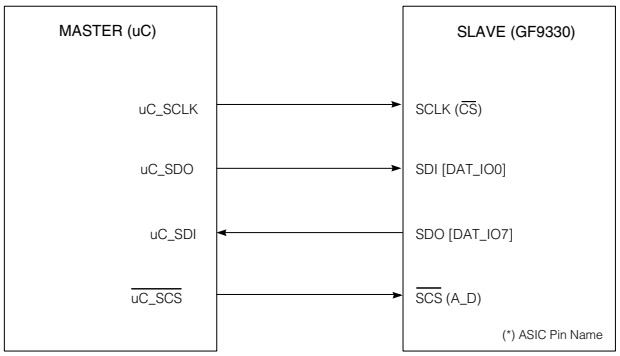


Fig. 3 Host Interface Serial Mode

5.1.1 SERIAL COMMAND WORD DESCRIPTION

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Update control bit, nine reserved bits and a 5-bit address. As shown in Figure 4.

Fig. 4 Serial Command Word Bit Representation

The R/W bit indicates a Read command if R/W = high, and a write command when R/W = low.

The auto-update feature will be executed when the Auto-Update control bit is set. All configuration registers will be set to their appropriate settings corresponding on the previously stored video standard and operational mode. This simplifies configuration while allowing customization of many features and format parameters.

The 5-bit address is used to identify all configuration registers within the GF9330.

5.1.2 SERIAL DATA WORD DESCRIPTION

Serial data word consists of a 16-bit word as shown in Figure 5. Serial data is transmitted or received MSB first.

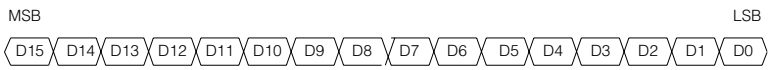


Fig. 5 Serial Data Word Bit Representation

Both command and data words are clocked into the GF9330 on the rising edge of the serial clock (SCLK) which may operate in either a continuous or burst fashion. The first bit (MSB) of the serial output (SDO) is available following the last falling SCLK edge of the "read" command word. The remaining bits are clocked out on the negative edges of SCLK.

5.1.3 WRITE OPERATION

All write cycles consist of a command word followed by a data word, both transmitted to the GF9330 via SDI. The first 16-bit word transmitted following a high-to-low transition of $\overline{SCS}$ is a command word. Several write cycles may be performed while $\overline{SCS}$ is low. See Figure 6.

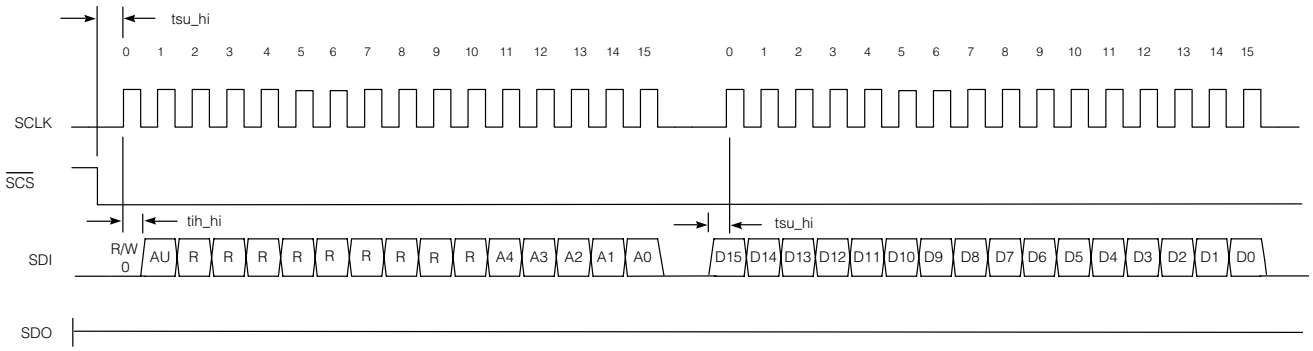


Fig. 6 Write Cycle

5.1.4 READ OPERATION

All read cycles consist of a command word transmitted to the GF9330 via SDI followed by a data word transmitted from the GF9330 via SDO. The first 16-bit word transmitted following a high-to-low transition of $\overline{SCS}$ is a command word. Several read cycles may be performed while $\overline{SCS}$ is low. See Figure 7.

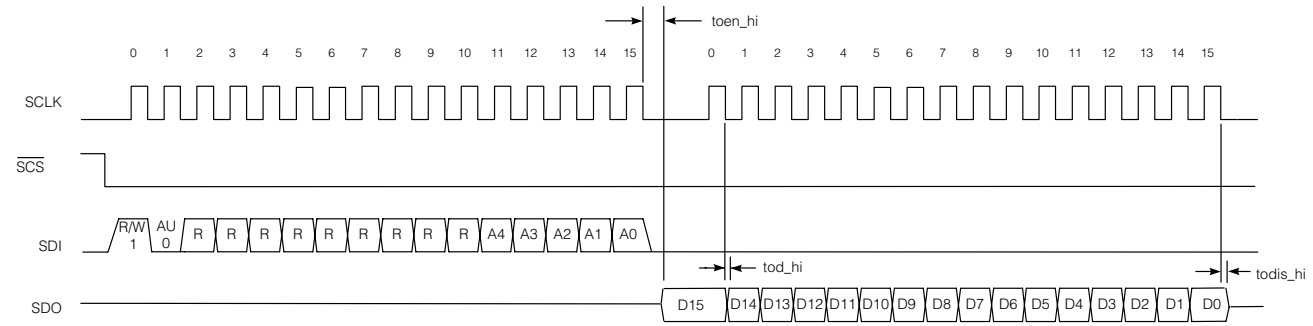


Fig. 7 Read Cycle

5.2 Host Interface Parallel Mode

The Gennum Parallel Peripheral Interface (GPPI) consists of an 8-bit multiplexed address/data bus (DAT_IO[7:0]), a chip select pin ($\overline{CS}$), a read/write pin (R_W), and an address/data pin (A_D) as shown in Figure 8.

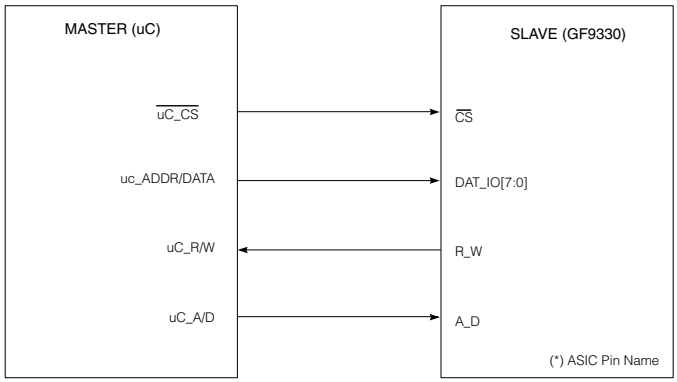


Fig. 8 Parallel Peripheral Interface

Data is strobed in/out of the parallel interface on the falling edge of $\overline{CS}$. The GF9330 drives the DAT_IO[7:0] bus when the R_W pin is HIGH and the $\overline{CS}$ pin is LOW, otherwise this port is in a high impedance state.

A write cycle to the parallel interface is shown below. First an 8-bit address word is provided to the DAT_IO port by asserting the R_W pin to LOW and A_D pin to HIGH. The MSB of the address word contains an auto-update flag, which allows automatic configuration of predefined registers. The 5 LSB's of the address word contain the address location for the read or write operation. The remaining address bits DAT_IO[6:5] are reserved. The address word is registered on the falling edge of $\overline{CS}$. Following this, the A_D pin is driven LOW and two DATA words are sent upper byte (UB) word first and are each clocked in on the falling edge of $\overline{CS}$. Two 8-bit data words must follow each address word to occupy each 16-bit parameter which are defined in Table 5.

A read cycle begins with an ADDRESS write by asserting the R_W pin low and A_D HIGH. The address is clocked on the falling edge of $\overline{CS}$. Following the address, the R_W pin must be driven HIGH and A_D driven LOW to allow the upper byte of data to be clocked out on the first falling edge of $\overline{CS}$ followed by the lower byte on the second negative edge of $\overline{CS}$. See Figure 9.

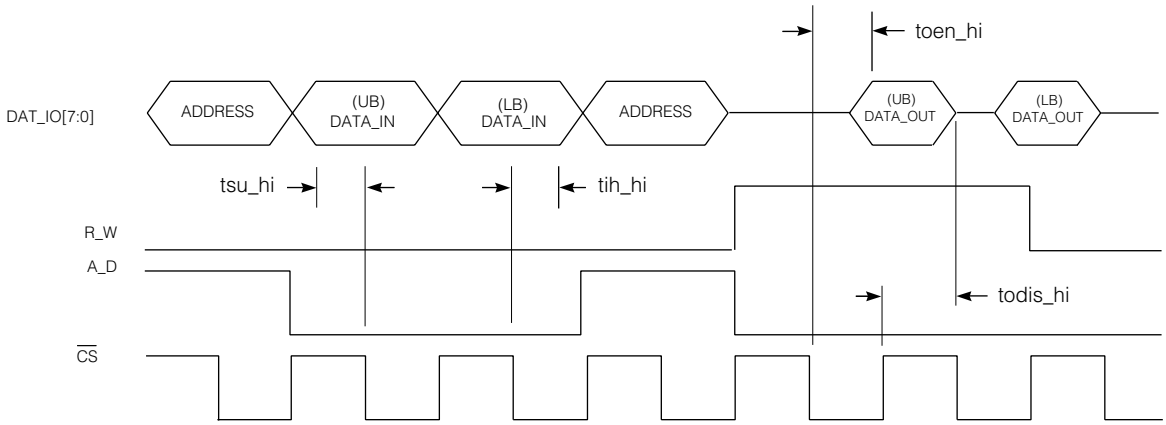


Fig. 9 Write Cycle to the Parallel Interface

TABLE 5: Host Interface Register Allocation

	Hex	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 31	1F	CMD_RESET															START_OPERATION
Address 30	1E														CLK_X1_SEL	VCCLK_X1_SEL	EXT_MEMCLK_SEL
Address 29	1D	ADD_LINES_TOP_F2						V_FIELD2_LASTLINE(11:0)									
Address 28	1C	ADD_LINES_BOTTOM_F1						V_BLANK2_LASTLINE(11:0)									
Address 27	1B	ADD_LINES_BOTTOM_F2						V_FIELD1_LASTLINE(11:0)									
Address 26	1A	F_VBI1_OFFSET(3:0)						V_BLANK1_LASTLINE(11:0)									
Address 25	19	F_VBI2_OFFSET(3:0)						OUTPUT_H_BLANK_SIZE(11:0)									
Address 24	18							OUTPUT_H_LINE_SIZE(12:0)									
Address 23	17	CM_MODE(2:0)			FRAME_REGEN	FDC_MODE(1:0)		NO_LINE_DELAYS(9:0)									
Address 22	16	ODD_FIELD_ONE_MORE	EVEN_FIELD_ONE_MORE	FIELD2_HAS_TOP_LINE	H_BLANK_SIZE_1/HALF	INPUT_H_BLANK_WORDS_PER_LINE(11:0)											
Address 21	15	ID_MODE(1:0)		PROGRESSIVE_INPUT	FORMAT_SD	ACTIVE_PIXEL_LINE(10:0)											
Address 20	14	V_BLANK_OFFSET				ACTIVE_LINE_FIELD(10:0)											
Address 19	13	V_BLANK_SIZE_ODD(7:0)								V_BLANK_SIZE_EVEN(7:0)							
Address 18	12														DIFF3T(18:16)		
Address 17	11									DIFF3T(15:0)							
Address 16	10														MSF(18:16)		
Address 15	F									MSF(15:0)							
Address 14	E														M32(18:16)		
Address 13	D									M32(15:0)							
Address 12	C											CROP_V_CROP_SIZE(11:0)					
Address 11	B											CROP_V_FRAME_SIZE(11:0)					
Address 10	A											CROP_H_CROP_SIZE(11:0)					
Address 9	9				CROP_SMOOTH_EDGE							CROP_H_LINE_SIZE(11:0)					
Address 8	8	DETAIL_ENH(9:0)											MSF_COEFF(2:0)			DIFF3T_COEFF(2:0)	
Address 7	7	TV32(7:0)												FREEZE_FRAME_THRESHOLD			
Address 6	6	CC_BLANK_START_LINE(7:0)												CC_BLANK_END_LINE(7:0)			
Address 5	5	TVSF(7:0)												THSF(7:0)			
Address 4	4	MD_THRESHOLD			SOBEL_THRESHOLD(9:0)									NOISE_RED(7:0)			
Address 3	3	V_OFFSET_ODD(7:0)								V_OFFSET_EVEN(7:0)							
Address 2	2	F_OFFSET_ODD(7:0)								F_OFFSET_EVEN(7:0)							
Address 1	1	H_POLARITY	V_POLARITY	F_POLARITY	FVH_EN_BIT	CROP_EN		CL_RND(2:0)		CC_BLANK_EN	MODE_32	MD_MODE(1:0)			FF_EN_BIT	FF_MODE(1:0)	
Address 0	0			LOCK_32	FF_DETECT	SEQUENCE(3:0)				MODE(2:0)		STD(4:0)					

5.3 Control Register Definition

The host interface internal registers are divided into three classes: User Configurable (UC), Auto-Configurable (AC), and Read-Only (RO). Address locations 0 through 14 contain parameters which may be configured by the user. Locations 15 through 31 are automatically configured based on the STD[4:0] and [2:0] registers, but can be user configured if desired. Address 0 contains three status registers LOCK_32, FF_DETECT, and SEQUENCE[3:0] which can only be read. Writing to the read-only registers will have no effect on their contents.

STD[4:0] Address [0][4:0], UC, Default Value = 00000, Defines the video standard as described in section 1.

MODE[2:0] Address [0][7:5], UC, Default Value = 000, Defines the GF9330 operating mode as show below:

- 000: Interlaced to Progressive Mode
- 001: Field Merging Mode
- 010: Film Rate Down Conversion Mode
- 011: Film Rate Down Conversion (Progressive Segmented Frame) Mode
- 111: Bypass Mode (Video Pass Through Mode)

SEQUENCE[3:0] Address [0][11:8], RO, Default Value = Calculated, Provides the detected field sequence number from the 3:2 detection circuit.

FF_DETECT Address [0][12], RO, Default Value = Calculated, Set high if a video freeze frame has been detected.

LOCK_32 Address [0][13], RO, Default Value = Calculated, Set high if a 3:2 video sequence has been detected.

FF_MODE[1:0] Address[1][1:0], UC, Default Value = 01, Defines the freeze frame operating mode as shown below:

- 00: Manual freeze frame detection/compensation
- 01: Automatic freeze frame detection/compensation
- 10: Disabled
- 11: Reserved

FF_EN_BIT Address[1][2], UC, Default Value = 1, Enables (high) or disables (low) freeze frame detection/ compensation when in manual freeze frame mode, i.e. FF_MODE = 00.

MD_MODE[1:0] Address[1][5:4], UC, Default Value = 01, Defines the motion detection and compensation mode as shown below:

- 00: Manual motion detection/compensation through MD_MODE pins.
- 01: Automatic motion detection/compensation
- 10: Disabled
- 11: reserved

MODE_32 Address[1][6], UC, Default Value = 0, Selects the internal 3:2 sequence detection when set to low, otherwise uses external sequence from the input pins, XSEQ[3:0].

CC_BLANK_EN Address[1][7], UC, Default Value = 0, Enables blanking in the close captioned video region.

CL_RND[2:0] Address[1][10:8], UC, Default Value = 000, Defines the Clipping and Rounding output format as shown below:

- 000: 12-bit output with 10.2 (.25 lsb) resolution
- 001: 10-bit output clipped/rounded from 0 to 1023
- 010: 10-bit output clipped/rounded from 4-1019
- 011: 10-bit output Y clipped/rounded from 64 to 940, Cr/Cb clipped/rounded from 64 to 960
- 100: Reserved
- 101: 8-bit output clipped/rounded from 0 to 255
- 110: 8-bit output rounded/clipped from 1 to 254
- 111: 8-bit output Y clipped/rounded from 16 to 235, Cr/Cb clipped/rounded from 16 to 240

CROP_EN Address[1][11], UC, Default Value = 0, Enables output video cropping based on CROP_V_CROP_SIZE, CROP_V_FRAME_SIZE, CROP_H_CROP_SIZE, and CROP_H_LINE_SIZE parameters.

FVH_EN_BIT Address[1][12], UC, Default Value = 0, Enables the GF9330 to use external FVH control in place of embedded TRS.

F_POLARITY Address[1][13], UC, Default Value = 1, Defines the polarity of the F_IN pin. When set to '1', F follows normal convention where F_IN is '0' for field 1(odd) and '1' for field 2 (even).

V_POLARITY Address[1][14], UC, Default Val = 1, Defines the polarity of the V_IN pin. When set to '1', V_IN follows normal convention where V_IN is high in the vertical blanking region.

H_POLARITY Address[1][15], UC, Default Value = 1, Defines the polarity of the H_IN pin. When set to '1', H_IN follows normal convention where H is high in the horizontal blanking region.

F_OFFSET_EVEN[7:0] Address[2][7:0], UC, Default Value = 00000000, Defines the number of lines from the F_IN pin EAV transition to the desired position within the vertical blanking interval following the even field. This parameter has a maximum value of 255.

F_OFFSET_ODD[7:0] Address[2][15:8], UC, Default Value = 00000000, Defines the number of lines from the F_IN pin EAV transition to the desired position within the vertical blanking interval following the odd field. This parameter has a maximum value of 255.

V_OFFSET_EVEN[7:0] Address[3][7:0], UC, Default Value = 00000000, Defines the number of lines from the V_IN pin EAV transition to the end of the even active video field region. This parameter has a maximum value of 255.

V_OFFSET_ODD[7:0] Address[3][15:8], UC, Default Value = 00000000, Defines the number of lines from the V_IN pin EAV transition to the end of the odd active video field region. This parameter has a maximum value of 255.

NOISE_RED[7:0] Address[4][7:0], UC, Default Value = 00000001, The upper five bits of this parameter adjusts the noise reduction level applied to the video image, the resolution of the adjustment is defined by the lower 3-bits. A higher value represents more noise reduction with greater resolution.

SOBEL_THRESHOLD[3:0] Address[4][11:8], UC, Default Value = 0100, Edge detection threshold used for the SOBEL filter output within the Freeze Frame and 3:2 Detect functions.

MD_THRESHOLD[3:0] Address[4][15:12], UC, Default Value = 0100, Defines the motion detection threshold, a low value causes noise to have a larger impact on motion detection.

THSF[7:0] Address[5][7:0], UC, Default Value = 00110010 (50 decimal), Defines the horizontal edge detection threshold for same frame detection. A higher value will lower the number of pixels detected as a horizontal edge.

TVSF[7:0] Address[5][15:8], UC, Default Value = 00011110 (30 decimal), Defines the vertical edge detection threshold for same frame detection. A higher value will lower the number of pixels detected as a vertical edge.

CC_BLANK_END_LINE[7:0] Address[6][7:0], UC, Default Value = 0000000, Defines the last line number at which to end closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.

CC_BLANK_START_LINE[7:0] Address[6][15:8], UC, Default Value = 00000000, Defines the first line number at which to start closed captioned blanking. For this parameter, line 0 is defined as the first active line of the field/frame.

FREEZE_FRAME_THRESHOLD[4:0] Address[7][4:0], UC, Default Value = 10000 (16 decimal), Defines the Freeze frame detection threshold, a low value causes noise to have a larger impact on freeze frame detection.

TV32[7:0] Address[7][15:9], UC, Default Value = 00101000 (40 decimal), Defines the threshold for the detection of vertical motion between two consecutive fields. A higher value will increase the sensitivity.

DIFF3T_COEFF[2:0] Address[8][2:0], UC, Default Value = 100, Defines the scaling coefficient for the DIFF3T calculation. See DIFF3T.

MSF_COEFF[2:0] Address[8][5:3], UC, Default Value = 100, Defines the scaling coefficient for the MSF calculation. See MSF.

DETAIL_ENH[9:0] Address[8][15:6], UC, Default Value = 0000000001, Defines the detail enhancement configuration. The upper five bits of this word adjust the high frequency detail in the image. The lower 5-bits control the resolution or granularity, a higher value represents more detail with higher granularity.

CROP_H_LINE_SIZE[11:0] Address[9][11:0], UC, Default Value = 000000000000, Specifies the length of the line to output, following the cropped pixels on the left side of the line.

CROP_SMOOTH_EDGE Address[9][12], UC, Default Value = 0 Indicates no smoothing when set to '0', and 3 pixel smoothing when set to '1'.

CROP_H_CROP_SIZE[11:0] Address[10][11:0], UC, Default Value = 000000000000, Specifies the number of active pixels to blank at the beginning of each line.

CROP_V_FRAME_SIZE[11:0] Address[11][11:0], UC, Default Value = 000000000000, Specifies the number of lines to output, following the cropped lines at the top of the frame (or field).

CROP_V_CROP_SIZE[11:0] Address[12][11:0], UC, Default Value = 000000000000, Specifies the number of active lines to blank at the beginning of each frame.

M32[18:0] Address[14][2:0] & Address[13][15:0], UC, Default Value = 00080H (128 decimal), Represents the number of pixels per smallest active field required to estimate the 3:2 pull down detection.

MSF[18:0] Address[16][2:0] & Address[15][15:0], UC, Default Value = Calculated, Represents the number of pixels per smallest active field divided by a scaling factor required to estimate same frame detection. A higher value also means vertical edges will have more effect on the detection of same frames. The equation is as follows:

MSF = #active_pixels_per_smallest_field / 2^(MSF_COEFF + 3)

DIFF3T[18:0] Address[18][2:0]& Address[17][15:0], UC, Default Value = Calculated, Represents the number of active pixels per smallest field divided by a factor required to estimate the odd and even pattern detection. The equation is as follows:

DIFF3T = #active_pixels_per_smallest_field 2^(DIFF3T_COEFF + 3)

V_BLANK_SIZE_EVEN[7:0] Address[19][7:0], AC, Default Value = Auto, Defines the number of lines that comprise the vertical blanking interval that follows the even input field. This parameter has a maximum value of 255.

V_BLANK_SIZE_ODD[7:0] Address[19][15:8], AC, Default Value = Auto, Defines the number of lines that comprise the vertical blanking interval that follows the odd input field. This parameter has a maximum value of 255.

ACTIVE_LINE_FIELD[10:0] Address[20][10:0], AC, Default Value = Auto, Defines the number of active lines in per smallest input field.

V_BLANK_OFFSET[3:0] Address[20][15:12], AC, Default Value = Auto, For 3:2 pull-down compensation, this parameter must provide the difference (if any) in number of input active lines per frame and the number of output active lines per frame.

ACTIVE_PIXEL_LINE[10:0] Address[21][10:0], AC, Default Value = Auto, Defines the number of active pixels per video input line.

FORMAT_SD Address[21][12], AC, Default Value = Auto Used to configure the GF9330 SDRAM controller. Set high when in 24-bit mode. This bit is auto-configured based on standard and mode selection.

PROGRESSIVE_INPUT Address[21][13], AC, Default Value = Auto, When high configures the GF9330 to accept a progressive video format. This bit is auto-configured based on standard and mode selection.

ID_MODE[1:0] Address[21][15:14], UC, Default Value = Auto, Defines the type of video sequence for input video de-multiplexing. When set to "00" the input represents a 4:2:2 sequence, "01" represents a 4:1:1 sequence, and "10" represents an HD format. This word can be auto-configured based on video standard and mode.

INPUT_H_BLANK_WORDS_PER_LINE[11:0] - Address[22][11:0], AC, Default Value = Auto, Defines the number of horizontal blanked input words per line which corresponds to 2 times the number of blanking pixels per line for 4:2:2 SD modes and is equal to the number of pixels per line for HD formats. This value can be auto-configured.

H_BLANK_SIZE_1HALF Address[22][12], AC, Default Value = Auto, Reserved for output video formats requiring the equivalent of ½ pixel line size resolution. This occurs for STD 0, MODE 2 and 3 only.

FIELD2_HAS_TOP_LINE Address[22][13], AC, Default Value = Auto, Set high when field 2 line one is the first line in the video frame (SMPTE 260M).

EVEN_FIELD_ONE_MORE Address[22][14], AC, Default Value = Auto, Set high for video standards that have an even number of lines per frame (SMPTE 295M).

ODD_FIELD_ONE_MORE Address[22][15], AC, Default Value = Auto, Set high for video standards that have an even number of lines per frame (SMPTE 295M).

NO_LINE_DELAYS[9:0] Address[23][9:0], AC, Default Value = Auto, Defines the number of line delays to implement within the external a field delay. This value is auto-configured based on standard and mode. The calculation is:

No_line_delays = (Total number of lines per frame -7) / 2.

FDC_MODE[1:0] Address[23][11:10], AC, Default Value = Auto, Defines the Field Delay Controller Mode for output video formatting as shown below:

- 00: I to P mode
- 01: PsF to P
- 10: 30i to 24p
- 11: 30i to 24PsF

FRAME_REGEN Address[23][12], AC, Default Value = Auto, Defines frame timing regeneration. This occurs for all 30i-24p and 30i-24PsF modes.

OM_MODE[2:0] Address[23][15:13], AC, Default Value = Auto, Defines the GF9330 video output mode as shown below:

- 000: SD bypass
- 001: SD I to P or field merging
- 010: SD I to P
- 011: SD I to PsF
- 100: HD bypass
- 101: HD I to P or field merging
- 110: HD I to P
- 111: HD I to PsF

This value can be auto-configured based on standard and mode.

OUTPUT_H_LINE_SIZE[11:0] Address[24][12:0], AC, Default Value= Auto, Represents the total number of pixels (Active plus blanking) per output line.

OUTPUT_H_BLANK_SIZE[11:0] Address[25][11:0], AC, Default Value = Auto, Defines the number of blanking pixels per line at the output.

F_VBI2_OFFSET[3:0] Address[25][15:12], AC, Default Value = Auto, Defines the number of lines to wait before the 0-1 F transition in the vertical blanking interval on the output.

V_BLANK1_LASTLINE[11:0] Address[26][11:0], UC, Default Value = Auto, Defines the last line of the first blanking interval, where line 1 is the first blank line of the vertical blanking interval that precedes the odd field or first frame.

F_VBI1_OFFSET[3:0] Address[26][15:12], AC, Default Value = Auto, Defines the number of lines to wait before the 1-0 F transition in the vertical blanking interval on the output.

V_FIELD1_LASTLINE[11:0] Address [27] [11:0], UC, Default Value = Auto, Defines the last line of the first active video field

ADD_LINES_BOTTOM_F2 Address[27][14:12], UC, Default Value = Auto, Defines the number of lines to add to the bottom of field 2 (not used).

V_BLANK2_LASTLINE[11:0] Address[28][11:0], UC, Default Value = Auto, Defines the last line of the second blanking interval

ADD_LINES_BOTTOM_F1 Address[28][14:12], UC, Default Value = Auto, Defines the number of lines to add to the bottom of field 1 (not used).

V_FIELD2_LASTLINE[11:0] Address[29][11:0], UC, Default Value = Auto, Defines the last line of the second active video field

ADD_LINES_TOP_F2 Address[29][14:12], AC, Default Value = Auto, Defines the number of lines to add to the top of field 2 (not used).

EXT_MEMCLK_SEL Address[30][0], AC, Default Value = Auto, Controls the selection of the SDRAM clock source. For VCLK_IN frequency less than 36 MHz, the internal clock doubler can be used, in all other modes an external source is required (MEMCLK_IN).

VOCLK_X1_SEL Address[30][1], AC, Default Value = Auto, Normally set for HD modes where the output video clock is equal to the input video clock frequency and is set to '0' for SD cases where the output video clock is double the video input clock frequency.

CLK_X1_SE Address[30][2], AC, Default Value = Auto, Normally set for all HD modes and is '0' for all other cases.

START_OPERATION Address[31][0], UC, Default Value = 0, using external F_IN, V_IN and H_IN signals, this parameter must be set following the completion of programming the F_IN, V_IN and H_IN offsets.

CMD_RESET Address[31][15], UC, Default Value = 0, Forces the GF9330 to enter a reset state. This commanded reset remains in effect until this parameter is cleared with a subsequent command.

6. CLOSED CAPTION BLANKING

The GF9330 provides a blanking function for selected input video lines. Consecutive lines within each input field are blanked, when this function is enabled, beginning with the CC_BLANK_START_LINE and ending with the CC_BLANK_END_LINE. The blanking is applied prior to any processing of the video data.

The blanking function is enabled with the CC_BLANK_EN bit. BLANK_START_LINE and BLANK_END_LINE are each allocated 8-bits within the host interface.

7. PROGRAMMABLE NOISE REDUCTION AND DETAIL ENHANCEMENT

The GF9330 performs an efficient technique for high frequency noise reduction and detail enhancement. There are 256 levels of control provided by the NOISE_RED[7:0] bits within the host interface.

High frequency details that are detected with a two-dimensional high pass filter are enhanced using a non-linear function mapping between input and output signal. The are 512 levels of control provided by the DETAIL_EN[8:0] bits within the host interface.

8. MODES OF OPERATION

The GF9330 supports stand-alone, motion adaptive, pass-through, and film rate down conversion modes of operation. Table 6 shows the basic operating modes for the GF9330 as selected using the MODE[2:0] control bits. host interface control of operation is provided through the MODE[2:0] register.

TABLE 6: Modes of Operation: MODE[2:0]

MODE[2:0]	DESCRIPTION
000	De-interlacing of input video signal.
001	Enhanced De-interlacing of input video signal (with pull-down compensation).
010	Film Rate Down Conversion Mode (60Hz -> 24Hz).
011	Film Rate Down Conversion Mode (60Hz -> 24Hz Segmented Frame)
100 to 110	Reserved
111	Video Pass Through Mode.

8.1 De-Interlacing Mode (MODE=000)

When set to operate as a de-interlacer the GF9330 can operate either as a “stand-alone” device performing standard VT processing of the input signal or as an adaptive de-interlacer. In order to function as an adaptive de-interlacer the GF9330 must be connected to the GF9331 as prescribed in section 3.

Segmented frame to progressive frame conversion is also supported in this mode. This function is performed when the progressive segmented frame input video format is selected on either the external pins or host interface register STD[4:0].

8.2 Enhanced De-interlacing Mode (MODE=001)

When set to operate as an enhanced de-interlacer the GF9330 can operate either as a “stand-alone” device performing standard VT processing of the input signal or as an adaptive de-interlacer. In order to function as an adaptive de-interlacer the GF9330 must be connected to the GF9331 as prescribed in the section 3.

In addition, the GF9330 will provide 3:2 sequence compensation (field merging) for film source material. When using internal 3:2 sequence detection, the GF9330 will perform "field-merging" for 3:2 sequences, or will revert to VT processing when no 3:2 sequence is identified. The 3:2 sequence can be internally detected (host interface bit, MODE_32 = low), or supplied via the external sequence pins (XSEQ[3:0]) for MODE_32 = high. With external Sequence selected, the device will revert back to VT processing if the external sequence pins have an invalid code (i.e. A to F). The XSEQ[3:0] value should be changed during the sixth blank line of each vertical blanking interval.

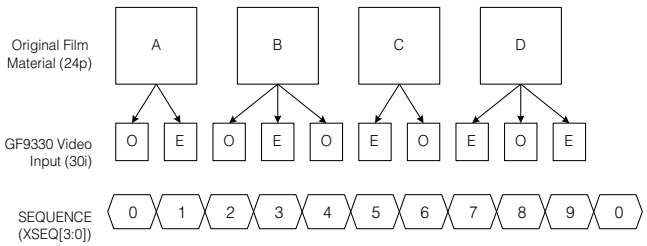


Fig.10 Sequence Detection Input Signals

8.3 Film Rate Down Conversion Mode (MODE= 010)

When configured to operate as a Film Rate Down Converter, the GF9330 removes 3:2 sequences from the input video stream and outputs 24Hz progressive scan video. No filtering of the signal is performed in this mode of operation. The external 3:2 sequence pins (XSEQ[3:0]) are used in this mode, the setting of the MODE_32 bit has no effect.

Note: In this mode, 3:2 compensation remains in effect at all times.

8.4 Film Rate Down Conversion Mode, Segmented Frame Output (MODE= 011)

This mode operates in the same manner as the Film Rate Down Converter mode, but outputs the progressive scan video in segmented frame format.

8.5 Video Pass Through Mode (MODE=111)

The GF9330, operating in Pass-through Mode, will pass through only the active portion of the input video signal. All other ANC data will be lost from the input data stream.

9. OUTPUT DATA FORMATS

The GF9330 supports multiple output data formats. The output data format depends on the input format selected as well as the defined operating mode.

Table 7 specifies the available output formats for the GF9330.

TABLE 7: Output formats

STD	INPUT FORMAT	DE-INTERLACING		FILM RATE DOWN-CONVERSION		BYPASS
		I-TO-P CONVERT MODE=000	FIELD MERGING MODE=001	I-TO-P CONVERT MODE=010	I-TO-PSF CONVERT MODE=011	MODE=111
0	525i (30/1.001) SMPTE 125M	525p (60/1.001) SMPTE 293M See Note: 1	525p (60/1.001) SMPTE 293M See Note: 1	525p (24/1.001 See Note: 1	525p (24/1.001) See Note: 1	See Note: 1
1	Reserved	NA	NA	NA	NA	
2	525i (30/1.001) SMPTE 267M - 16x9	525p (60/1.001) 16x9 See Note: 1	525p (60/1.001) 16x9 See Note: 1	525p (24/1.001) 16x9 See Note: 1	525PsF (24/1.001) 16x9 See Note: 1	See Note: 1
3	Reserved					
4	625i (25) EBU Tech 3267	625p (50) ITU-R BT.1358 See Note: 1	625p (50) ITU-R BT.1358 (2:2 Pulldown Comp.) See Note: 1	625p (25) (2:2 Pulldown Comp.) See Note: 1	625PsF (25) (2:2 Pulldown Comp.) See Note: 1	See Note: 1
5	Reserved					
6	625i (25) 16 x9 ITU-R BT.601 Part B	625p (50) 16 x 9 See Note: 1	625p (50) 16 x 9 See Note: 1	625p (25) 16 x 9 See Note: 1	625PsF (25)16 x 9 See Note: 1	See Note: 1
7	Reserved					
8	525p (60/1.001) SMPTE 293M	NA	NA	NA	NA	See Note: 1
9	Reserved					
10	Reserved					
11	Reserved					
12	625p (50) ITU-R BT-1358	NA	NA	NA	NA	See Note: 1
13	625p (50) 16x9	NA	NA	NA	NA	See Note: 1
14	Generic SD 4:1:1	Refer to section 2.2				See Note: 1
15	Generic SD 4:2:2	Refer to section 2.2				See Note: 1

TABLE 7: Output formats (continued)

STD	INPUT FORMAT	DE-INTERLACING		FILM RATE DOWN-CONVERSION		BYPASS
		I-TO-P CONVERT MODE=000	FIELD MERGING MODE=001	I-TO-P CONVERT MODE=010	I-TO-PSF CONVERT MODE=011	MODE=111
16	720p (60 & 60/1.001) SMPTE 296M Jan '99 Draft (System #1 and #2)	NA	NA	NA	NA	See Note: 2
17	720p (30 & 30/1.001) SMPTE 296M Jan '99 Draft (System #4 and #5)	NA	NA	NA	NA	See Note: 2
18	1080p (30 & 30/1.001) SMPTE 274M (System #7 and #8)	NA	NA	NA	NA	See Note: 2
19	720p (50) SMPTE 296M Jan '99 Draft (System #3)	NA	NA	NA	NA	See Note: 2
20	1080p (25) SMPTE 274M (System #9)	NA	NA	NA	NA	See Note: 2
21	720p (25) SMPTE 296M Jan '99 Draft (System #6)	NA	NA	NA	NA	See Note: 2
22	1080p (24 & 24/1.001) SMPTE 274M (System #10 and #11)	NA	NA	NA	NA	See Note: 2
23	720p (24 & 24/1.001) SMPTE 296M Jan '99 Draft (System #7 and #8)	NA	NA	NA	NA	See Note: 2
24	1080i (30 & 30/1.001) SMPTE 274M (System #4 and #5)	1080p (60 & 60/1.001) SMPTE 274M (System #1 and #2) See Note: 3	1080p (60 & 60/1.001) SMPTE 274M (System #1 and #2) See Note: 3	1080p (24 & 24/1.001) SMPTE 274M See Note: 2	1080PsF (24 & 24/1.001) Draft RP May 99 See Note: 2	See Note: 2

TABLE 7: Output formats (continued)

STD	INPUT FORMAT	DE-INTERLACING		FILM RATE DOWN-CONVERSION		BYPASS
		I-TO-P CONVERT MODE=000	FIELD MERGING MODE=001	I-TO-P CONVERT MODE=010	I-TO-PSF CONVERT MODE=011	MODE=111
25	1080PsF (30 & 30/1.001) Draft RP May 99 (System #12 and #13)	1080p (30 & 30/ 1.001) SMPTE 274M See Note: 4	NA	NA	NA	See Note: 2
26	1080i (25) SMPTE 274M (System #6)	1080p (50) SMPTE 274M (System #3) See Note: 3	1080p (50) SMPTE 274M (System #3) (2:2 Pulldown Comp.) See Note: 3	1080p (25) SMPTE 274M (System #9) (2:2 Pulldown Comp.) See Note: 2	NA	See Note: 2
27	1080PsF (25) Draft RP May 99 (System #14)	1080p (25) SMPTE 274M (System #9) (PsF to P) See Note: 4	NA	NA	NA	See Note: 2
28	1080i (25) SMPTE 295M (System #2)	1080p (50) SMPTE 295M (System #1) See Note: 3	1080p (50) SMPTE 295M (System #1) (2:2 Pulldown Comp.) See Note: 3	1080p (25) SMPTE 274M (System #9) (2:2 Pulldown Comp.) See Note: 2	NA	See Note: 2
29	1080PsF (24 & 24/1.001) Draft RP May 99 (System #15 & #16)	1080p (24 & 24/ 1.001) SMPTE 274M (System #10 & #11) (PsF to P) See Note: 4	NA	NA	NA	See Note: 2
30	1035i (30 & 30/1.001) SMPTE 260M	1035p (60&60/ 1.001)See Note: 3	1035p (60&60/ 1.001) See Note: 3	1035p (24&24/1.001) See Note: 2	1035p (24&24/1.001) See Note: 2	See Note: 2
31	Generic HD 4:2:2	Refer to section 2.2				See Note: 2

NOTES:

1. Y/C Output Multiplexed on Y1_OUT[11:0].
2. Y Output on Y1_OUT[11:0] C Output on C1_OUT[11:0].
3. Odd (first) pixel Y data on Y1_OUT[11:0], Even (second) pixel Y data on Y2_OUT[11:0], Odd (first) pixel C data on C1_OUT[11:0], Even (second) pixel C data on C2_OUT[11:0].
4. These standards cannot be used in stand alone mode. OM_MODE[2:0] register within the host interface must be configured to “110” in order to achieve output port operation as described in Note: 2.

9.1 Output Video Frame Cropping

The GF9330 provides programmable output video cropping in both the horizontal and vertical directions. Any rectangular window within the full output active frame (or field) is selectable for output, with all video data outside of this rectangular window cropped (set to the blanking level). The H_OUT, V_OUT, F_OUT signals are generated to provide timing for the cropped video frame. The embedded TRSs I remain in the original positions.

Output video cropping is enabled with the CROP_EN bit within the host interface.

Cropping in the horizontal direction is implemented based on the settings of the CROP_H_CROP_SIZE and CROP_H_LINE_SIZE. The CROP_H_CROP_SIZE parameter specifies the number of active pixels to blank at the beginning of each line. The CROP_H_LINE_SIZE parameter specifies the length of the line to output, following the cropped pixels on the left side of the line. CROP_H_CROP_SIZE and CROP_H_LINE_SIZE are each allocated 12-bits within the host interface.

Two levels of horizontal edge smoothing are provided. The CROP_SMOOTH_EDGE bit within the host interface, dictates no smoothing when set low, and 3 pixel smoothing when set high.

Cropping in the vertical direction is implemented based on the settings of the CROP_V_CROP_SIZE and CROP_V_FRAME_SIZE. The CROP_V_CROP_SIZE parameter specifies the number of active lines to blank at the beginning of each frame. The CROP_V_FRAME_SIZE parameter specifies the number of lines to output, following the cropped lines at the top of the frame (or field). CROP_V_CROP_SIZE and CROP_V_FRAME_SIZE are each allocated 12-bits within the host interface.

Valid H_OUT, V_OUT and F_OUT are always be present even when output signals contain embedded TRS signals. When outputting one of the standards with embedded TRSs, H_OUT, V_OUT and F_OUT is synchronized with the GF9330's output data stream. (V_OUT and F_OUT transition on EAV sequences).

Refer to Figure 11 for a pictorial representation of the cropping function.

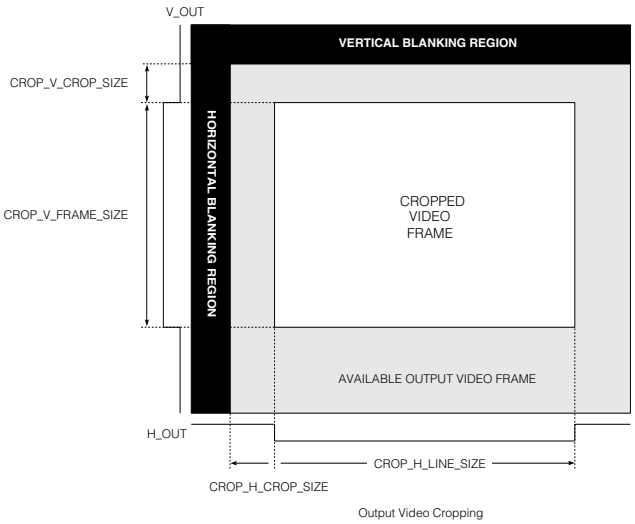


Fig. 11 Output Video Cropping

9.2 12-BITS OUTPUT RESOLUTION

All output data busses are 12-bits in total resolution. Output Y data is always an unsigned data format. Output Cr Cb is always in a offset binary data format. Relative to the input data stream the 12-bits outputs are formatted as 10.2 (2 LSB extensions).

9.3 Controllable Rounding and Clipping on Output Data

The GF9330 provides a wide range of round/clipping options based on the setting of CL_RND[2:0] bits within the host interface as shown in Table 8.

TABLE 8: CL_RND[2:0]

CL_RND[2]	CL_RND[1]	CL_RND[0]	DESCRIPTION
0	0	0	12-bit Output. All channels rounded to 10.2 output resolution.
0	0	1	10-bit Output #1. Data clipped/rounded to 0 to 1023.
0	1	0	10-bit Output #2. Data clipped/rounded to 4-1019.
0	1	1	10-bit Output #3. Y data clipped/rounded 64 to 940. Cr/Cb clipped/rounded 64 to 960.
1	0	0	RESERVED
1	0	1	8-bit Output #1. Data clipped/rounded to 0 to 255.
1	1	0	8-bit Output #2. Data clipped/rounded to 1 to 254.
1	1	1	8-bit Output #3. Y data clipped/rounded 16 to 235. Cr/Cb clipped/rounded 16 to 240.

10. SEQUENCE DETECTION

The GF9330 supports two modes of operating with respect to 3:2 sequence detection (internal and external modes) as described in Table 9. One bit in the host interface is reserved for the MODE_32 bit.

TABLE 9: 3:2 Mode Select

MODE_32	DESCRIPTION
0	Internal. 3:2 sequence are automatically detected in the input data stream. The GF9330 reports 3:2 lock and 3:2 sequence information in the host interface registers called LOCK_32 and SEQUENCE. The GF9330 also reports this information on the XSEQ[3:0] pins configured as outputs.
1	External. The GF9330 accepts a 3:2 sequence from the XSEQ[3:0] pins configured as inputs.

10.1 INTERNAL 3:2 DETECTION

When set to operate in internal 3:2 detect mode, the GF9330 automatically detect a 3:2 pull-down sequence in the incoming video data stream. If a 3:2 sequence is detected, the GF9330 sets the LOCK_32 control bit in the host interface high. The LOCK_32 pin is also asserted high once the sequence has been detected.

The actual 3:2 sequence information is reported in the SEQUENCE[3:0] register within the host interface and on the XSEQ[3:0] pins. Refer to Figure 10 for a pictorial representation of the 3:2 sequence reporting.

10.2 External 3:2 Detection

When set to operate in external mode, the user will supply the 3:2 sequence information to the XSEQ[3:0] pins. The GF9330 uses this information to properly de-interlace the input signal or to perform 60Hz to 24Hz conversion depending on the state of the MODE[2:0] register in the host interface or MODE[2:0] pins.

When operating in this mode the input 3:2 sequence information relates to the input data stream. The 3:2 sequence information requires updating during the sixth blank line of the vertical blanking interval, identifying the sequence number for the following field.

10.3 Sequence Detection and Compensation

The GF9330 supports external 2:2 sequence detection. A LOCK_22 pin is provided to indicate the presence of a 2:2 sequence. The sequence information is inherently embedded in the interlaced video input data, and is identified with the F_IN signal (either derived from the embedded TRSs or supplied from the external pin). The LOCK_22 signal will be updated during the first line of each vertical blanking interval.

10.4 Static and Freeze Frame Detection/Compensation

The GF9330 operates in either disabled, automatic or manual mode for detection and compensation of freeze frame conditions within the video input stream. When set to operate in disabled mode (host interface bits, FF_MODE=10), the GF9330 disables the internal freeze frame detection and compensation circuitry and also ignores any information presented to the FF_EN pin or the host interface bit, FF_EN. When set to operate in automatic mode (FF_MODE[2:0]=01) the GF9330 internally detects and compensates for Freeze Frame situations. When a Freeze Frame situation is detected, the GF9330 reports this in the FF_DETECT status bit found in the host interface. This bit is updated at the beginning of a field and remains valid for the remainder of the field. When set to operate in manual mode (FF_MODE=00) the GF9330 monitors the FF_EN pin and the host interface bit, FF_EN to enable or disable Freeze Frame compensation. Static and Freeze Frame detection compensation is further described in Table 10.

TABLE 10: FF_MODE[1:0]

HOST INTERFACE FF_MODE[1:0] REGISTER	EXTERNAL FF_EN Pin	HOST INTERFACE FF_EN Bit	DESCRIPTION
00	0	0	Manual: Freeze Frame Detection and Compensation Disabled
	0	1	Manual: Perform Freeze Frame Compensation
	1	0	
	1	1	
01	x	x	Automatic Freeze Frame detection/compensation
10	x	x	Freeze Frame Detection and Compensation Disabled
11	x	x	Reserved

10.5 Motion Detection and Compensation

The GF9330 operates in disabled, automatic, or external mode for motion detection and compensation. When set to operate in disable mode (host interface bits, MD_MODE=00), the GF9330 does not perform internal motion detection and compensation. When set to operate automatic mode (MD_MODE=01) the GF9330 internally detects and compensates for motion. When set to operate in external mode (MD_MODE=10) the GF9330 monitors the XMVT_IND pins to perform motion detection and compensation. Motion detection and compensation control is further described in Table 11.

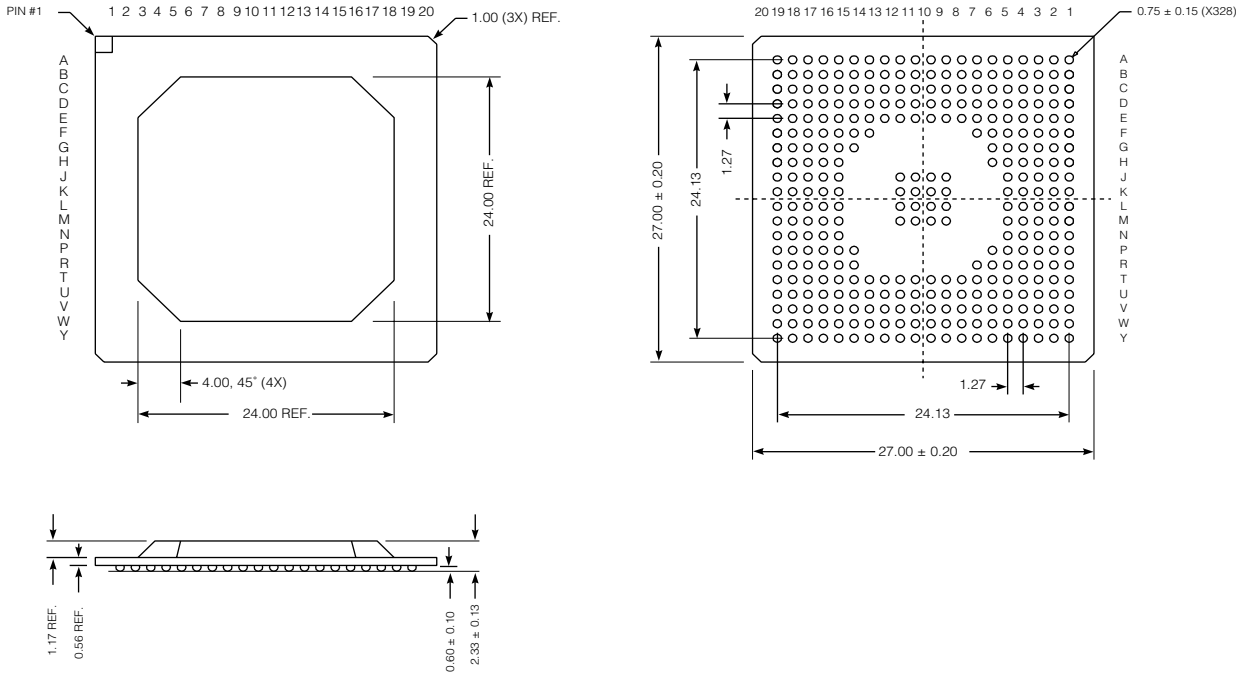
TABLE 11: MD_MODE[1:0]

HOST INTERFACE MD_MODE[1:0] REGISTER	EXTERNAL XMVT_IND[1:0] PINS	DESCRIPTION
00	xx	Disabled Mode
01	xx	Automatic Mode
10	 00 01 10 11	External Mode: Static Transition Motion Reserved
11	xx	Reserved

10.6 Processing Latency

In de-interlacing mode (with the exception of progressive segmented frame to progressive format conversion), the GF9330 processing latency is constant regardless of input or output format selection. In all other modes, (including progressive segmented frame to progressive format conversion and Film Rate Down Conversion) the GF9330 processing latency is unique yet constant regardless of input or output format selection.

PACKAGE DIMENSIONS



DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

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