

Features

- Bidirectional interface between GTLP and TTL logic levels
- Designed with Edge Rate Control Circuit to reduce output noise on the GTLP port
- Power up/down high impedance for live insertion
- 1:6 fanout clock driver for TTL port
- Lower Drive (12mA) on TTL Port to reduce noise
- 1:2 fanout clock driver for GTLP port
- TTL compatible driver and control inputs
- Flow-through architecture optimizes PCB layout
- Open drain on GTLP to support wired-or connection
- Operating Temperature: -40°C to $+85^{\circ}\text{C}$
- Package:
–24-Pin 173 mil wide plastic TSSOP (L24)

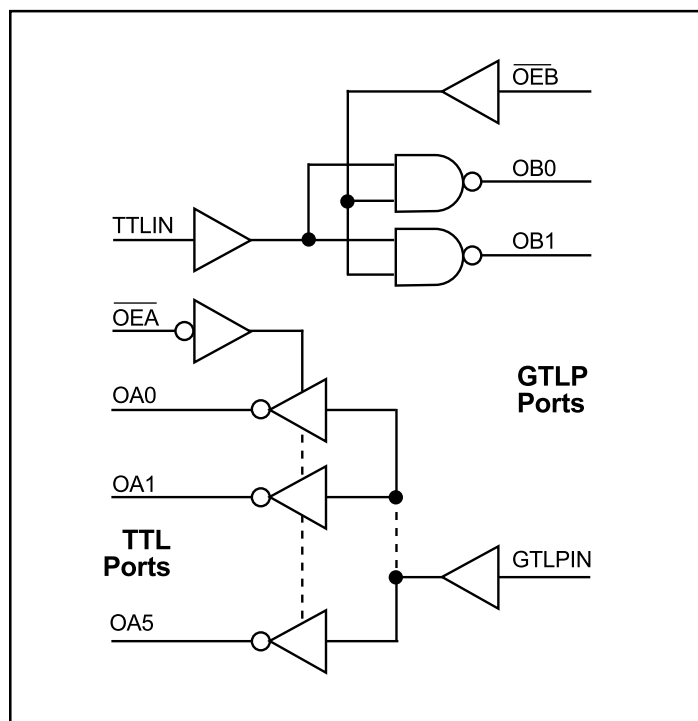
Product Description

Pericom Semiconductor's GTLP series of logic circuits are produced using the Company's advanced 0.5 micron CMOS technology, achieving industry leading performance.

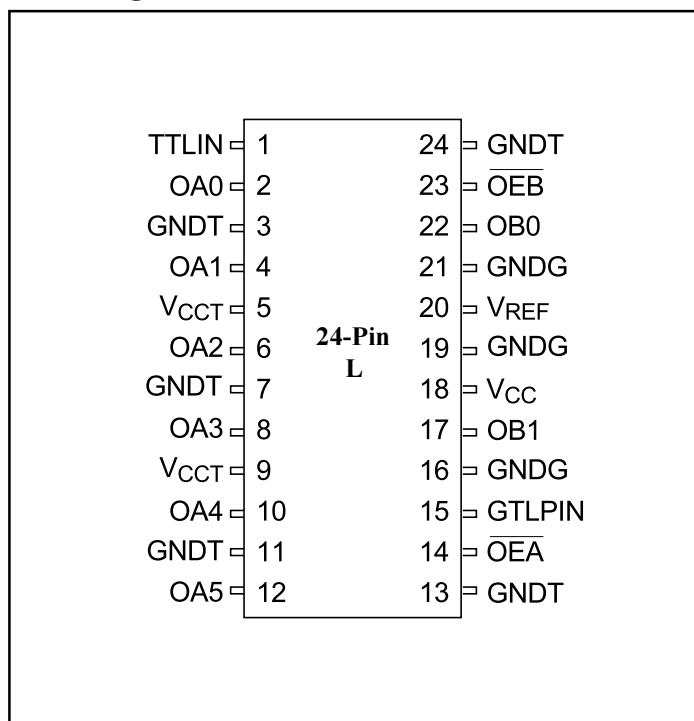
The GTLP6C816 is a clock driver that provides TTL to GTLP signal level translation (and vice versa). The device provides a high-speed interface between cards operating at TTL logic levels and a backplane operating at GTLP logic levels. High-speed backplane operation is a direct result of GTLP's reduced output swing ($<1\text{V}$), reduced input threshold levels, and output edge-rate control which minimizes bus settling times.

Pericom's GTLP has internal edge-rate control. Its function is similar to BTL or GTL but with different output levels and receiver threshold. GTLP output low voltage is typically less than 0.5V , the output level HIGH is 1.5V and the receiver threshold is 1.0V .

Logic Block Diagram



Pin Configuration



Functional Description

The GTLP6C816 is a clock driver that provides TTL to GTLP clock translation, and GTLP-to-TTL clock translation. The TTL-to-GTLP direction is a 1:2 clock driver path with a single Enable pin ($\overline{\text{OEB}}$).

For the GTLP-to-TTL direction, the clock receiver path is a 1:6 buffer with a single Enable control ($\overline{\text{OEA}}$). Data polarity is inverting for both directions.

Pin Descriptions

Pin Names	Description
TTLIN, GTLPIN	Clock Inputs (TTL and GTLP respectively)
$\overline{\text{OEB}}$	Output Enable (Active LOW) GTLP Port (TTL Levels)
$\overline{\text{OEA}}$	Output Enable (Active LOW) TTL Port (TTL Levels)
V_{CCT} , GNDT	TTL Output Supplies (5V)
V_{CC}	Internal Circuitry V_{CC} (5V)
GNDG	OBn GTLP Output Grounds
V_{REF}	Voltage Reference Input
OA0 - OA5	TTL Buffered Clock Outputs
OB0 - OB5	GTLP Buffered Clock Outputs

Truth Table

Inputs		Outputs
TTLIN	$\overline{\text{OEB}}$	OBn
H	L	L
L	L	H
X	H	High Z
GTLPIN	$\overline{\text{OEA}}$	OAn
H	L	L
L	L	H
X	H	High Z

Absolute Maximum Ratings⁽¹⁾

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage (V _{CC})	–0.5V to +7.0V
DC Input Voltage (V _I)	–0.5V to +7.0V
DC Output Voltage (V _O)	
Outputs 3-State	–0.5V to +7.0V
Outputs Active ⁽²⁾	–0.5V to +7.0V
DC Output Sink Current into OA-Port I _{OL}	32mA
DC Output Source Current into OA-Port I _{OH}	–32mA
DC Output Sink Current into OB-Port in the LOW State I _{OL}	80mA
DC Input Diode Current (I _{IK})	
V _I < 0V	–50mA
DC Output Diode Current (I _{OK})	
V _O < 0V	–50mA
V _O > V _{CC}	+50mA
ESD Rating	>2000V
Storage Temperature (T _{STG})	–65°C to +150°C

Recommended Operating Condition⁽³⁾

Supply Voltage V _{CC}	4.75V to 5.25V
Bus Termination Voltage (V _{TT})	
GTLP	1.47V to 1.53V
V _{REF}	0.98V to 1.02V
Input Voltage (V _I) on INA-Port and Control Pins	0.0V to 5.5V
HIGH Level Output Current (I _{OH})	
OA-Port	–12mA
LOW Level Output Current (I _{OL})	
OA-Port	+12mA
OB-Port	+34mA
Operating Temperature (T _A)	–40°C to +85°C

Notes:

1. Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.
2. I_O Absolute Maximum Rating must be observed
3. Unused inputs must be held HIGH or LOW.

DC Electrical Characteristics

(Over the recommended Operating Free-Air Temperature Range, $V_{REF} = 1.0$ (Unless otherwise noted))

Symbol		Test Conditions		Min.	Typ. ⁽⁴⁾	Max.	Units
V_{IH}	GTLPIN			$V_{REF} + 0.05$		V_{TT}	V
	Others			2.0			
V_{IL}	GTLPIN			0.0		$V_{REF} - 0.05$	
	Others					0.8	
$V_{REF}^{(5)}$	GTLP				1.0		
	GTL				0.8		
$V_{TT}^{(5)}$	GTLP				1.5		
	GTL				1.2		
V_{IK}		$V_{CC} = 4.75V$	$I_I = -18mA$			-1.2	
V_{OH}	OAn-Port	$V_{CC} = 4.75V$	$I_{OH} = -100\mu A$	$V_{CC} - 0.2$			
			$I_{OH} = -8mA$	2.4			
			$I_{OH} = -12mA$	2.2			
V_{OL}	OAn-Port	$V_{CC} = 4.75V$	$I_{OL} = 100\mu A$			0.2	μA
			$I_{OL} = 8mA$			0.4	
			$I_{OL} = 12mA$			0.5	
V_{OL}	OBn-Port	$V_{CC} = 4.75V$	$I_{OL} = 100\mu A$			0.2	
			$I_{OL} = 34mA$			0.65	
I_I	TTLIN/ Control Pins	$V_{CC} = 5.25V$	$V_I = 5.25V$ $V_I = 0V$			5 -5	
	GTLPIN	$V_{CC} = 5.25V$	$V_I = V_{TT}$ $V_I = 0V$			5 -5	
I_{OFF}	TTLIN	$V_{CC} = 0$	V_I or $V_O = 0V$ to $5.25V$			100	
I_{OZH}	OAn-Port	$V_{CC} = 5.25V$	$V_O = 5.25V$			5	
	OBn-Port		$V_O = 1.5V$			5	
I_{OZL}	OAn-Port	$V_{CC} = 5.25V$	$V_O = 0$			-5	
I_{CC}	OAn or OBn Ports	$V_{CC} = 5.25V$	Outputs HIGH		7	18	mA
			Outputs LOW		7	20	
		$V_I = V_{CC}$ or GND	Outputs Disabled		7	20	
ΔI_{CC}	TTLIN	$V_{CC} = 5.25V$	$V_I = V_{CC} - 2.1$			6	
C_{IN}	Control Pins/ GTLPIN/TTLIN		$V_I = V_{CC}$ or 0		3.5		pF
C_{OUT}	OAn-Port OBn-Port		$V_I = V_{CC}$ or 0		7		
			$V_I = V_{CC}$ or 0		7		

Notes:

- All typical values are at $V_{CC} = 5.0V$ and $T_A = 25^\circ C$
- GTLP, V_{REF} and V_{TT} are specified to 2% tolerance since signal integrity and noise margin can be significantly degraded if these supplies are noisy. In addition, V_{TT} and R_{TERM} can be adjusted to accommodate backplane impedances other than 50W, within the boundaries of not exceeding the DC Absolute I_{OL} ratings. Similarly, V_{REF} can be adjusted to compensate for changes in V_{TT} .

AC Operating Requirements

(Over recommended ranges of supply voltage and operating free-air temperature, $V_{REF} = 1.0$ (Unless otherwise noted)
 $C_L = 30\text{pF}$ for OBn-Port and $C_L = 50\text{pF}$ for OAn-Port.

Symbol	From (Input)	To (Output)	Min.	Typ. ⁽⁶⁾	Max.	Units
t _{PLH} t _{PHL}	TTLIN	OBn	0.5 0.5	3.8 2.8	4.5 3.5	ns
t _{PLH} t _{PHL}	$\overline{\text{OEB}}$	OBn	1.5 1.5	6.4 3.2	6.5 5.0	
t _{RISE}	Transition Time. OB Outputs (20% to 80%)			2.3		
t _{FALL}	Transition Time. OB Outputs (20% to 80%)			2.3		
t _{RISE}	Transition Time. OA Outputs (10% to 90%)			2.0		
t _{FALL}	Transition Time. OA Outputs (10% to 90%)			2.0		
t _{pZH} , t _{pZL} t _{pLZ} , t _{pHZ}	$\overline{\text{OEA}}$	OAn	0.5 0.5	3.6 3.8	6.5 6.5	
t _{PLH} t _{PHL}	GTLPIN	OAn	1.5 1.5	3.0 3.0	5.5 5.5	
t _{OSHL} , t _{OSLH} ⁽⁷⁾	Common Edge Skew			0.15	0.25	

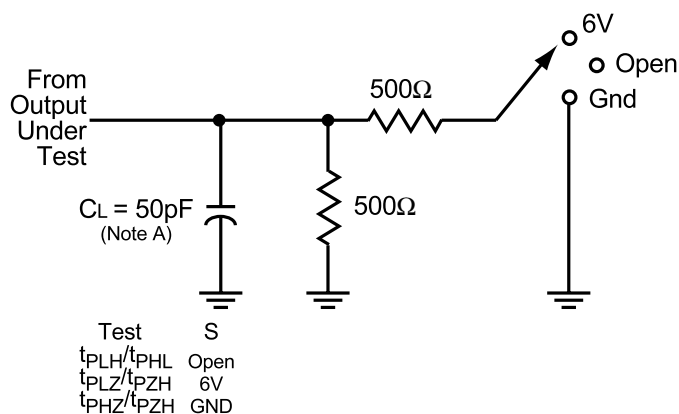
Notes:

6. All typical values are at $V_{CC} = 5.0\text{V}$ and $T_A = 25^\circ\text{C}$

7 Skew specs are given for specific worst case V_{CC} Temp. Skew values between the OBn outputs could vary on the backplane owing to loading and impedance seen by the device.

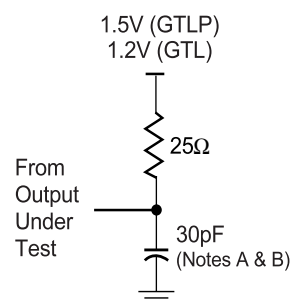
Test Circuits and Timing Waveforms

Test Circuit for A Outputs



Note A: C_L includes probes and jig capacitance

Test Circuit for B Outputs

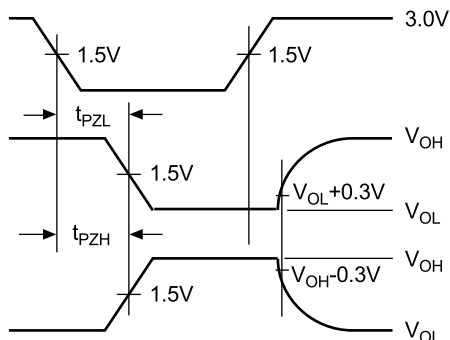


Notes:

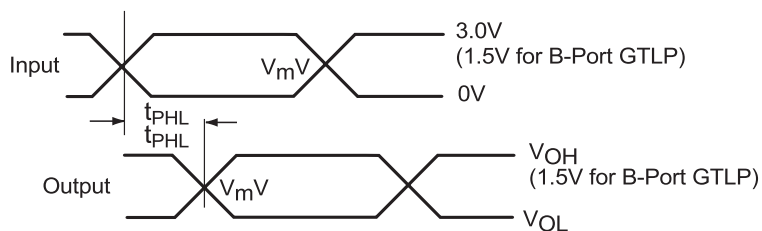
A. C_L includes probes and jig capacitance.

B. For B-Port outputs, $C_L = 30\text{pF}$ is used for worst case.

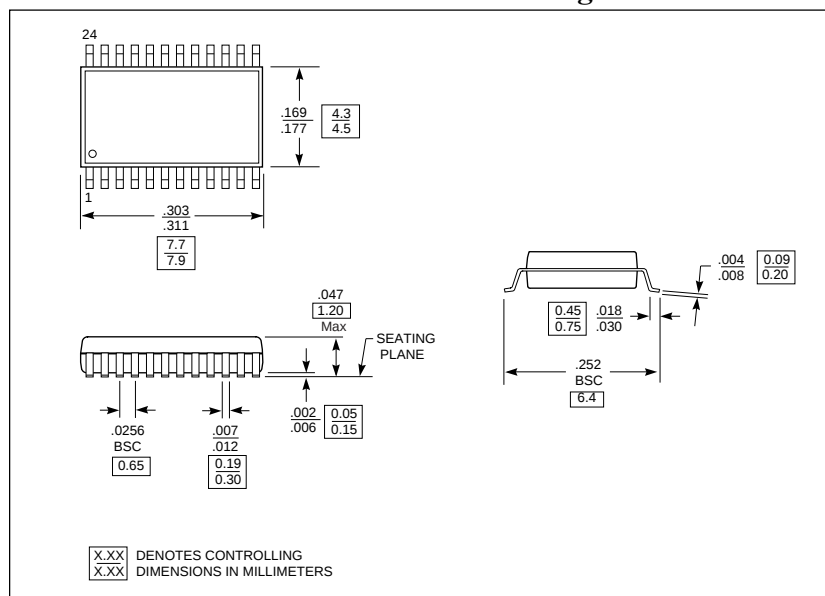
Voltage Waveforms Enable and Disable Times A-Port



Voltage Waveforms Propagation Delay
($V_m = 1.5V$ for A-Port and 1.0 for B-Port)



24-Pin 173 Mil Wide Plastic TSSOP Package



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