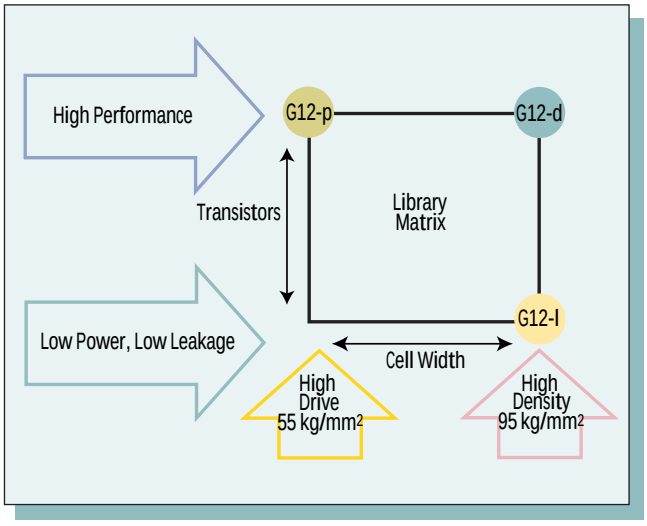
G12™ ASIC Cell-Based Product

Twelfth Generation ASIC Technology

Overview

LSI Logic's G12 ASIC Cell-Based product, with its three digital libraries, offers unprecedented options for system ASIC designers to optimize their ASIC or system-on-a-chip design for end product applications. Within the targeted computer, communications, consumer and storage markets, there are divergent requirements for ASIC products, namely, low power, high performance and high density.
The G12 product addresses these requirements by utilizing a uniquely modular 0.18-micron L-drawn (0.13-micron L-effective) CMOS process combined with three cell-based libraries optimized for performance, density and low static power.
The G12 product offers system architects 33,000,000 usable gates on a single chip.

The powerful combination of LSI Logic's G12 product, containing advanced digital and mixed-signal functions together with the advanced FlexStream 2.0 design methodology, CoreWare® design program and an industry-leading package offering, raises the bar on system-on-a-chip and leading-edge ASIC capabilities.



The G12 product has three libraries optimized for end design requirements.

Description

The G12 product has three differentiated libraries allowing designers to optimize system requirements specifically for:

- High performance: G12-p. Applications include workstations, servers, and telecom switches. The G12-p library utilizes high-performance cells and high-performance transistors.
- High density: G12-d. Applications include networking, communications, storage and consumer products, and personal computer systems. The G12-d library utilizes high-density cells and high-performance transistors.
- Low power: G12-l. Applications include battery-operated cellular phones and digital consumer electronics. The G12-l library utilizes low leakage transistors and high-density cells.

Additional benefits include the ability to integrate different libraries at a macro-level on the same chip, thus providing a true system-on-a-chip capability.

Features/*Benefits*

- ASIC technology with 0.18 micron L-drawn and 0.13 micron L-effective transistors
- *Enables higher density, higher performance ASIC/SOC designs*
- 3 libraries optimized for design requirements
- *Libraries optimized for high density, high performance and low power*
- Up to 33 million usable gates
- *Maximizes performance and IP reusability*
- Hierarchical Design Methodology (HDM)
- *Shortens design cycles by reducing risk and ensuring first-time design success*
- Supports up to 6 layers of metals
- *Support for large flat layout designs as well as hierarchical designs; the sixth layer supports Flip Chip redistribution*
- Submicron metal pitch
- *Metal rules and configurations optimized for high gate utilization and performance*
- High-performance, high-density multi-port memory compilers
- *Multiple memory compilers to meet different application requirements*
- Extended I/O library
- *Industry-standard I/Os and high voltage tolerant I/Os for backward compatibility: 3.3 V/2.5 V/1.8 V LVTTL, 3.3 V/5.0 V tolerant SSTL, HSTL, GTL, NTL, GTL+, PCI, AGP, LVDS, SCSI, 1284, 1394, USB, PECL BZ (Controlled Impedance)*
- Broad mixed-signal core offering
- *Range of mixed signal cores to reduce system costs and improve reliability*

LSI LOGIC®

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G12-p (Performance)

The G12-p library delivers the highest performance solution at 1.8 V with nominal gate delays less than 24 ps and system clock rates up to 400 MHz. High drive cells are optimized for long interconnects associated with large designs.

G12-d (Density)

The G12-d library delivers the broadest solution for consumer, communications and computer system requirements. This library enables designers to optimize performance, density and power for most applications.

G12-l (Low Power)

The G12-l library delivers an ultra-low power and high-density solution at 22 nW/MHz/Gate. Low dynamic and standby leakage current makes the G12-l the optimal choice for battery-operated devices.

Design Methodology

Advanced delay predictors, sophisticated and silicon verified modeling, RTL optimization, CoreWare library, and extensive LSI Logic and EDA tool support for system, logic and physical design from LSI Logic's FlexStream design solution are all integral components of the G12 design methodology. This hierarchical or flat design methodology maximizes chip-level performance and reliability while reducing design time.

Testability

The G12 product includes leading-edge testability features and tools essential for achieving cost-effective reliable designs. Automatic scan and JTAG insertion, memory BIST, IDDQ testing, an extensive ATPG toolset and DC/AC parametric testing are all part of a complete G12 test portfolio.

Memory

The G12 product includes synchronous and asynchronous SRAMs and ROMs, plus single-port, dual-port, triple-port and quad-port SRAM compilers. Our memory compilers are optimized for high density, high performance and low power to allow designers to achieve the optimal design implementation. LSI Logic also supports TLB and CAM memory subsystems.

Mixed Signal

The G12 product offers a robust and comprehensive mixed-signal solution which includes:

- enhanced transistor technology optimized to support a range of supply voltages and higher performance designs
- precision passive components for die size, cost and component reduction
- a mixed-signal methodology that integrates seamlessly into LSI's FlexStream design environment for easy instantiation of mixed-signal solutions.

CoreWare Design Program

The CoreWare program is a complete design process for delivering system functions reliably and repeatedly on a single chip.

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