G10™-p Deep Submicron ASIC Technology

Datasheet

The G10-p cell-based CMOS ASIC technology is the highest performance, highest density 3.3 V product in LSI Logic's portfolio, and supports consumer, computer, and communications applications. The G10-p ASIC product combined with specialized cores enable optimized solutions for cost effective logic integration of system-on-a-chip designs.

Features and Benefits

- 0.35-micron drawn gate length provides 50 ps gate delays
- Up to 3.5 million usable gates make system-on-a-chip integration a reality for complex systems
- Cell-based solution minimizes die size
- LVDS high-speed I/Os deliver gigabit-per-second data rates
- Wide selection of specialized I/Os, including PCI, PECL, NTL/GTL+, HSTL, and AGP
- 3.3 V and 5 V compatible I/Os preserve system compatibility
- Up to 6 Mbits of RAM and 10 Mbits of ROM bring system memory on-chip
- 0.7 μW/MHz/gate dissipation manages power in megagate designs
- Predesigned digital and mixed signal CoreWare® cores accelerate product development and increase performance
- Sign-off support for industry-leading third-party verification tools in the FlexStream™ design solution
- Extensive package selection - including BGA, PQFP, and MQUAD meet a range of system requirements
- Integration of test solutions, such as JTAG, Scan, BIST and I_{DDQ}, accelerate test flow

G10-p Cell-Based ASIC Architecture

The G10-p cell-based product offers the highest density and performance at 3.3 V.

- Small die size for high-volume production

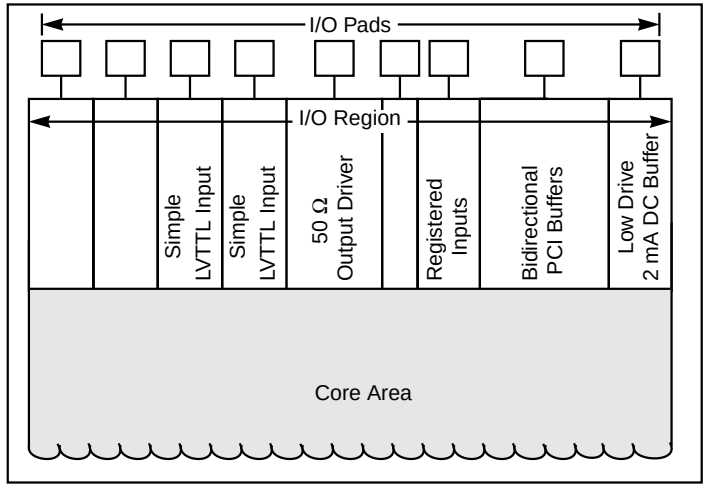
- Area-efficient, low power, and high density memory compilers for implementing RAM and ROM (See Embedded Memory section on page 9)
- Variable aspect ratio I/O cells minimize die size for core-limited designs (See Figure 2 on page 3)
- Extensive selection of synthesis optimized cells for performance, area, testability, and power trade-offs

The G10-p cell-based product speeds development while ensuring that performance and density objectives are achieved. Dense, high-performance system-on-a-chip designs are possible through macrocells, megacells, macrofunctions, megafunctions, and specialty CoreWare blocks that are optimized for area and performance, and that can be readily embedded in designs.

Cell-Based I/O Architecture Saves Area

The G10-p cell-based product contains a variable aspect ratio I/O architecture that minimizes silicon area. I/O cells use only the physical area required for a specific function, not a predefined I/O "slot," as shown in Figure 2. Variable widths allow you to maximize the number of I/Os over a given area.

Figure 1 Minimize Silicon Area with Variable Aspect Ratio I/Os



Advanced Process Technology for 3.3 V Optimized Performance

The G10-p product family achieves its performance and density using an advanced, high-performance CMOS ASIC process technology. The process is robust and reliable, using filled contact openings, highly planar dielectric films, and electromigration-resistant metal compositions. LSI Logic manufactures G10-p ASICs in Santa Clara, California, and in its advanced, high-volume fab in Tsukuba, Japan. Each facility has prototyping capability. Manufacturing capability is also available in the Gresham, Oregon fab.

The G10-p process employs state-of-the-art I-line lithography to produce 0.35-micron drawn gate length CMOS devices, optimized for high performance and high reliability at 3.3 V. G10-p two-layer and three-layer metallization options provide more than twice the interconnect density of 0.5-micron generation CMOS ASICs. An optional fourth metal layer is available for flip-chip interconnect.

High Speed Buffers and Clock Interfaces

In addition to advanced process geometries, performance is optimized through special circuitry:

- 5 V compatible I/Os interface with existing 5 V bus standards.
- High-speed I/Os include PCI, PECL, NTL/GTL+, HSTL, LVDS, and AGP.
- Impedance-matched I/Os eliminate ringing on controlled impedance PC board traces and enable true incident wave signalling.
- Single- and double-ended trunk, local buffered, and balanced clock tree clock distribution architectures ensure less than 400 ps clock skew under worst-case conditions.
- PLLs synchronize internal circuitry to within 300 ps of external ICs, provide on-chip frequency multiplication, and offer clock and data recovery.

5 V Compatible I/Os Simplify Interfacing

As designs transition from 5 V to 3.3 V operation, mixed 5 V and 3.3 V power supplies must be maintained. These mixed-voltage designs require interfacing between 5 V and 3.3 V signals. Although the G10-p

family operates with a single supply voltage of 3.3 V, its 5 V compatible I/Os allow a G10-p device to be connected directly to a 5 V signalling environment.

High Performance, Low-Noise I/Os

LSI Logic minimizes I/O bottlenecks by offering a wide range of high performance I/O solutions, as shown in Table 1. The Peripheral Component Interconnect (PCI) I/Os available in G10-p technology makes it simple to interface to industry-standard PCI buses. It is a fully PCI-compliant solution that makes the G10-p technology ideal for EDP applications.

For telecommunications and other applications that require high-speed I/Os, Pseudo-ECL (PECL) I/Os are available in both single-ended and differential formats. PECL supports the 622 MHz and 155 MHz high speed I/O requirements for SONET interfacing in telecommunication applications.

NTL/GTL+ I/Os offer 300 MHz chip-to-chip and 100 MHz backplane performance. NTL/GTL+ buffers offer high speed and excellent signal quality without the power consumption penalty of bipolar interfaces.

HSTL I/Os offer compliance with the new JEDEC standards for low swing CMOS I/Os. HSTL buffers can deliver chip-to-chip speeds up to 300 MHz through four different classes of 50 Ω or 25 Ω drivers.

Hyper-LVDS™ (Low-Voltage Differential Signal) buffers, compliant with IEEE Standard 1596, enable G10-p I/Os to deliver gigabit-per-second

data rates previously available only with Bipolar or GaAs ASIC technologies.

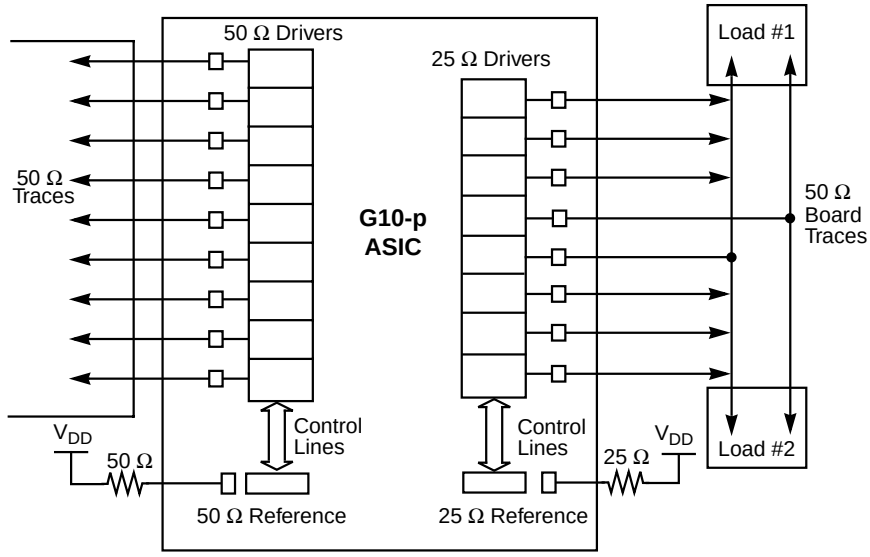
Table 1 I/O Types

I/O Type	Max Frequency (MHz)	Pads	Power at Speed (mW)
LVTTL/CMOS	65	1	85
PCI	66	1	32
Backplane GTL+	83	1	18
Backplane NTL	100	1	21
Matched-impedance LVTTL	155	1	85
Single-ended PECL	155	1	17
Point-to-point GTL+	200	1	10
Point-to-point NTL	300	1	13
HSTL	300	1 or 2	10
Differential PECL	500	2	43
Hyper-LVDS	1200	2	41

Impedance Matched LVTTL I/Os

Impedance compensation adjusts LVTTL output buffer impedance (drive strength) to compensate for variations from nominal conditions in device temperature, operating voltage or process strength. G10-p technology offers impedance-controlled buffers in a range of common system impedance levels (25, 33, 50, 66, and 75 Ω) to allow for the creation of system level interconnects that are free from the signal ringing and reflection that arises from driver-load impedance mismatches. A single I/O pad is used for a reference circuit to match internal device characteristics to an external precision reference resistor. Impedance is controlled within ±10% of the nominal target under commercial conditions (3.3 V, 5% tolerance, T_J = 0 to +115 ˚C), enabling LVTTL system design with I/O frequencies exceeding 100 MHz in unterminated, controlled-impedance signal environments (see Figure 3).

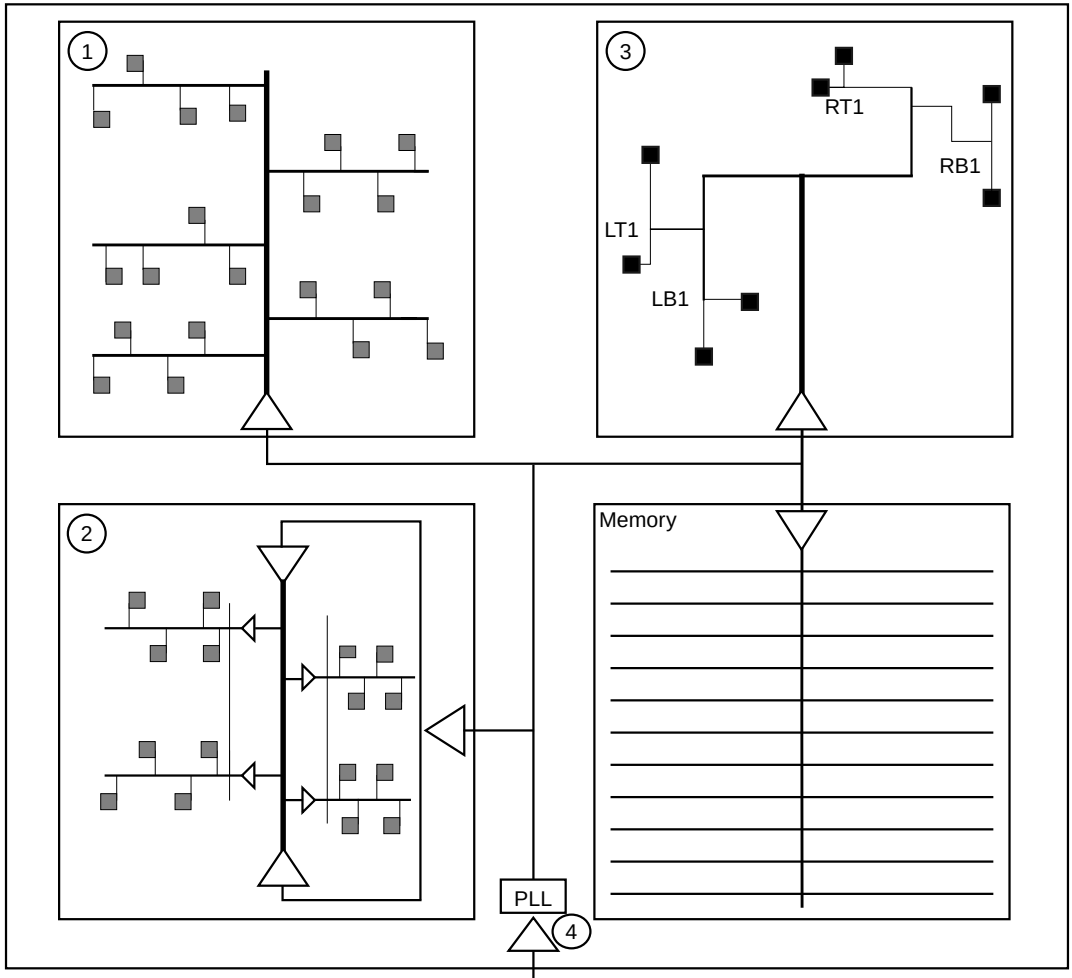
Figure 2 Two Types of Impedance-Controlled Buffers on a Single G10-p ASIC



Low-Skew Clock Distribution

In LSI Logic's Design Methodology, a design is partitioned into blocks, and an optimal clock distribution network is used within each block to minimize clock skew. This methodology ensures less than 400 ps worst-case on-chip clock skew. An example of a chip with different clock architectures in each block is shown in Figure 4.

Figure 3 Low-Skew Clock Distribution Architectures



1. Single-ended tree.
2. Local-buffered tree.
3. Balanced clock tree.
4. PLL.

As a system's clock frequency increases, clock skew consumes a larger percentage of cycle time. The G10-p technology uses special clock distribution architectures and phase-locked loops (PLL) to minimize clock skew on a chip and between chips in a system. Table 2 provides specifications for the different clock distribution architectures.

Table 2 Summary of Clock Distribution Specifications

Architecture	Worst Case Skew[1] (ps)	Max Operating Frequency[1] (MHz)	Max Loads[1]	Nom Rise Time (ns)	Nom Prop Delay (ns)	I/O Slots
Single-ended Tree	400	155	275	1.2	1.1	3
Double-ended Tree	400	155	700	1.2	1.1	7
Local-buffered Tree						
with lclkbuf1a	400	155	5,000	1.6	1.7	7
with lclkbuf2a	400	155	10,000	1.6	1.6	7
with lclkbuf3a	400	155	15,000	1.6	1.6	7
Balanced Clock Tree	400	165	25,000	0.5	2.8	3

1. Tighter skew values and higher operating frequencies can be attained by reducing the number of clock loads.

To maximize system performance, clock skew must be minimized between different ICs in a system. PLLs synchronize the internal ASIC clock to the external system clock, compensating for delays and changes in a clock signal caused by PC board trace lengths and capacitive and resistive loading effects. PLLs also can be used to multiply a signal to a higher frequency. The analog PLL used in the G10-p family operates at up to 400 MHz and reduces interchip clock skew to less than 150 ps. Specifications for high-frequency, low-jitter PLLs are shown in Table 3.

Table 3 PLL Specifications

Parameter	Specification
Operating Frequency Range	30–400 MHz
Phase Detection Error	< 100 ps
Phase Jitter	< 50 ps
Total Error	< 150 ps
Power Dissipation	(Frequency dependent)

Embedded Memory

LSI Logic's Memory Compiler tool automatically generates two and three layer, highly optimized user-specified memory configurations to shorten design development. Table 4 provides typical block sizes and cycle times for three low-power, embedded RAMs generated by the Memory Complier.

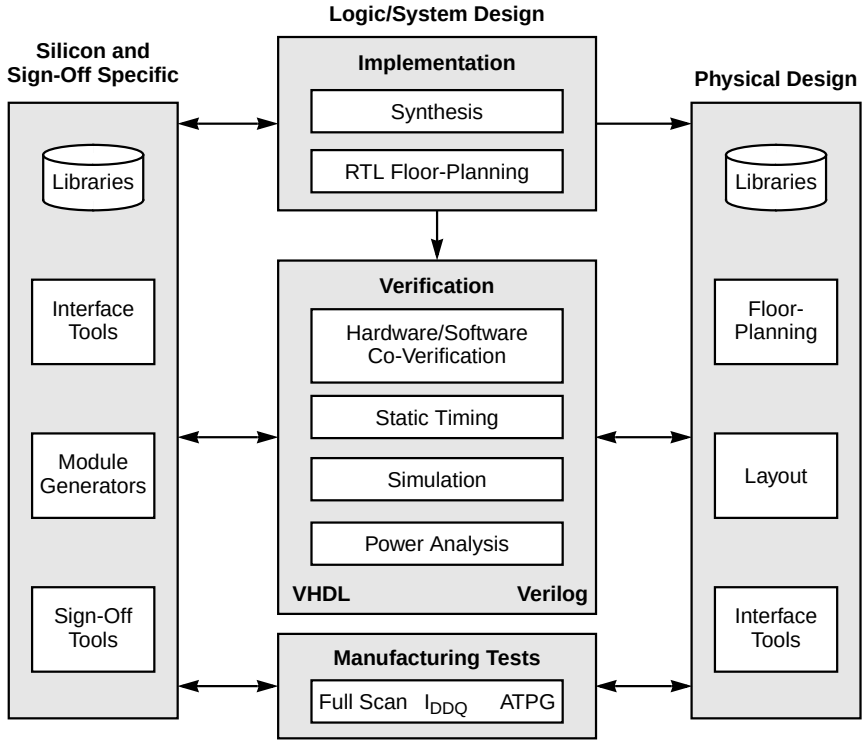
Table 4 Embedded Memory Characteristics

Compiler Name	Memory Type	Maximum Block Size	Access/Cycle Time (typical, ns)
M10P111LA	Asynchronous RAM, 1-port, 1 R/W, low power	512 K x 72 bits	3.5 for 128 x 32 bits
M10P111HS	Synchronous RAM, 1-port, 1 R/W, high density	8 K x 72 bits	5.0 for 1024 x 32 bits
M10P211LA	Asynchronous RAM, 2-port, 1 R/1 W, low power	512 K x 72 bits	3.5 for 128 x 32 bits

FlexStream Design Solution

FlexStream Deep Submicron Design Solution is a comprehensive design automation package consisting of LSI Logic and leading third-party EDA (Electronic Design Automation) tools. The FlexStream solution addresses the challenging system, logic and physical design issues faced by chip designers today by providing a complete methodology that can double chip complexity in half the design time.

Figure 4 FlexStream Deep Submicron Design Solution Flow



As more system functions are integrated onto single chips, FlexStream Design Solution helps solve system issues with its hardware/software co-verification environment. Furthermore, design planning can be achieved earlier at the register-transfer-level (RTL) design phase to ensure that timing, area, and power requirements are met. The FlexStream Design Solution incorporates the CoreWare methodology to take advantage of LSI Logic's extensive catalog of advanced and complex cores. Specifically, FlexStream Design Solution tackles the synthesis iteration bottleneck through an efficient synthesis methodology. Lastly, the FlexStream Design Solution combines a complete set of physical design capabilities with a proven sign-off methodology that allows designers to proceed from system design to physical implementation in a seamless flow.

System Design

Hardware/Software Co-Design

Hardware/software co-design enables designers to debug software and analyze issues early in the system design phase through the use of a virtual hardware prototype. LSI Logic, working with third-party EDA vendors, brings this capability to its customers, who can now enjoy a complete design solution from system level to the integrated circuit level.

CoreWare Methodology

FlexStream Design Solution is a delivery vehicle for the CoreWare design program. LSI Logic offers an extensive catalog of advanced predesigned, preverified cores for applications in consumer, communication, and computer markets. CoreWare designs allow for higher system integration and faster time to market.

CoreWare Cores

Listed below are examples of predeveloped G10-p Technology CoreWare cores that speed the development of system-on-a-chip designs:

- Microprocessors — MiniRISC® MIPS-compatible MPUs and Oak DSP digital signal processors
- Digital video — JPEG, MPEG-1 audio and video decoders, MPEG-2 audio and video decoders, 16VSB, QPSK, MPEG-2 Transport, Motion Estimation Processor (MEP), 3-D rendering
- High speed interconnect — Fibre Channel, SeriaLink®, Ethernet
- Error correction products/channel decoding — Reed-Solomon, Viterbi, QPSK demodulator, Trellis, Hamming, VSB demodulator, deinterleaver, equalizer, randomizer
- Networking — ATM

Contact your local LSI Logic sales representative for core availability.

Mixed Signal Building Blocks

Mixed signal building blocks support analog functionality and offer solutions for data conversion (analog-to-digital and digital-to-analog), communication interfaces, and special clocking (clock deskewing and recovery).

Highly integrated analog content enables high-speed communication and special clocking in products available in LSI Logic's CoreWare library. These products allow a design to include Ethernet, HyperPHY™ (modular high speed transceiver), DVD Channel Clock and Data Recovery, GSM and CDMA Cellular Baseband capability, and GigaBlaze™ (high speed serial interface). Listed below are examples of mixed signal cores supporting data conversion in G10-p:

D/A Converters

- 10-bit Triple Video DAC, 250 MSPS
- 10-bit DDS DAC, 250 MSPS
- 10-bit Low Power DAC, 10 MSPS
- 10-bit Multi-Channel S&H DAC
- 10-bit Switched Cap DAC, 2.0 MSPS
- 10-bit Switched Current DAC, 5.0 MSPS

A/D Converters

- 1-bit Slicer ADC, 10 MSPS
- 4-bit Flash ADC, 10 MSPS
- 6-bit Flash ADC, 90 MSPS
- 8-bit Flash ADC, 40 MSPS
- 4, 5, 6, or 8-bit Pipeline ADC, 25 MSPS
- 10-bit Sigma-Delta ADC, 2500 KSPS
- 10-bit SAR ADC, 250-500 KSPS
- 10-bit SAR ADC, 2.5 MSPS
- 14-bit Sigma-Delta ADC, 10 KSPS

Additional Cores

- 300 MHz Low Jitter, High Spectral Purity PLL
- 14-bit Voice Band Codec

Logic Design

RTL Optimization

FlexStream Design Solution provides complete chip power analysis capability at the register transfer level. Power dissipation is estimated and the information is used for system level power budgeting, as well as package selection. In addition, RTL codes can be rewritten and optimized for low power designs. The LSI Logic's Power program can be used as a final check for gate level power analysis.

Datapath Capabilities

LSI Logic's datapath tool (`lsidpc`) provides a complete solution from RTL partitioning, floorplanning, and synthesis, to place and route. Performance close to that from hand-crafted datapath designs can be achieved in half the time. The `lsidpc` tool helps designers achieve optimal physical implementations for datapath designs. LSI Logic's datapath tool is an integrated and complete solution enabling designers to go from RTL sources to hardmacros or physical implementations.

Specifically, LSI Logic's Datapath Synthesis provides silicon-optimized modules for datapaths. These modules have been carefully designed, leveraging the enhancements of LSI Logic's advanced process technologies to achieve maximum performance. LSI Logic's Datapath Synthesis provides a selection of datapath modules to satisfy any performance or area requirements. Furthermore, LSI Logic's Datapath Compiler performs datapath placement using the floorplan/placement information from LSI Logic's Datapath Synthesis. LSI Logic's datapath methodology is tightly linked to LSI Logic's layout tools, allowing for a seamless integration of datapath into the rest of the layout. In addition, a tight link to LSI Logic's delay prediction tool provides for accurate timing analysis.

Efficient Synthesis

Incorporated in FlexStream Design Solution is the efficient synthesis methodology using tools from Synopsys and Ambit. Now designers can perform the high capacity synthesis that is crucial for today's multi-million gate designs. This efficient synthesis methodology includes advanced technology mapping, pin-based incremental timing analysis with automatic time budgeting, and programmable synthesis.

Furthermore, LSI Logic's Custom Wireload Model provides designers with loading information that matches physical placement. Running placement in conjunction with synthesis allows for further reduction in synthesis iterations.

Physical Design

FlexStream Design Solution includes a complete place and route system with features such as routing congestion management, 5-layer routing capability, Engineering Change Order (ECO) placement, and flip chip routing. New in the area of physical design are hierarchical layout methodology and multi-processing placement capability.

Hierarchical Layout

Hierarchical layout allows designers to lay out blocks independently and in parallel to reduce development time. Layout constraints are passed down to individual blocks, allowing the flexibility to approach layout in either a top-down or bottom-up fashion. Unlike a traditional layout tool which typically requires a flat netlist that limits capacity, FlexStream Design Solution's hierarchical layout tool facilitates physical implementations of million-gate designs. Hierarchical layout also allows designers to integrate more functionality onto a single-chip system.

Incorporated in the hierarchical layout methodology are power planning, bus planning, and clock methodology. Power planning assigns or constrains layers for power to assure proper handling of power dissipation and chip performance. Bus planning allows for better timing control and easier timing analysis. And lastly, clock methodology minimizes clock skews and assures chip functionality.

Multi-Processing Placement

The Multi-Processing Placement System uses multiple processors to solve different portions of a layout problem in parallel, dramatically reducing layout turnaround time. With physical design being pushed toward the front end of the logic design phase, this placement speed improvement facilitates a better and more efficient synthesis methodology.

Test Tools

FlexStream Design Solution offers a comprehensive set of test capabilities including functional, scan, embedded memory, and parametric. Additionally, LSI Logic offers JTAG Builder (IEEE 1149.1) and I_{DDQ} test capabilities to provide a complete test portfolio.

Packaging

As part of the FlexStream Design Solution, Package Planner (`lsi`package) helps designers select the proper package to address lead-count and power dissipation issues. Tightly integrated with other FlexStream tools such as I/O Placer and Floorplanner, Package Planner guarantees designers access to the latest innovations in LSI Logic's packaging technologies, such as flip-chip interconnect. (See Packaging section on page 16.)

EDA Alliances and Tool Portfolio

FlexStream Design Solution provides a seamless interface to third-party design tools giving designers the flexibility to derive a methodology or flow for silicon sign-off. The EDA portfolio contains tools for power analysis, synthesis, simulation, timing analysis and test. LSI Logic is pleased to work with the leading EDA vendors listed below to provide designers the latest EDA tool capabilities to tackle today's complex ASIC designs.

- Ambit Design Systems
- Cadence Design Systems
- IKOS Systems
- Mentor Graphics
- Senté
- Synopsys
- Tera Systems
- Viewlogic Systems

Supported Platforms/Operating Systems

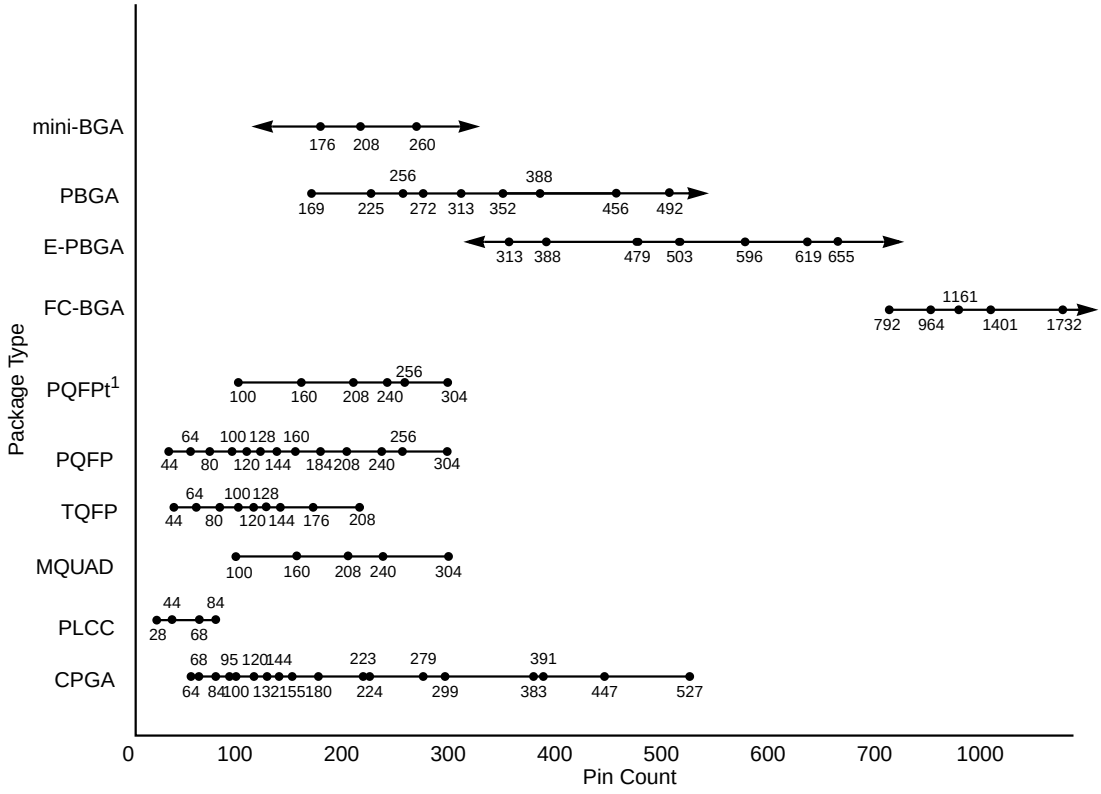
FlexStream Design Solution supports Sun SunOS, Sun Solaris, and HP-UX.

Packaging—Taking Silicon Performance to the System Level

LSI Logic's packaging translates G10-p technology's electrical performance into system performance. Advanced Ball Grid Array (BGA), and flip-chip technologies are available for high pin count, high-frequency applications, as shown in Figure 6. Also offered are well-established PQFP, PQFPt, TQFP, and MQUAD packages for less demanding applications.

All packaging solutions benefit from LSI Logic's experience in providing devices in high volume, on time, and within specification. Across all packaging technologies, LSI Logic provides thermal, electrical, and mechanical modeling of the package and silicon combination. When system design trade-offs must be made, the designer can rely on the experience of LSI Logic's Field Design Engineers to help choose the package best suited for the application. Through research, investment, and by driving industry standards, LSI Logic continues to be the first to market with cost-effective packaging solutions that support high performance requirements.

Figure 5 Package Pin Counts



1. PQFPt is a thermal enhanced PQFP with drop-in heat spreader.

Specifications

This section provides the electrical specifications for the G10-p technology. Table 5 lists the absolute maximum ratings for the G10-p technology. Operation beyond the limits specified in this table may cause permanent device damage. Table 6 lists the recommended operating conditions for the G10-p technology. Operation beyond these limits may impair the useful life of the device. Table 7 lists the G10-p family DC characteristics for standard 3.3 V LVTTL and 5 V compatible buffers. DC characteristics for NTL/GTL+ buffers are provided in Table 8 and DC characteristics for PECL buffers are provided in Table 9. Table 10, Table 11, and Table 12 list the DC characteristics of the HSTL Buffers.

Refer to the *G10™-p Cell-Based ASIC Products Databook* and the *G10™-p Cell-Based ASIC Products Design Manual* for the most current information.

Table 5 Absolute Maximum Rating (Referenced to V_{SS})

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	-0.3 to +3.9	V
LVTTL Input Voltage	V_{IN}	-1.0 to V_{DD} + 0.3	V
5 V Compatible Input Voltage	V_{IN}	-1.0 to 6.5	V
DC Input Current	I_{IN}	±10	µA
Storage Temperature Range (Ceramic)	T_{STG}	-65 to +150	˚C
Storage Temperature Range (Plastic)	T_{STG}	-40 to +125	˚C
ESD Per MIL-STD-883 Test Method 3015, Notice 8, Spec 2001V, Latch-up Over/undershoot: ±150 mA, 125 ˚C; V_{DD} Overstress: 2•V_{DD} (7.2 V)			

1. Ratings in this table are those beyond which permanent device damage is likely to occur. These values should not be used as the limits for normal device operation.

Table 6 Recommended Operating Conditions

Parameter	Symbol	Limits[1]	Unit
DC Supply Voltage	V_{DD}	+3.0 to 3.6	V
Operating Ambient Temperature Range Military Industrial Commercial	 T_A T_A T_A	 -55 to +125 -40 to +85 0 to +70	 ˚C ˚C ˚C
Junction Temperature	T_J	≤150	˚C

1. For normal device operation, adhere to the limits in this table. Sustained operation of a device at conditions exceeding these values, even if they are within the absolute maximum rating limits, may result in permanent device damage or impaired device reliability. Device functionality to stated DC and AC limits is not guaranteed if conditions exceed recommended operating conditions.

Table 7 DC Characteristics—Standard 3.3 V LVTTL Buffers and 5 V Compatible Buffers

Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	–	3.0	3.3	3.6	V
V_{IL}	Input Low Voltage	–	V_{SS} - 0.5	–	0.8	V
V_{IH}	Input High Voltage	LVTTL Com/Ind/Mil Temp Range	2.0	–	V_{DD} + 0.3	V
		5 V Compatible	2.0	–	5.5	V
V_T	Switching Threshold	–	–	1.4	2.0	V
V_{T+}	Schmitt Trigger, Positive-going Threshold	–	–	1.7	2.0	V
V_{T-}	Schmitt Trigger, Negative-going Threshold	–	0.8	1.0	–	V
	Schmitt Trigger, Hysteresis	–	0.6	0.7	–	V
I_{IN}	Input Current Inputs with Pull-down Resistors Inputs with Pull-up Resistors	$V_{IN} = V_{DD}$ or V_{SS} $V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$	-10 35 -35	±1 115 -115	10 222 -214	µA µA µA

Table 7 DC Characteristics—Standard 3.3 V LVTTL Buffers and 5 V Compatible Buffers (Cont.)

Symbol	Parameter	Condition[1]	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	Commercial and Military				
	Type b1	I_{OH} = -1 mA	2.4	–	V_{DD}	V
	Type b2	I_{OH} = -2 mA	2.4		V_{DD}	V
	Type bz25	I_{OH} = TBD mA	2.4		V_{DD}	V
	Type bz50	I_{OH} = TBD mA	2.4		V_{DD}	V
	Type bz75	I_{OH} = TBD mA	2.4		V_{DD}	V
V_{OL}	Output Low Voltage	Commercial and Military				
	Type b1	I_{OL} = 1 mA	–	0.2	0.4	V
	Type b2	I_{OL} = 2 mA		0.2	0.4	V
	Type bz25	I_{OL} = TBD mA		0.2	0.4	V
	Type bz50	I_{OL} = TBD mA		0.2	0.4	V
	Type bz75	I_{OL} = TBD mA		0.2	0.4	V
I_{OZ}	3-state Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10	±1	10	µA
I_{OS}	Output Short Circuit Current[2], bz50	$V_O = V_{DD}$	–	–	TBD	mA
		$V_O = V_{SS}$			TBD	mA
	Output Short Circuit, bz50	$V_O = V_{DD}$	–	–	TBD	mA
		$V_O = V_{SS}$			TBD	mA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}	User Design Dependent			–
C_{IN}	Input Capacitance[3]	Input and Bidirectional Buffers	2.5			pF
		5 V Compatible	3.0			pF
C_{OUT}	Output Capacitance[4]	Output Buffer[3]	2.0			pF
		5 V Compatible	3.0			pF

1. Military junction temperature range: -55 to +150 ˚C, ±10% power supply (ceramic packages only). Industrial junction temperature range: -40 to +125 ˚C, ±5% power supply. Commercial junction temperature range: 0 to 115 ˚C, ±5% power supply.
2. Excluding package capacitance.
3. Output using single buffer structure (excluding package).

Table 8 DC Characteristics—NTL/GTL+ Buffers

Symbol	Parameter	Type	Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	GTL+	–	–	–	V_{REF} - 0.05	V
		NTL	–	–	–	V_{REF} - 0.05	V
V_{IH}	Input High Voltage	GTL+	–	V_{REF} + 0.05	–	–	V
		NTL	–	V_{REF} + 0.05	–	–	V
V_{OL}	Output Low Voltage	GTL+	I_{OL} = 40 mA	–	–	0.4	V
		NTL	I_{OL} = 56 mA	–	–	0.5	V
V_{OH}	Output High Voltage	GTL+	$I_{OH} \leq 10$ µA	V_{TERM}	–	–	V
		NTL	$I_{OH} \leq 10$ µA	V_{TERM}	–	–	V
V_{REF}	External Reference Voltage	GTL+	–	0.7	0.8	0.9	V
		NTL	–	0.9	1.0	1.1	V
V_{TERM}	External Termination Voltage	GTL+	–	1.1	1.2	–	V
		NTL	–	1.4	1.5	–	V
I_{OL}	Output Low Current	GTL+	$V_{OL\ MAX}$	–	–	40	mA
		NTL	$V_{OL\ MAX}$	–	–	56	mA
I_{OH}	Output High Current	GTL+	$V_{OH} = V_{TERM}$	–	–	-10	µA
		NTL	$V_{OH} = V_{TERM}$	–	–	-10	µA

Table 9 DC Characteristics—Single-Ended PECL Buffers

Symbol	Parameter	Driver	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	–	–	–	V_{DD} - 1.4	V
V_{IH}	Input High Voltage	–	V_{DD} - 1.2	–	–	V
V_{OL}	Output Low Voltage	–	–	–	V_{DD} - 1.6	V
V_{OH}	Output High Voltage	–	V_{DD} - 1.0	–	–	V

Table 9 DC Characteristics—Single-Ended PECL Buffers (Cont.)

Symbol	Parameter	Driver	Min	Typ	Max	Unit
V_{REF}	External Reference Voltage	–	V_{DD} - 1.35	V_{DD} - 1.3	V_{DD} - 1.25	V
V_{TERM}	External Termination Voltage	–	V_{DD} - 2.1	V_{DD} - 2.0	V_{DD} - 1.9	V
I_{OL}	Output Low Current	50 Ω	–	–	100	µA
		25 Ω	–	–	100	µA
I_{OH}	Output High Current	50 Ω	-20	–	–	mA
		25 Ω	-40	–	–	mA

Table 10 Single-Ended HSTL Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDQ}	Output Supply Voltage	–	1.4	1.5	1.6	V
V_{REF}	Input Reference Voltage	Peak AC Noise < 2% of DC value	0.68	0.75	0.9	V
V_{IHdc}	Single-ended Input High Voltage (DC)	–	V_{REF} + 0.1	–	V_{DDQ} + 0.3	V
V_{IHac}	Single-ended Input High Voltage (AC)	–	V_{REF} + 0.2	–	–	V
V_{ILdc}	Single-ended Input Low Voltage (DC)	–	-0.3	–	V_{REF} - 0.1	V
V_{ILac}	Single-ended Input Low Voltage (AC)	–	–	–	V_{REF} - 0.2	V

Table 11 Differential HSTL Inputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INdc}	DC Input Voltage	–	-0.3	–	V_{DDQ} + 0.3	V
V_{DIFdc}	DC Differential Input Voltage	–	0.20	–	V_{DDQ} + 0.6	V
V_{DIFac}	AC Differential Input Voltage	–	0.40	–	V_{DDQ} + 0.6	V
V_{CMdc}	Common Mode Input Voltage	V_{TRUE} - [(V_{TRUE} - $V_{COMPLEMENT}$)/2]	0.68	–	0.9	V

Table 12 HSTL Outputs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OHdc}	DC Output High Voltage	I_{OH} varies by output class (See Table 13)	V_{DDQ} - 0.3	–	–	V
V_{OLdc}	DC Output Low Voltage	I_{OL} varies by output class (See Table 13)	–	–	0.4	V

Table 13 HSTL Class Definitions

Class	Description
HSTL Class 1 Buffers (50 Ω drivers)	$I_{OH} \geq +8$ mA, $I_{OL} \geq -8$ mA, Unterminated or 50 Ω Terminated Loads. $V_{TERM} = V_{DDQ}/2$
HSTL Class 2 Buffers (25 Ω drivers)	$I_{OH} \geq +16$ mA, $I_{OL} \geq -16$ mA, Series or Doubly Terminated Loads. $V_{TERM} = V_{DDQ}/2$
HSTL Class 3 Buffers (50 Ω drivers)	$I_{OH} \geq +8$ mA, $I_{OL} \geq -24$ mA, Asymmetric, 50 Ω Terminated Loads. $V_{TERM} = V_{DDQ}$
HSTL Class 4 Buffers (25 Ω drivers)	$I_{OH} \geq +8$ mA, $I_{OL} \geq -48$ mA, Asymmetric, Doubly Terminated Loads. $V_{TERM} = V_{DDQ}$

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